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# Lecture Agenda

- ◆ Microprocessor Systems, Embedded Systems
- ◆ ARM Processors Family
- ◆ Peripheral Devices
- ◆ ARM Processor as Platform for Embedded Programs
- ◆ Methodology of Designing Embedded Systems
- ◆ Interfaces in Embedded Systems



# Serial Peripheral Interface



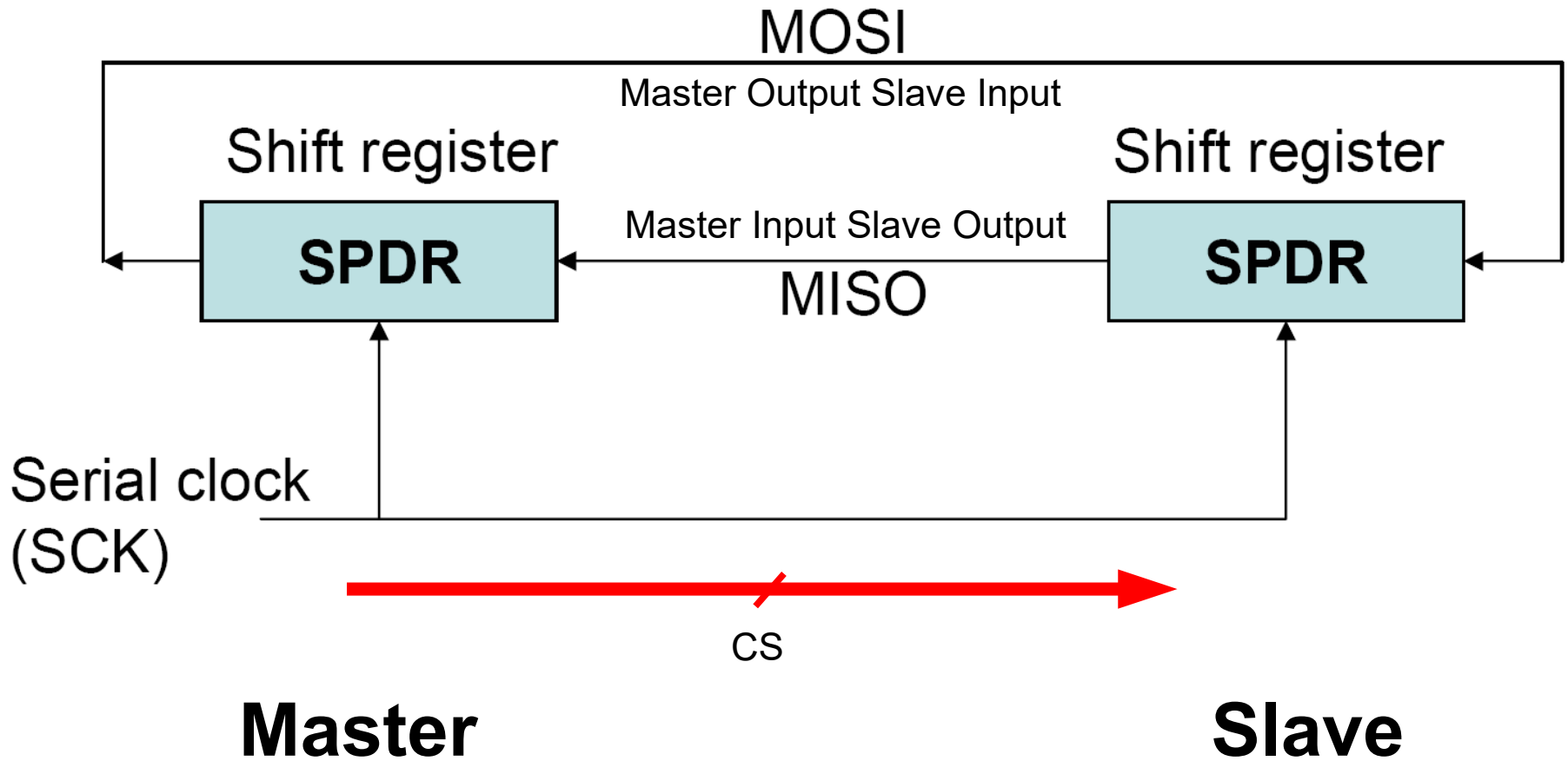
# Serial Peripheral Interface

## Features of SPI:

- Serial synchronous transmission,
- Full duplex, master-slave or master-multi-slave transfers,
- High data transmission speed (>12 Mbit/s),
- Application:
  - External peripheral devices (ADC, DAC, RTC, EEPROM, thermometers, etc...),
  - Auxiliary control, e.g. CCD matrix with high speed parallel interface, SPI used for configuration,
  - Memory cards, e.g. SD/SDHC/MMC.



# Serial Peripheral Interface





# SPI Protocol

**Clock signal configuration:**

**Clock polarisation:**

**Negative CPOL = 0**

(low level, 8 clock signals),

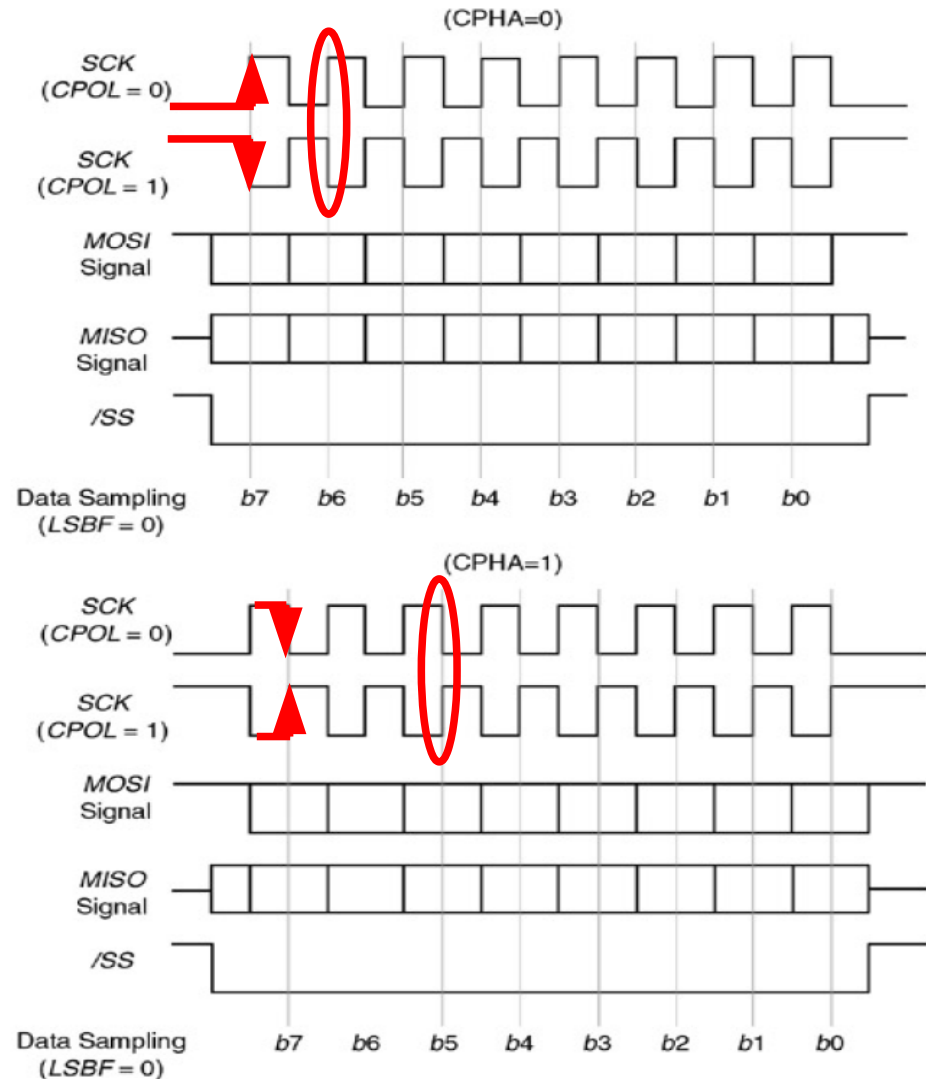
**Positive CPOL = 1**

(high level, 8 clock signals),

**Clock phase:**

Zero clock phase (data sampled on first clock slope),

Delayed clock phase (data sampled on second clock slope).

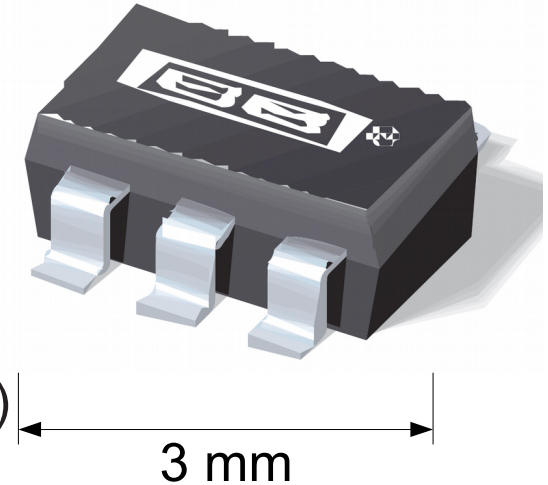




# Thermometer with SPI

## TMP 121:

- SOT 23-6 package,
- Maximum clock speed 15 MHz
- SPI-Compatible Interface
- Resolution: 12-Bit + Sign, 0,0625°C
- Accuracy: ±1.5°C for temp. -25°C - +85°C
- Current consumption in sleep mode: 50µA (max.)
- Power supply: 2,7V to 5,5V



D15	D14	D13	D12	D11	D10	D9	D8
T12	T11	T10	T9	T8	T7	T6	T5

D7	D6	D5	D4	D3	D2	D1	D0
T4	T3	T2	T1	T0	0	Z	Z

Table 1. Temperature Register

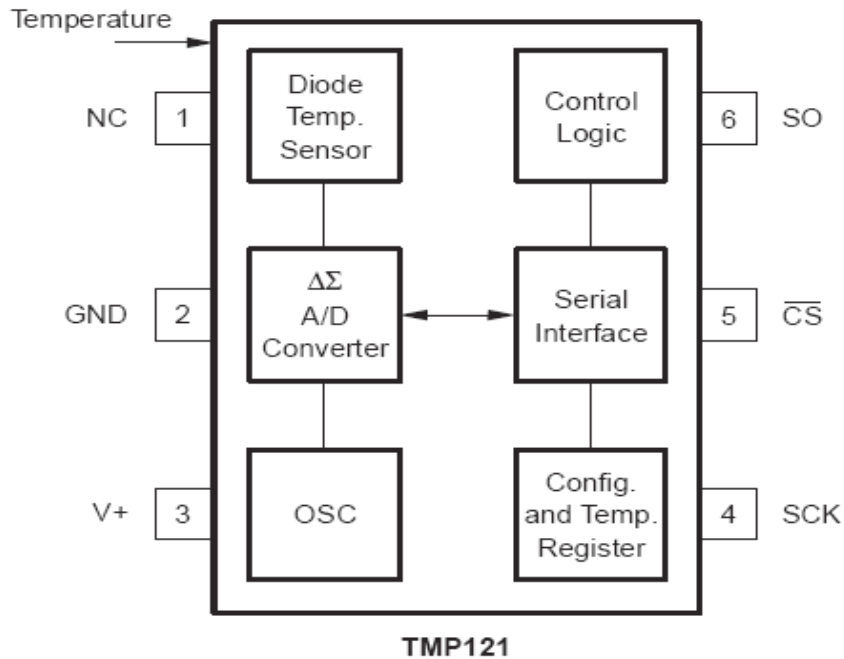
TEMPERATURE (°C)	DIGITAL OUTPUT <sup>(1)</sup> (BINARY)	HEX
150	0100 1011 0000 0000	4B00
125	0011 1110 1000 0000	3E80
25	0000 1100 1000 0000	0C80
0.0625	0000 0000 0000 1000	0008
0	0000 0000 0000 0000	0000
-0.0625	1111 1111 1111 1000	FFF8
-25	1111 0011 1000 0000	F380
-55	1110 0100 1000 0000	E480

<sup>(1)</sup> The last two bits are high impedance and are shown as 00 in the table.

Table 2. Temperature Data Format

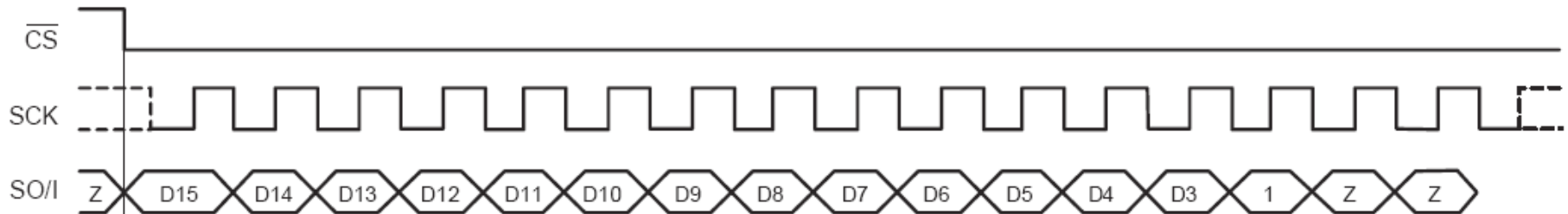


# SPI Frame of TMP121 Thermometer



D15	D14	D13	D12	D11	D10	D9	D8
T12	T11	T10	T9	T8	T7	T6	T5
D7	D6	D5	D4	D3	D2	D1	D0
T4	T3	T2	T1	T0	0	Z	Z

Table 1. Temperature Register







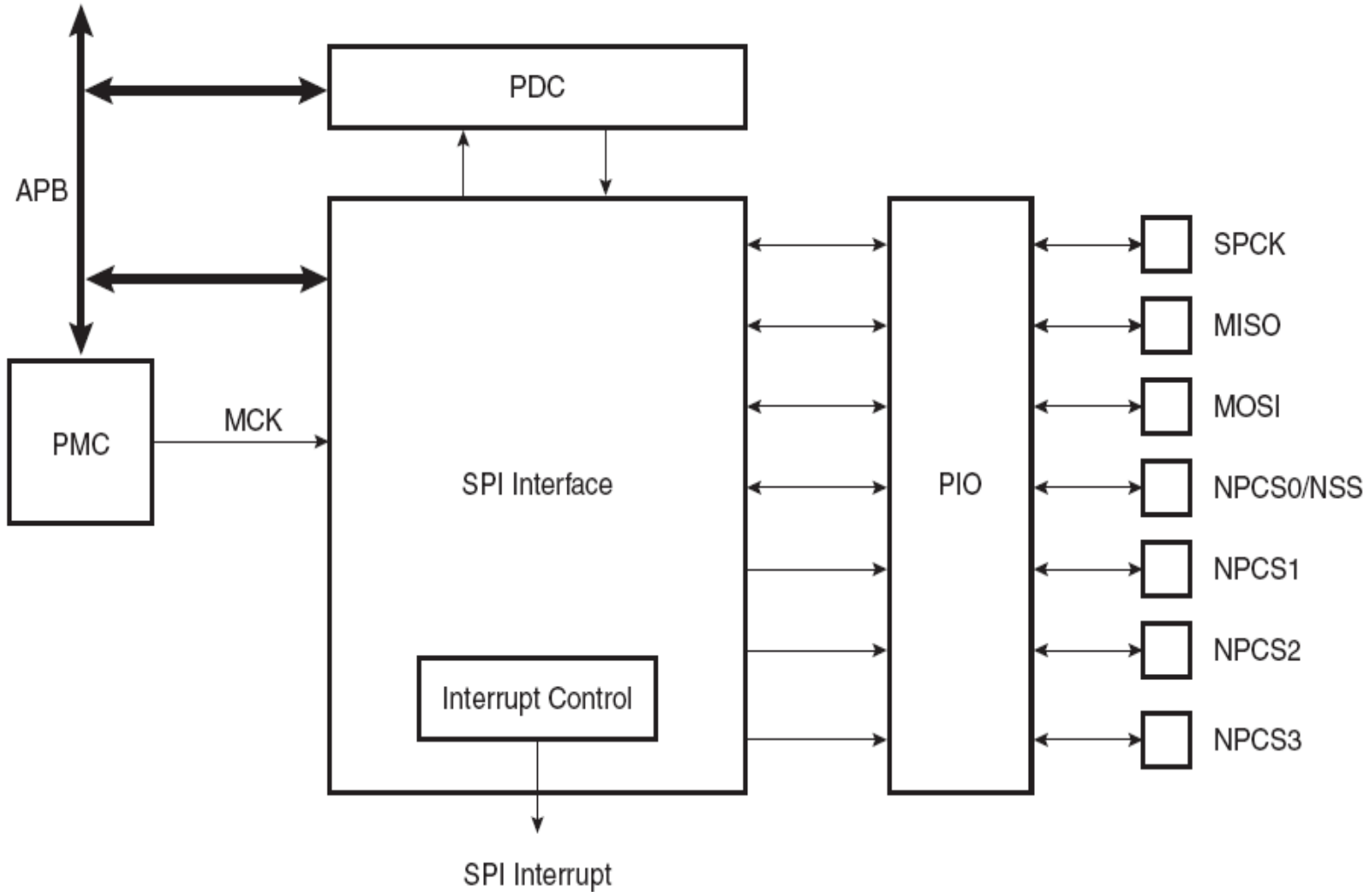
## SPI Module of ARM AT91SAM9263 processor (1)

### Features of SPI:

- Support for Master or Slave mode,
- Receiver and transmitter buffers,
- Data transfers: from 8 to 16 bits,
- Four programmable outputs for SPI devices selection (max. 15 devices),
- Programmable delay between transfers,
- Programmable clock phase and polarity.

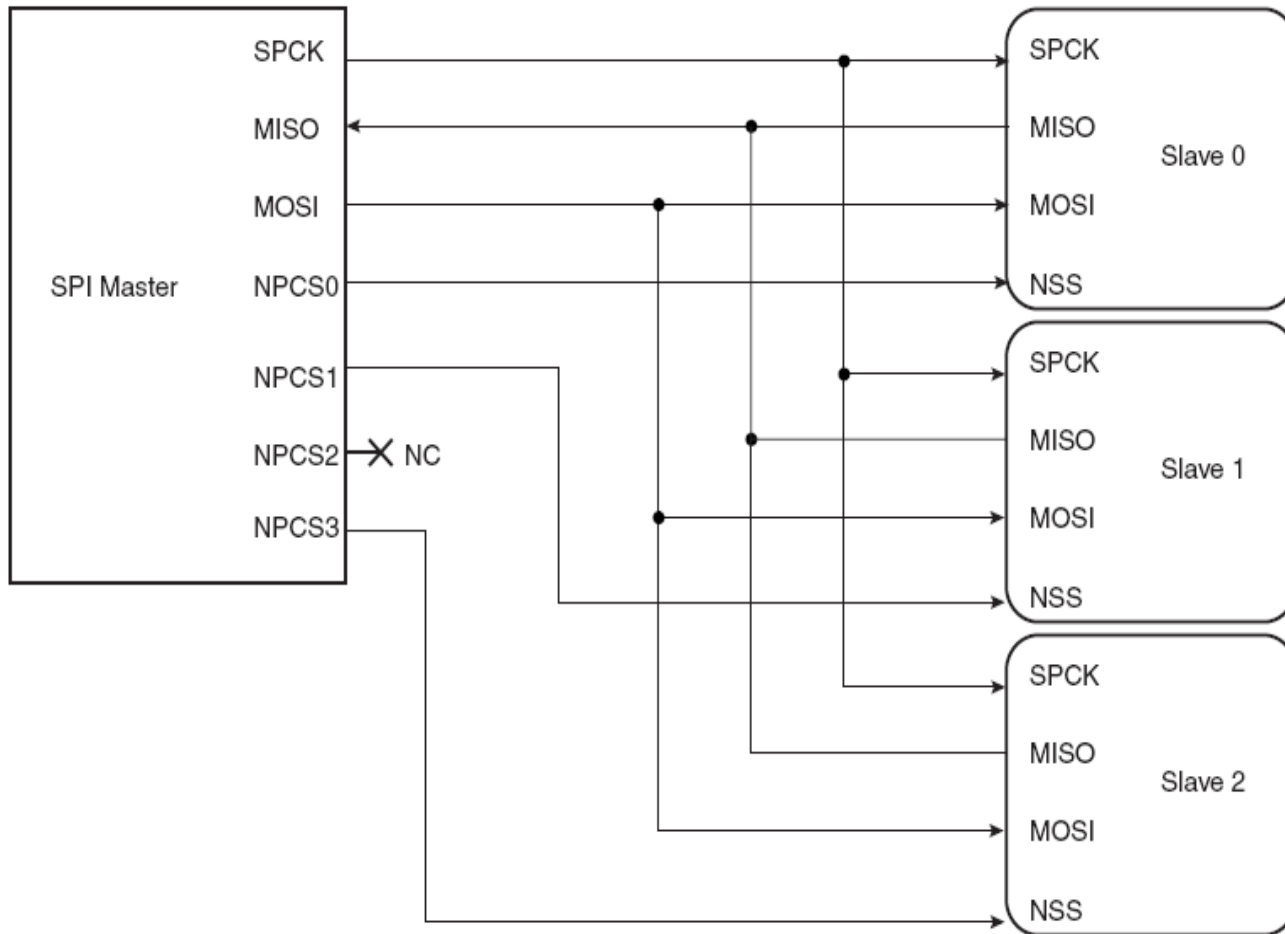


# SPI Module of ARM AT91SAM9263 processor (2)





# SPI Module of ARM AT91SAM9263 processor (3)



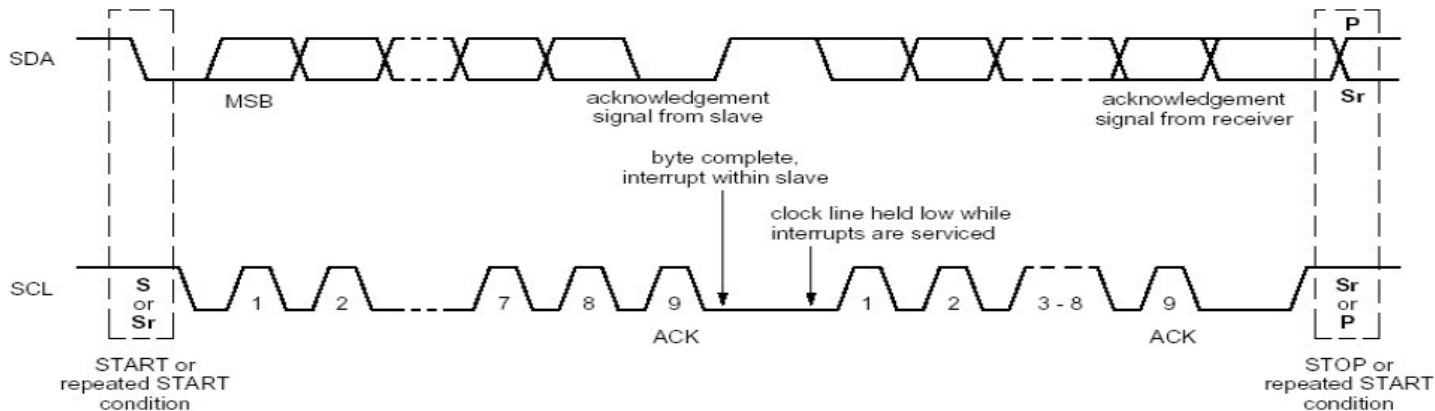


# I2C Bus Standard



# I2C Bus

- Standard developed by Philips company on early 80s,
- Two wire synchronous interface (SDA – data line, SCL – clock line),
- Bidirectional master-slave (multi-master) transfers, 8-bit frames,
- Transmission speed:
  - 100 kbps (standard mode),
  - 400 kbps (fast mode),
  - 3,4 Mbps (high-speed mode),
- 7-bit or 10-bits device address,
- Synchronisation allows to use devices with different speeds (autonegotiation),
- Number of devices connected to I2C bus limited by bus capacitance ( $C=400\text{ pF}$ ),
- Arbitration used for multi-master transmission.





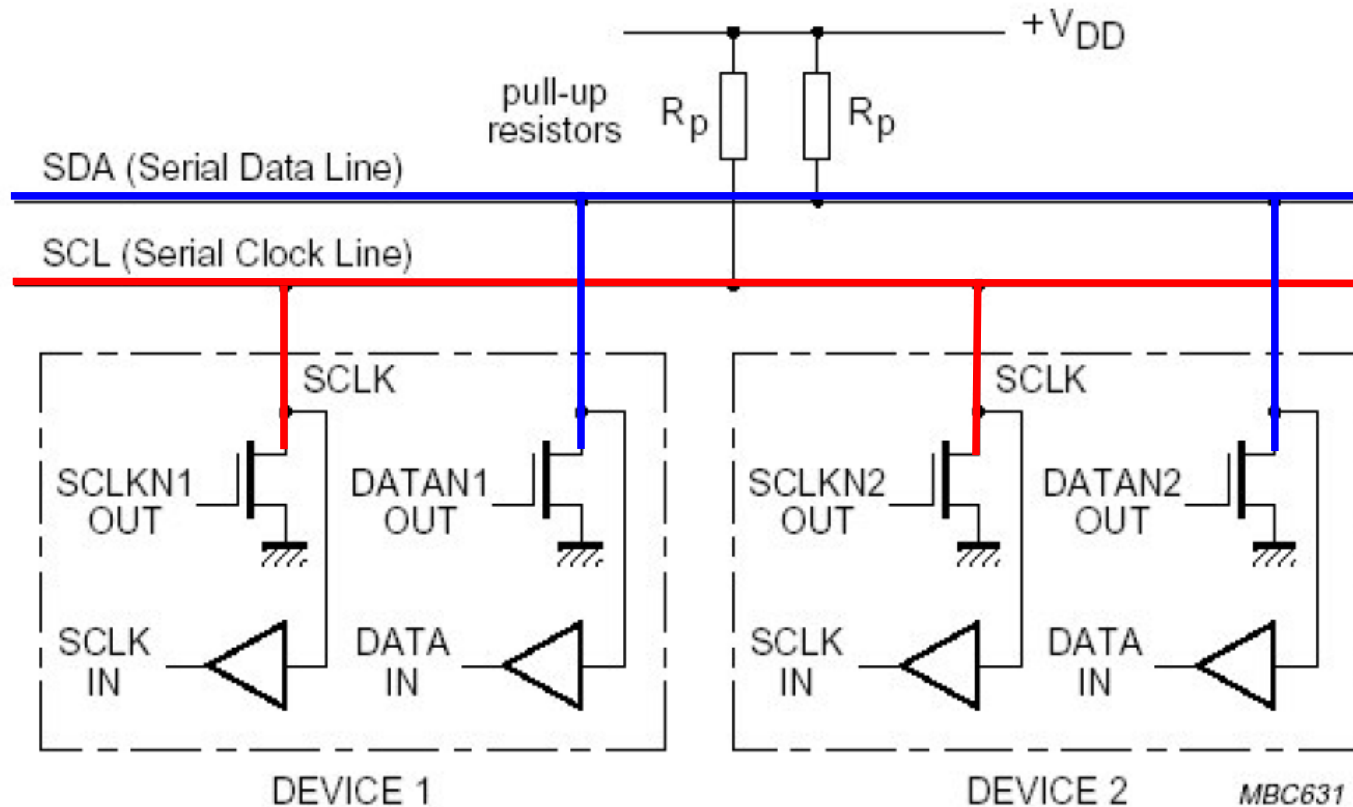
## Application of I2C Bus

I<sup>2</sup>C standard is applied to various digital and analogue devices:

- ★ PCF8563/8583 – clock, calendar, alarm, timer and NVRAM,
- ★ PCF8574 – 8-bit IO expander,
- ★ PCF8576, PCF8577 – LCD controllers,
- ★ PCF8582 - EEPROM memory, 256 bajts (1, 2, 4 kB, ... MB),
- ★ PCF8591 - 8-bit, 4-channels ADC/DAC converter.



# I2C Bus Signals



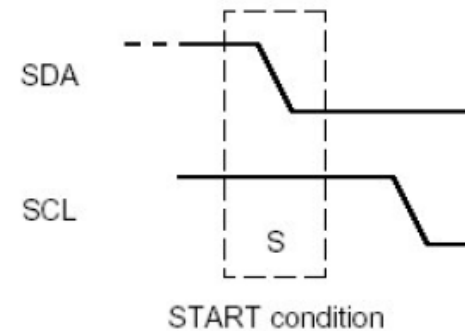
Master device – initialize transmission, generates clock signal

Slave device – analyse signals on bus, read address and data

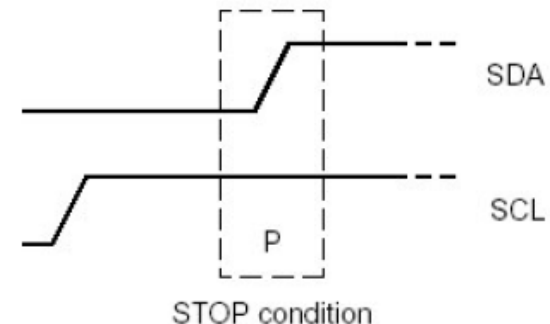


# Transmission Start and Stop

Transmission start – **START** signal (falling slope on SDA, change from “1” to “0”, during valid clock signal, SCL = “1”). Signal generated by Master.



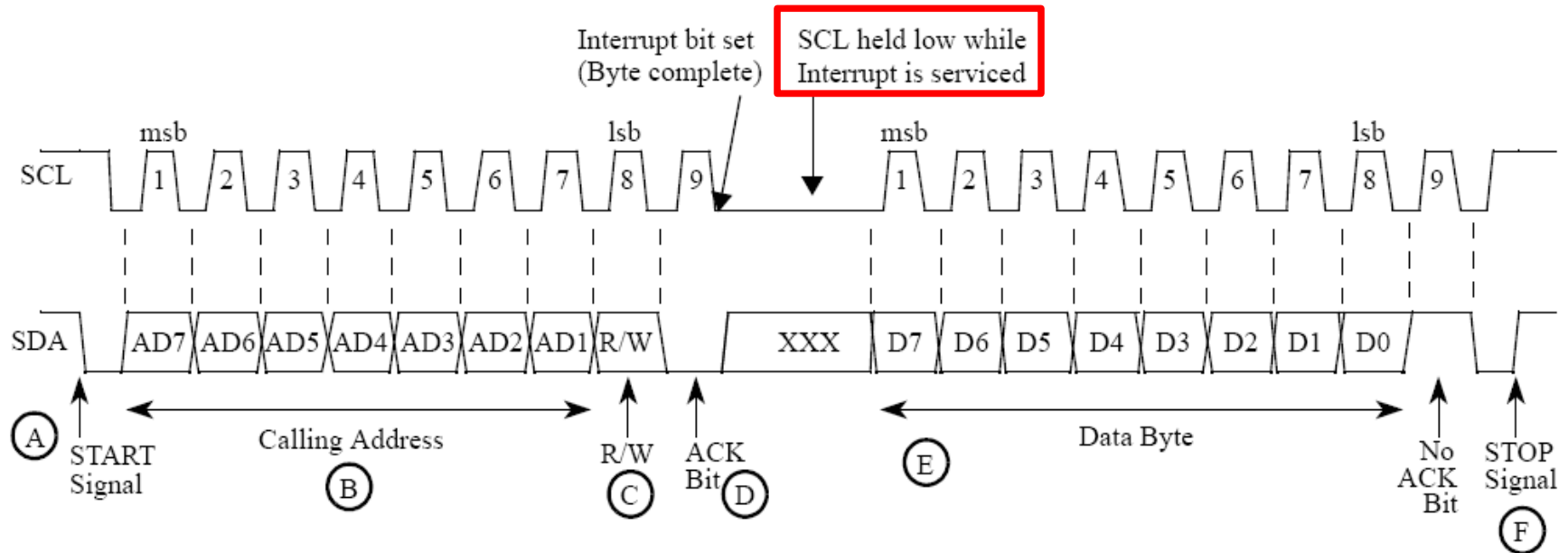
Transmission end – **STOP** (rising edge on SDA bus, change from “0” to “1” during valid clock signal, SCL = “1”). Signal generated by Master.







# I2C Protocol



A) Transmission initialised by Master, START condition.

B) Transmission of 8 bits (7 address bits, 1 R/W bit).

C) After 8 bit (clk signals) SDA bus is controlled by Slave (9th clk). Acknowledge is generated to confirm address receive ACK = '0' or not (ACK = "1").

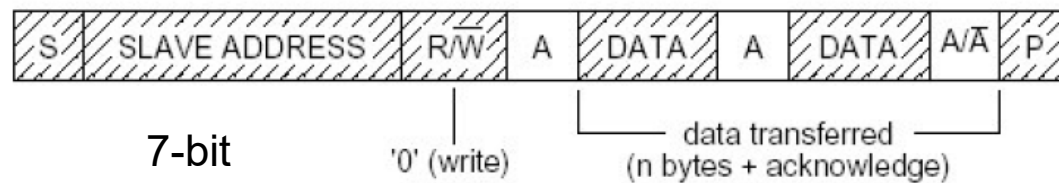
E) Data read or write phase – Master or Slave sends 8 data bits.

F) Transmission is finished when ACK signal is generated by data receiver (Master or Slave). Master generates Stop condition.



# I2C – Read or Write

Master write n-bytes of data  
master-transmitter

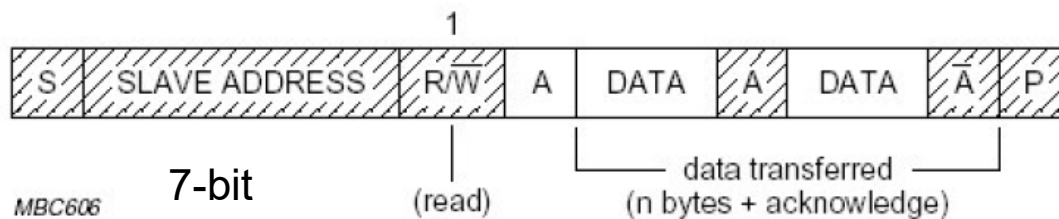


from master to slave

from slave to master

- A = acknowledge (SDA LOW)
- $\bar{A}$  = not acknowledge (SDA HIGH)
- S = START condition
- P = STOP condition

Master reads n-bytes of data  
master-receiver (since second byte)



MBC606



## Two-Wire Interface – standard compatible with I2C ?

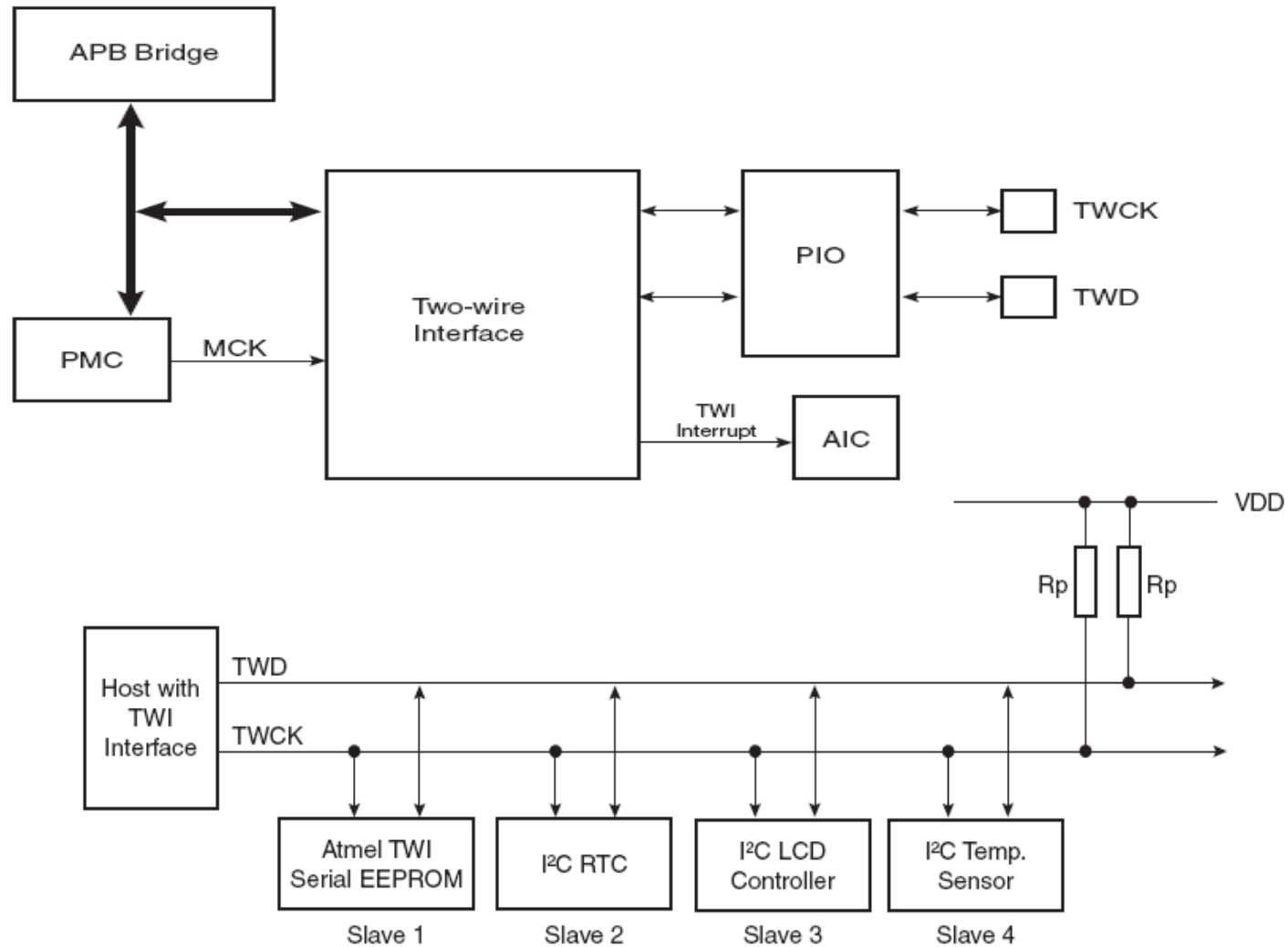
ARM processors are equipped with TWI interface compatible with developed by Philips I2C (I2C interface was patented by Philips).

### Features of TWI interface:

- ★ Compatible with I2C,
- ★ Master, Multimaster or Slave modes,
- ★ IO voltage equal to 3,3 V,
- ★ Maximum transmission speed: 400 kHz,
- ★ Transfers triggered with interrupts,
- ★ Automatically Slave mode activated when collision detected on I2C bus (Arbitration-lost interrupt),
- ★ Interrupt triggered when I2C slave address recognised,
- ★ Automatic bus busy recognition,
- ★ Support for 7 and 10-bits addresses.



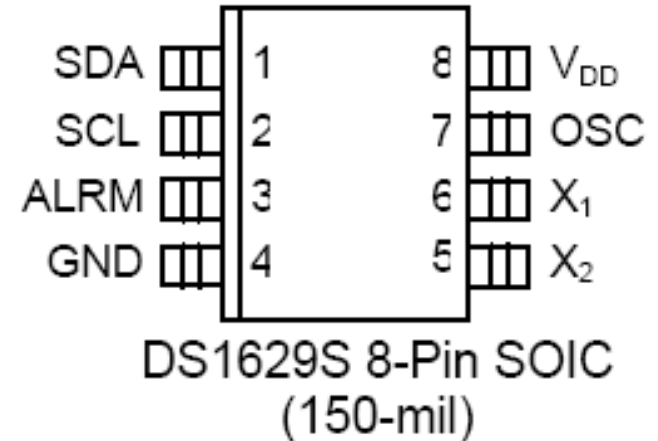
# Block diagram of TWI module





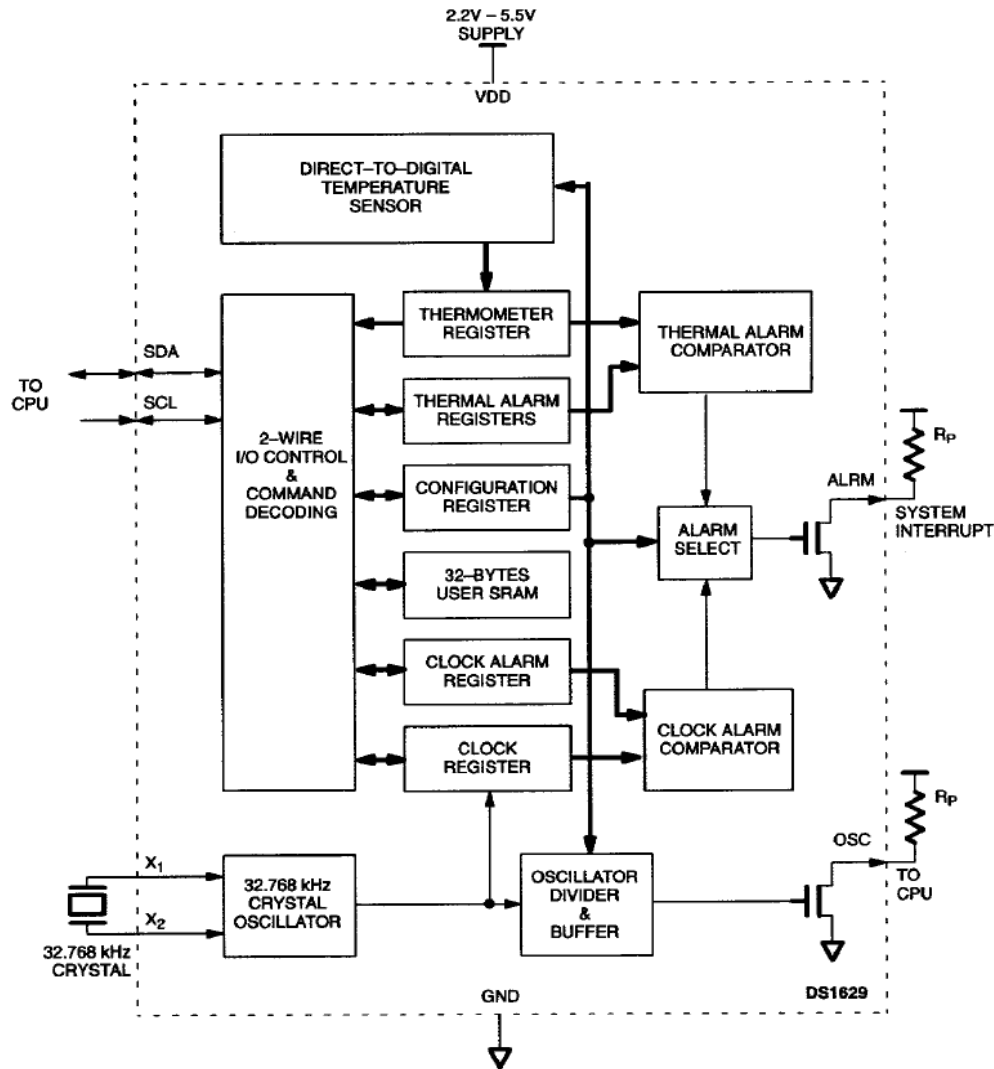
## Features of DS1629:

- ★ Real Time Clock,
- ★ Build-in thermometer -55 – 125 C,
- ★ Thermometer resolution: 9 bits,
- ★ Thermometer accuracy +/- 2 C,
- ★ Thermostat mode,
- ★ 32 bytes of SRAM,
- ★ Power Supply 2,2 – 5,5 V,
- ★ Interface compatible with I2C (400 kHz).



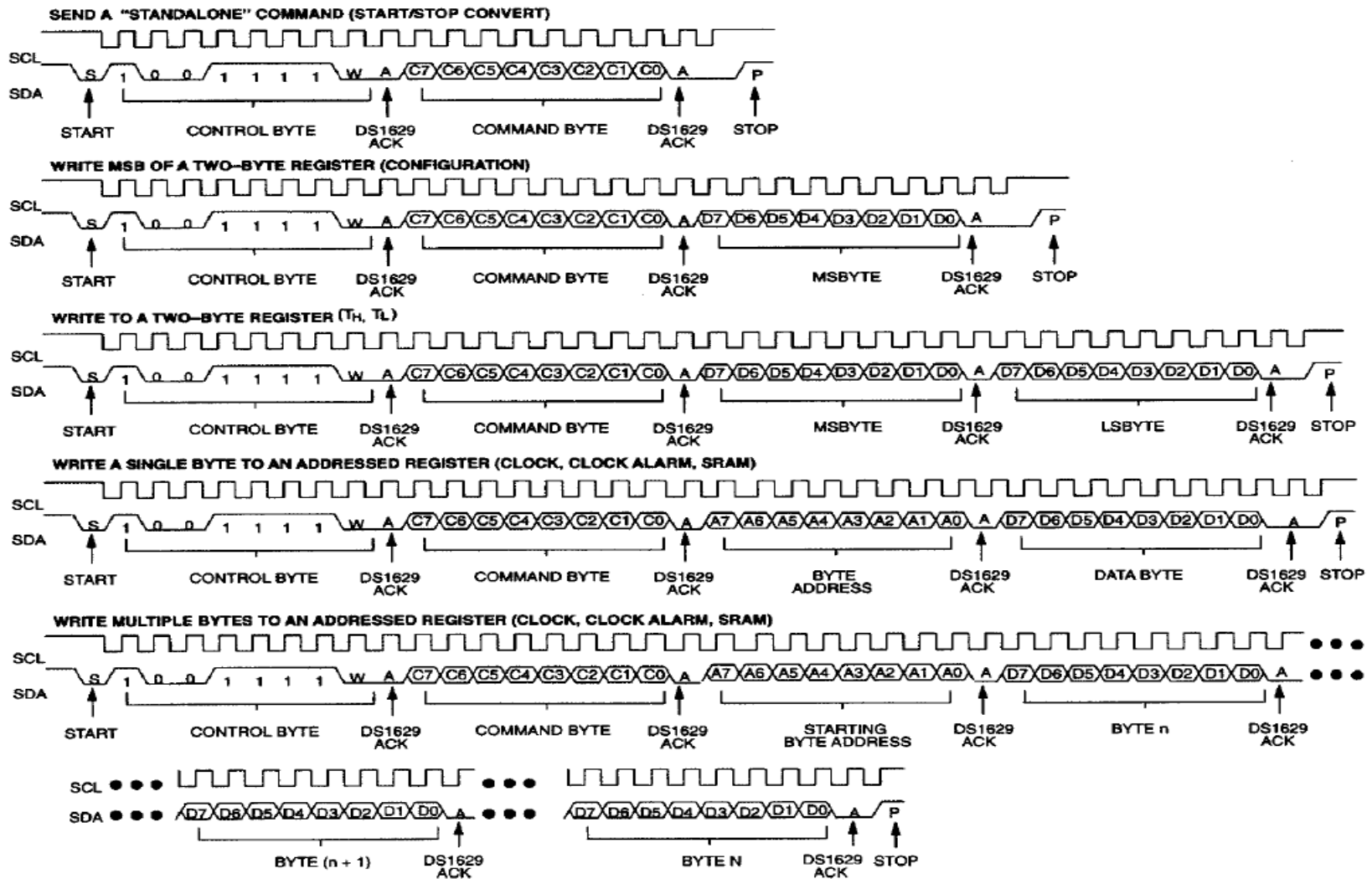


# Real Time Clock





# Real Time Clock – I2C Transmission





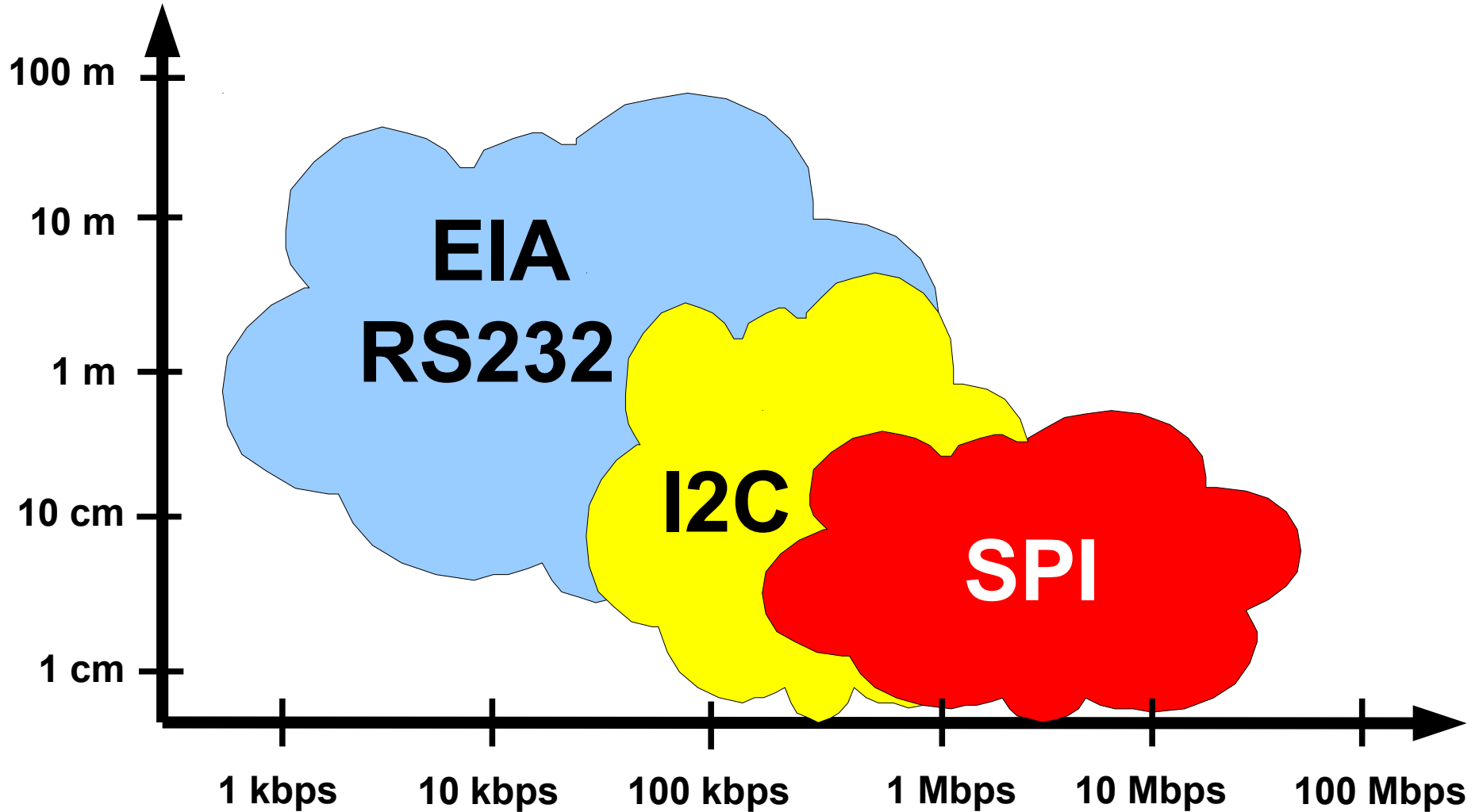
## Exam Dates

- Exam #1 – 22.06.2022 8.15-12.15
- Exam #2 – 29.06.2022 8.15-12.15
- Exam #3 – 14.09.2022 8.15-12.15





# Serial Interfaces - comparison

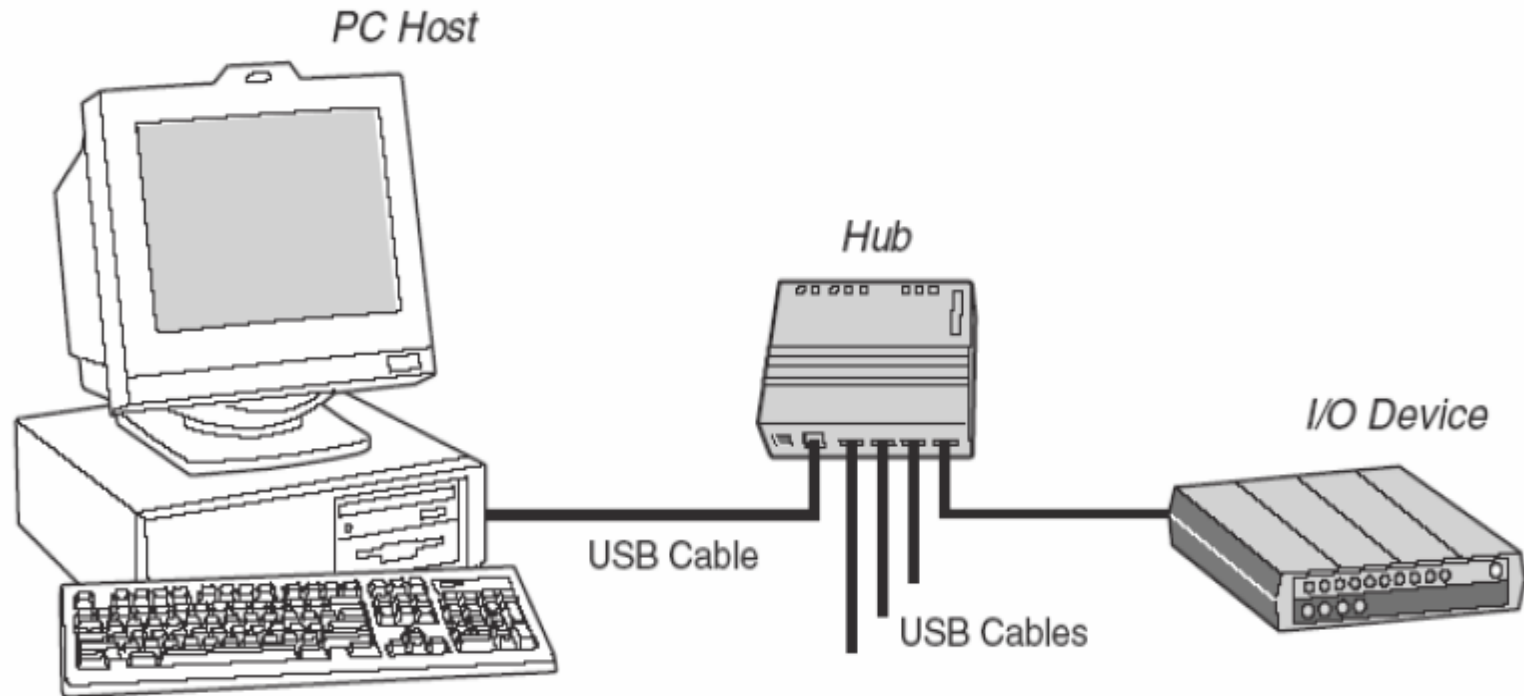




# Universal Serial Bus



# Universal Serial Bus





## Features of USB

- ★ Asynchronous, serial, differential data transmission,
- ★ Automatic recognition of connected/disconnected devices, automatic configuration,
- ★ Single, standardized connector,
- ★ Up to 127 devices on single bus,
- ★ Automatic detection and errors correction,
- ★ Transmission speed:
  - ➔ LOW 1.5 Mb/s, specification USB >1.1,
  - ➔ FULL 12 Mb/s, specification USB >1.1,
  - ➔ HIGH 480 Mb/s, specification USB 2.0,
  - ➔ **Specification USB 3.0 => 5 Gb/s.**

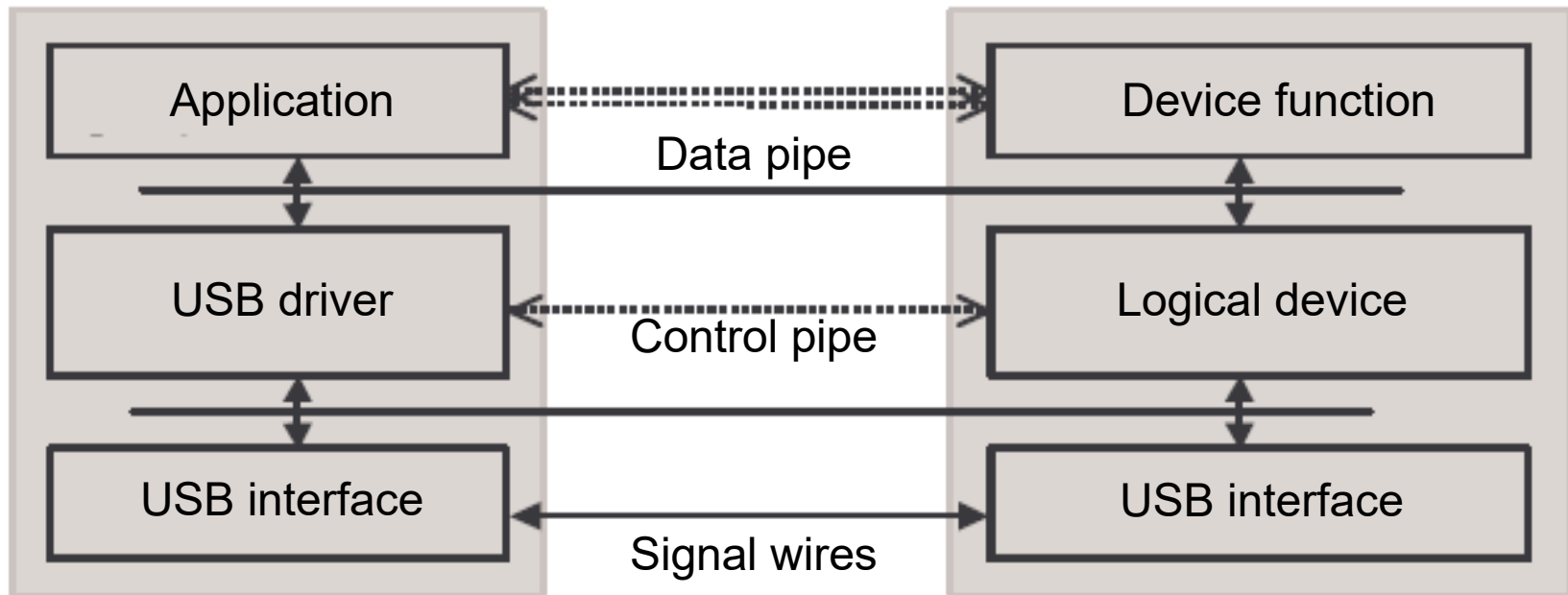
Transmission speed	Exemplary application	Throughput
<b>Low</b> 10 – 100 kbps	Keyboard, mouse, manipulators, IO devices, HID	Low <1.5 Mbps
<b>Medium</b> 500 kbps – 10 Mbps	Audio devices, data transmission	Full <12 Mbps
<b>Fast</b> 25 – 400 Mbps	Video device, mass storage device	High <480 Mbps



# Data layers of USB

## Host device

## USB



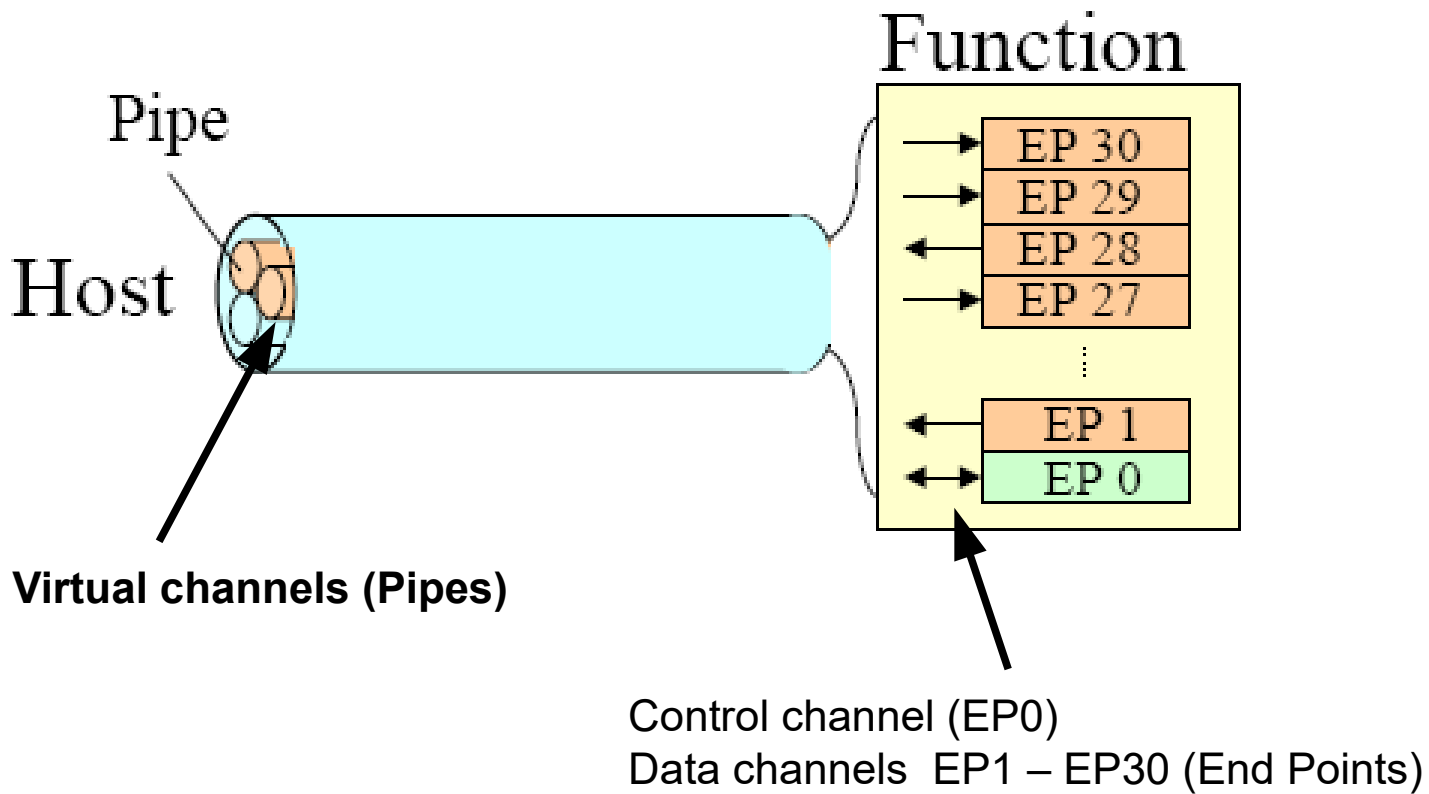
**USB is designed as a star bus.**

USB model is composed of three layers:

- ◆ Physical layer,
- ◆ Logical layer,
- ◆ Functional layer.

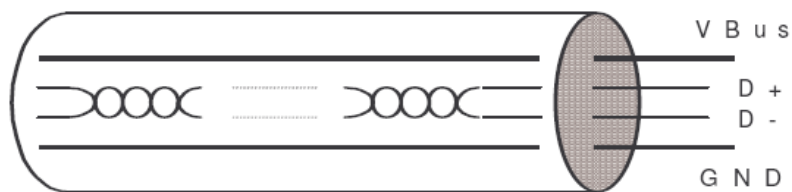


# Data flow in USB

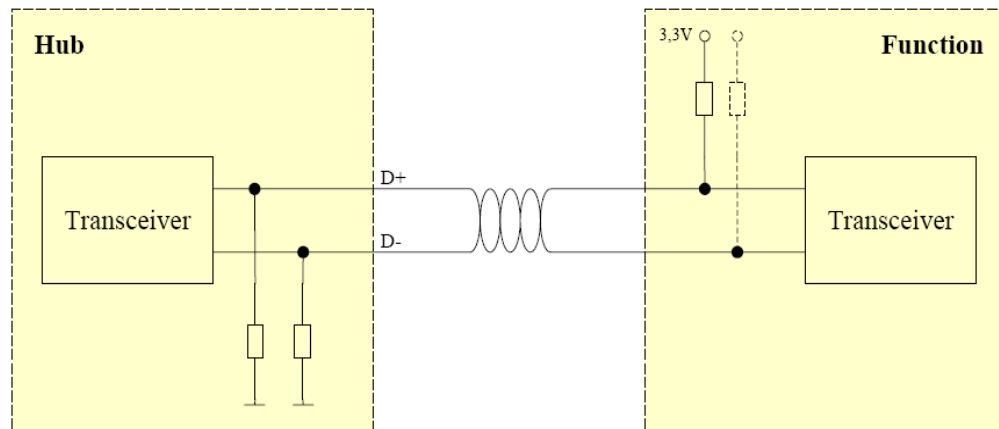




# Physical Layer



Differential transmission, half-duplex. Included power supply bus 5 V/500 mA



Mini USB

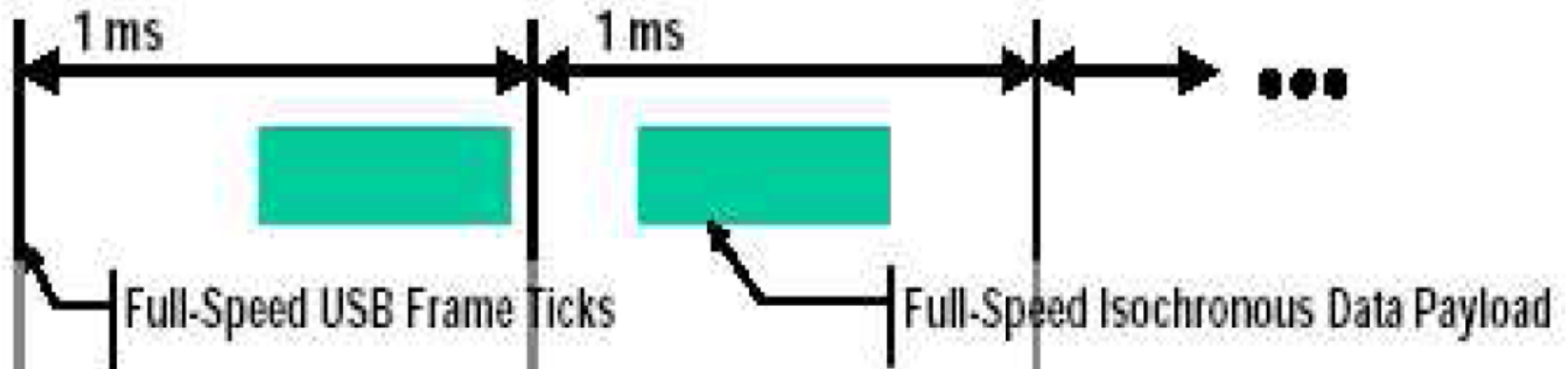


USB "A" and "B" type

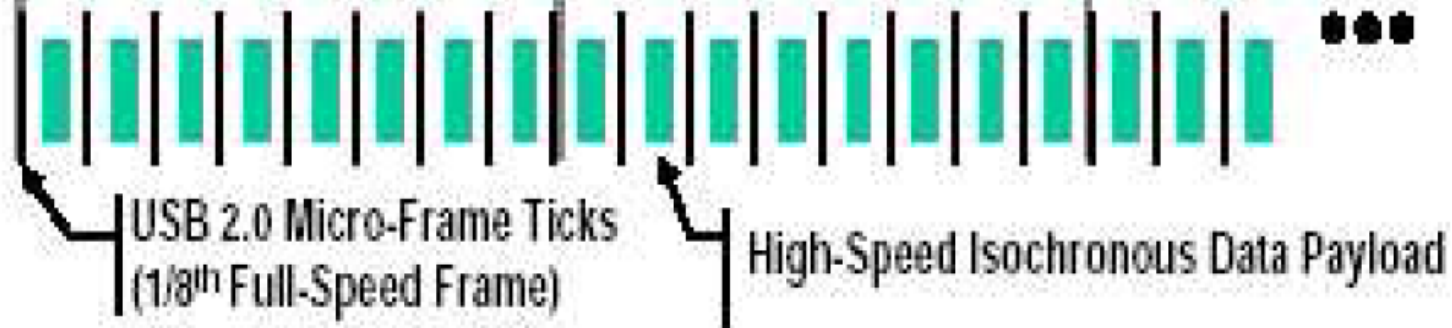


# USB Frame

## Full / Low-Speed Frame Size (1 ms)



## High-Speed Micro-Frames (125 us)





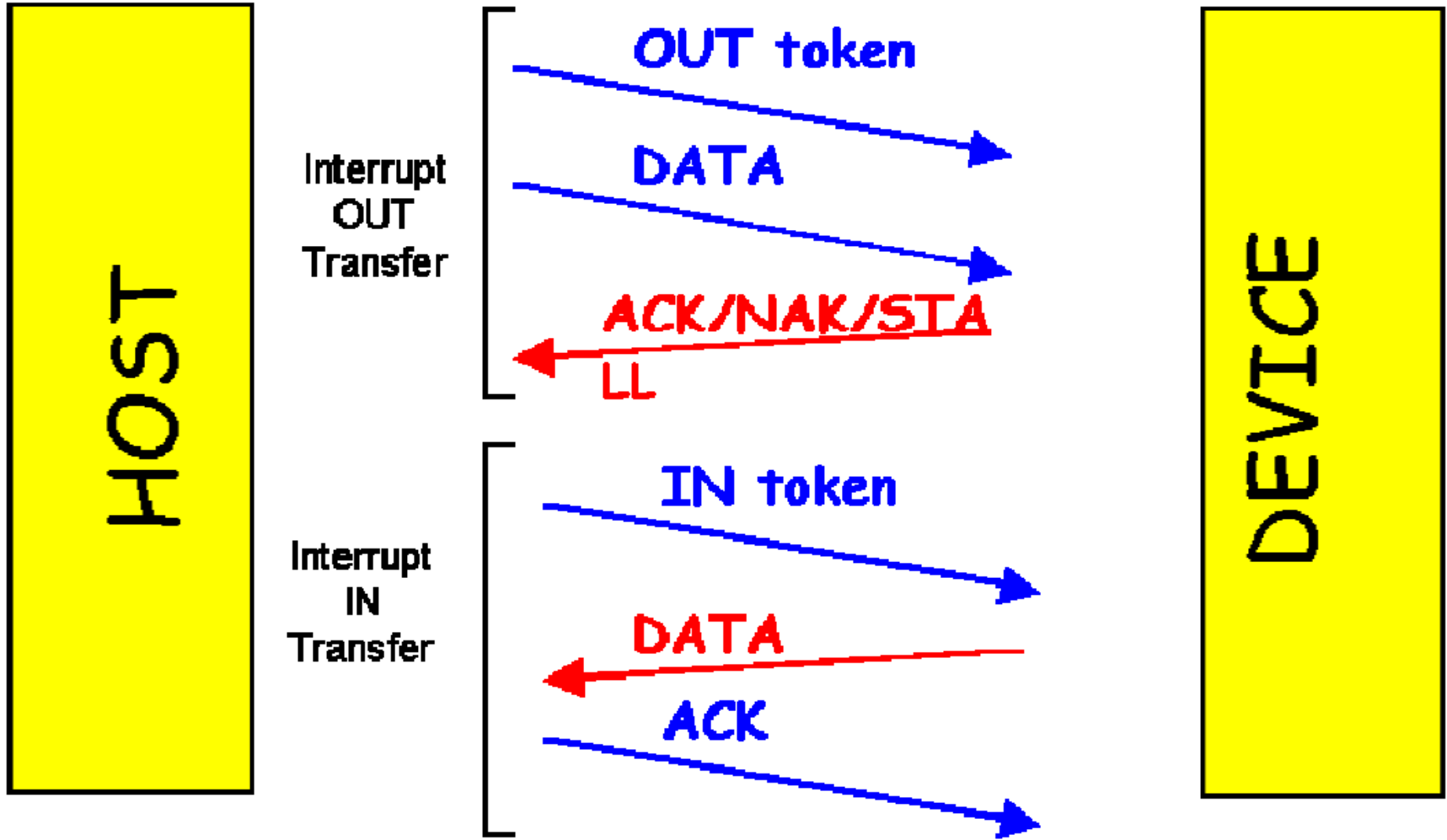


# Available Transfer Modes

Type	Important attributes	Max size LS	Max size FS	Max size HS	Examples
Interrupt	Quality + time	8	64	3072	Mouse, keyboard
Bulk	Quality	-	64	512	Printer, scanner
Isochronous	time	-	1023	3072	Audio, video
Control	Quality + time	8	64	64	System control

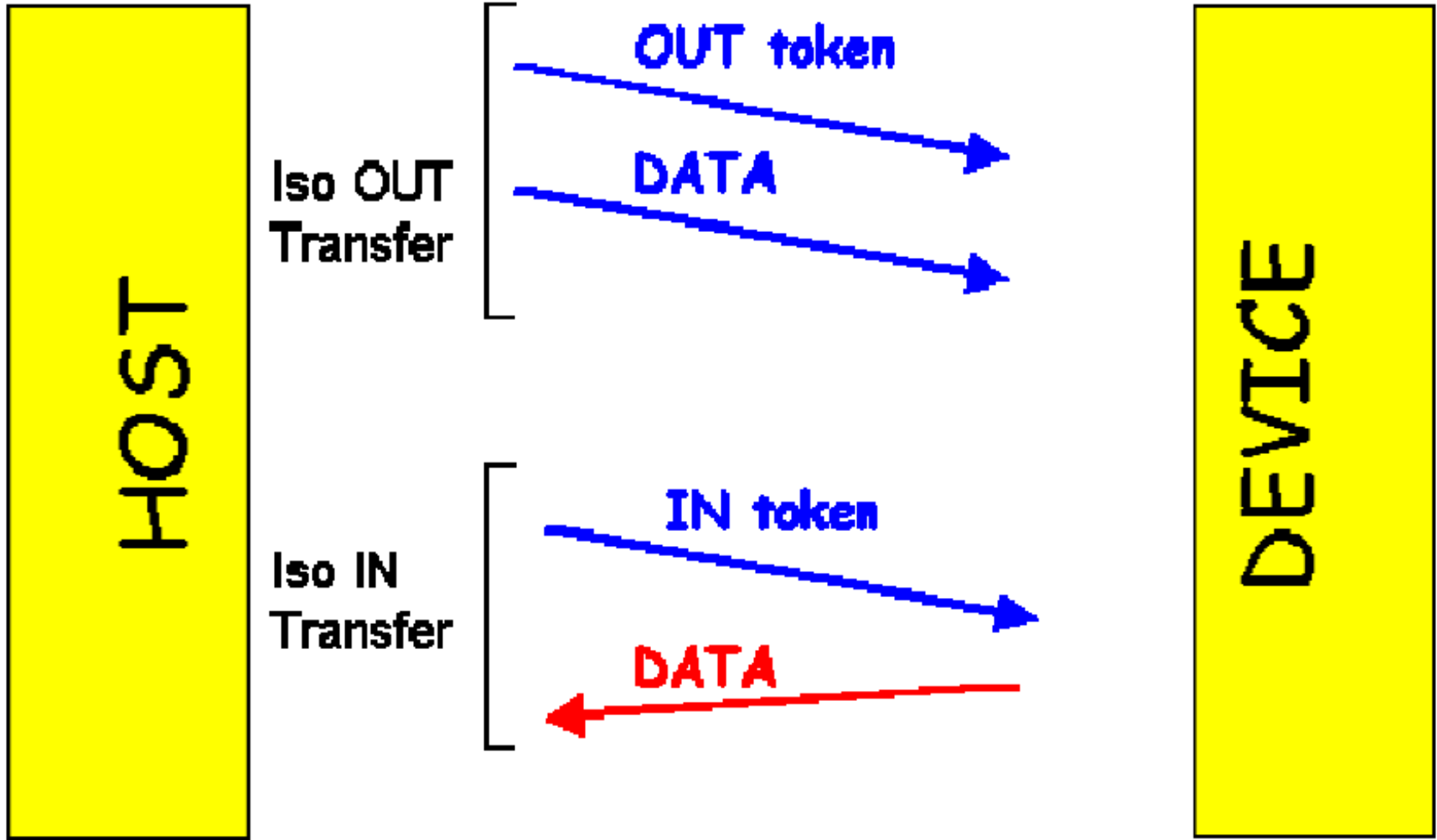


# Bulk and Interrupt Transfer



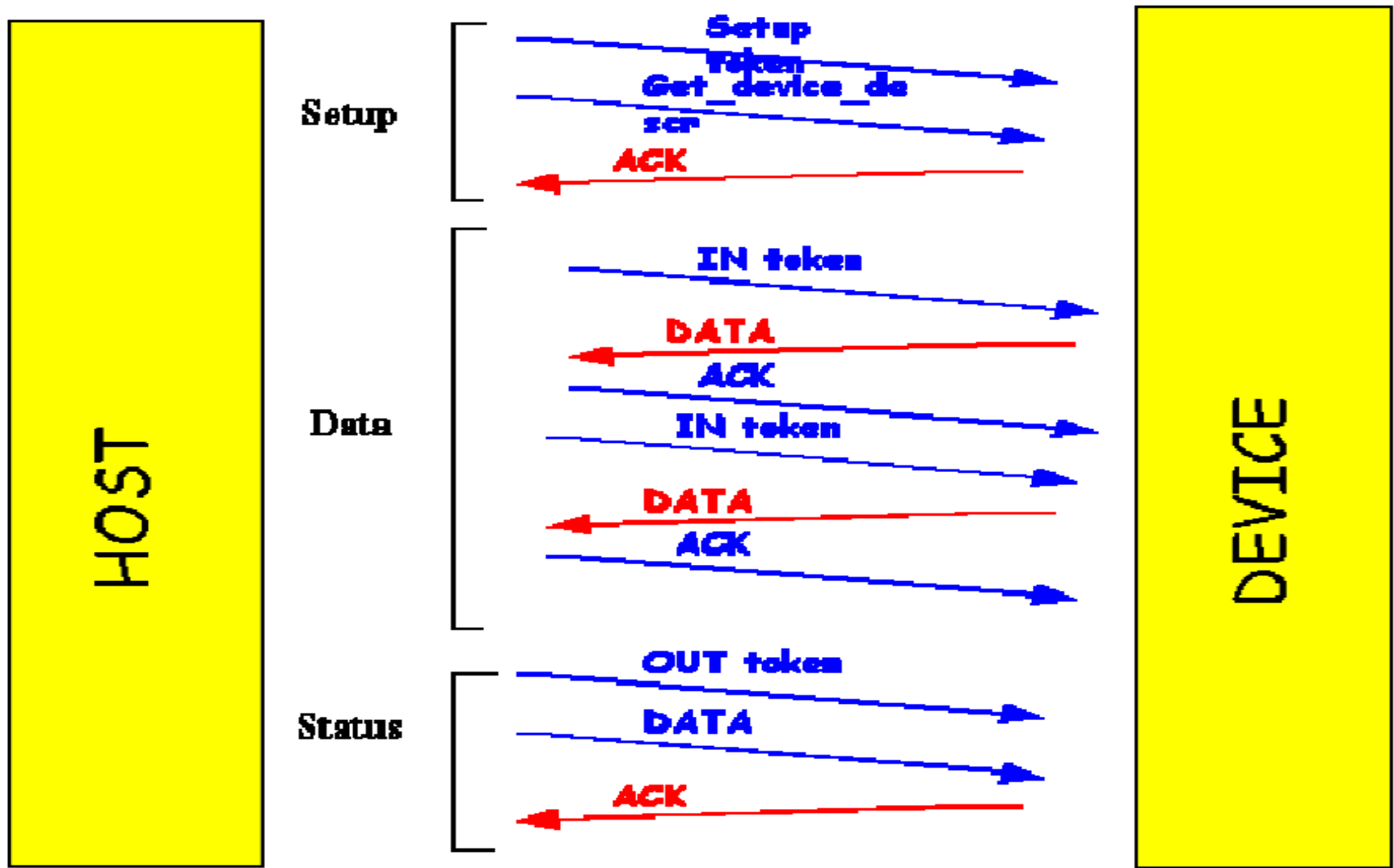


# Isochronous Transfer





# Control Transfer





## Configuration

**Enumeration** – configuration of devices connected to USB bus after connection to disconnection of devices from bus. Enumeration is performed by Master node (address 0). Master assigned individual address to devices connected to USB and configures basic parameters:

- Device address in USB area,
- Transfer mode,
- Transfer direction (read, write, read-write),
- Size of data packet,
- Transmission speed,
- Allocates buffers for virtual channels,
- Allocated power for connected devices.



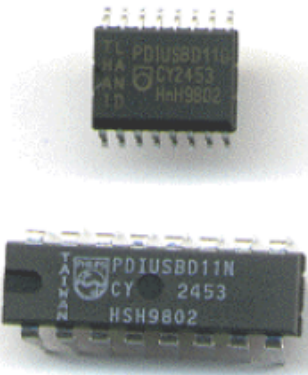
# USB Hubs



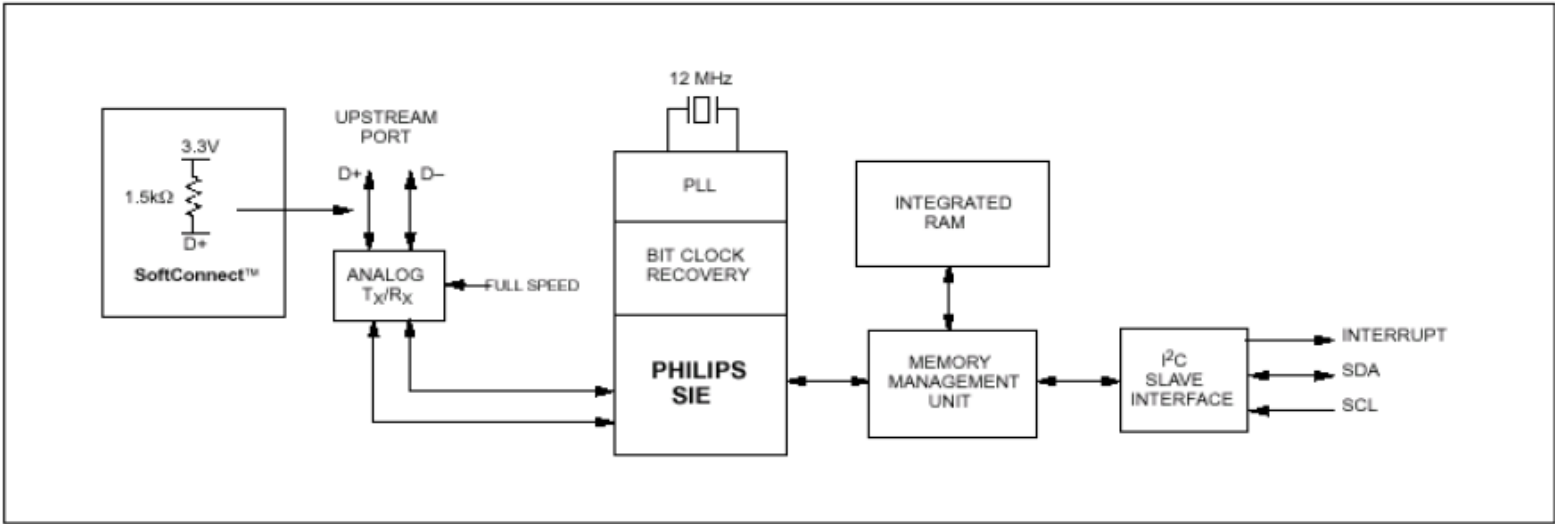


# USB to I2C converter

## Philips PDIUSB011 (USB to I2C)

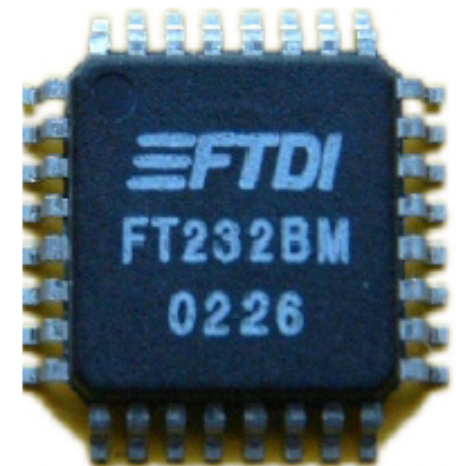
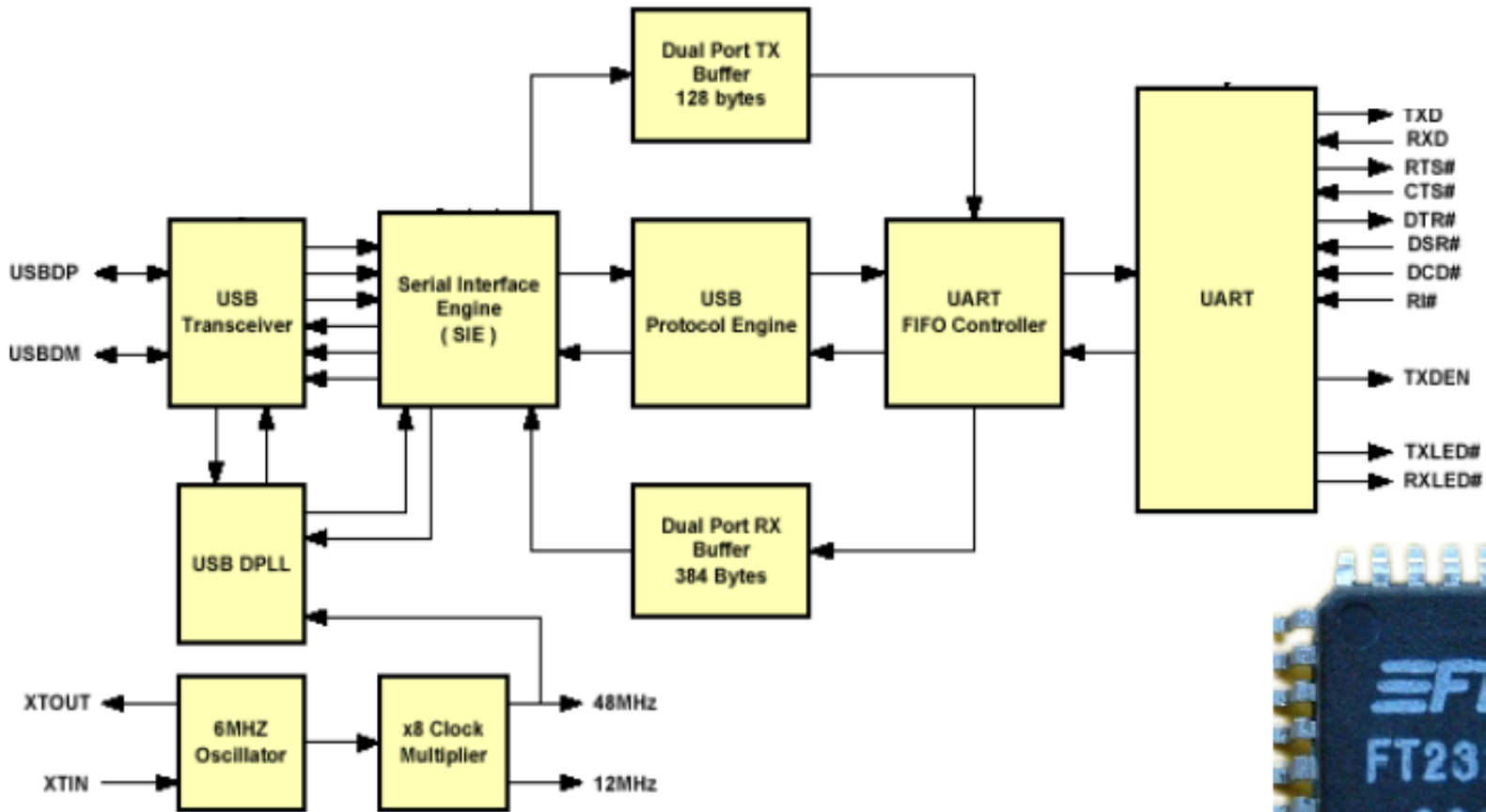


### BLOCK DIAGRAM





# Universal converter



- RS 232, parallel, SPI, CAN to USB





# USB and ColdFire processors

## Low\Full speed:

MCF 527X (72-75)	66 – 166 MHz
MCF 5221X (72-75)	80 MHz
MCF 5222X (72-75)	80 MHz
MCF 527X (72-73)	240 MHz

68HCS08JW32            8 MHz

## High Speed:

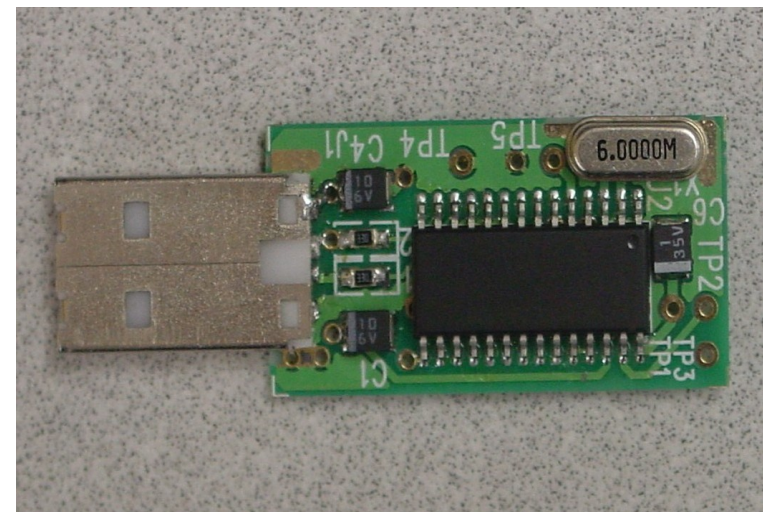
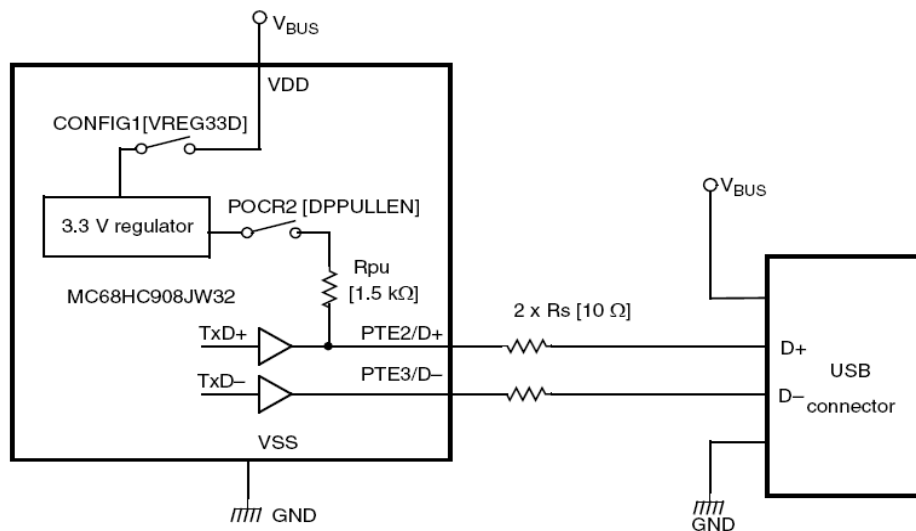
MCF 547X (72-75)	200 –266 MHz
MCF 548X (82-85)	166 – 200 MHz
MCF 537X (77-79)	240 Mhz
MCF 5253	140 MHz



# Motorola 68HC908JW32

Features of USB module of HC908:

- Interface compatible with USB 2.0 full speed,
- 12 Mbps data rate,
- Build-in 3.3 V regulator,
- Endpoint 0 with 8-bytes Tx/Rx buffers
- 64 bytes buffer for endpoints 1-4.

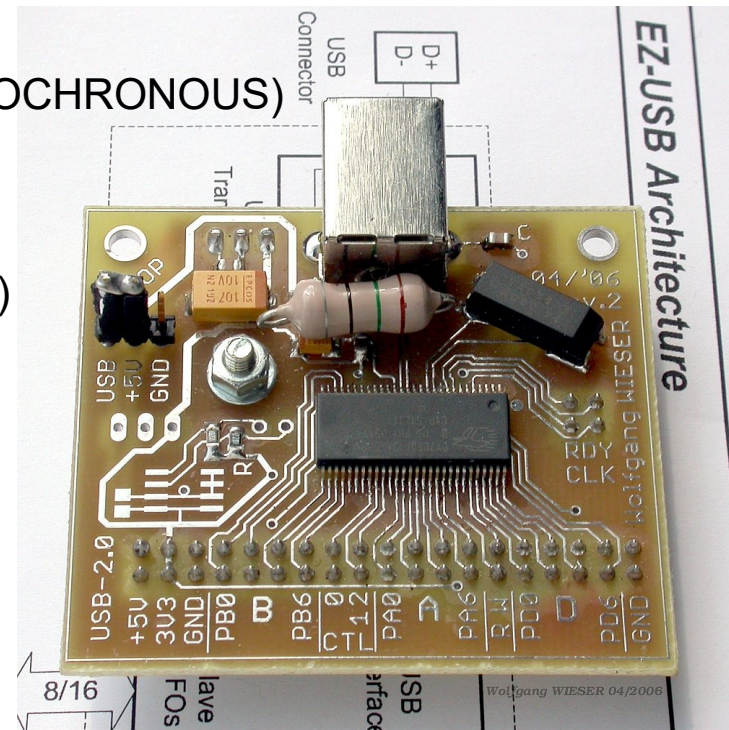




# Cypress Processor with USB CY7C68013A

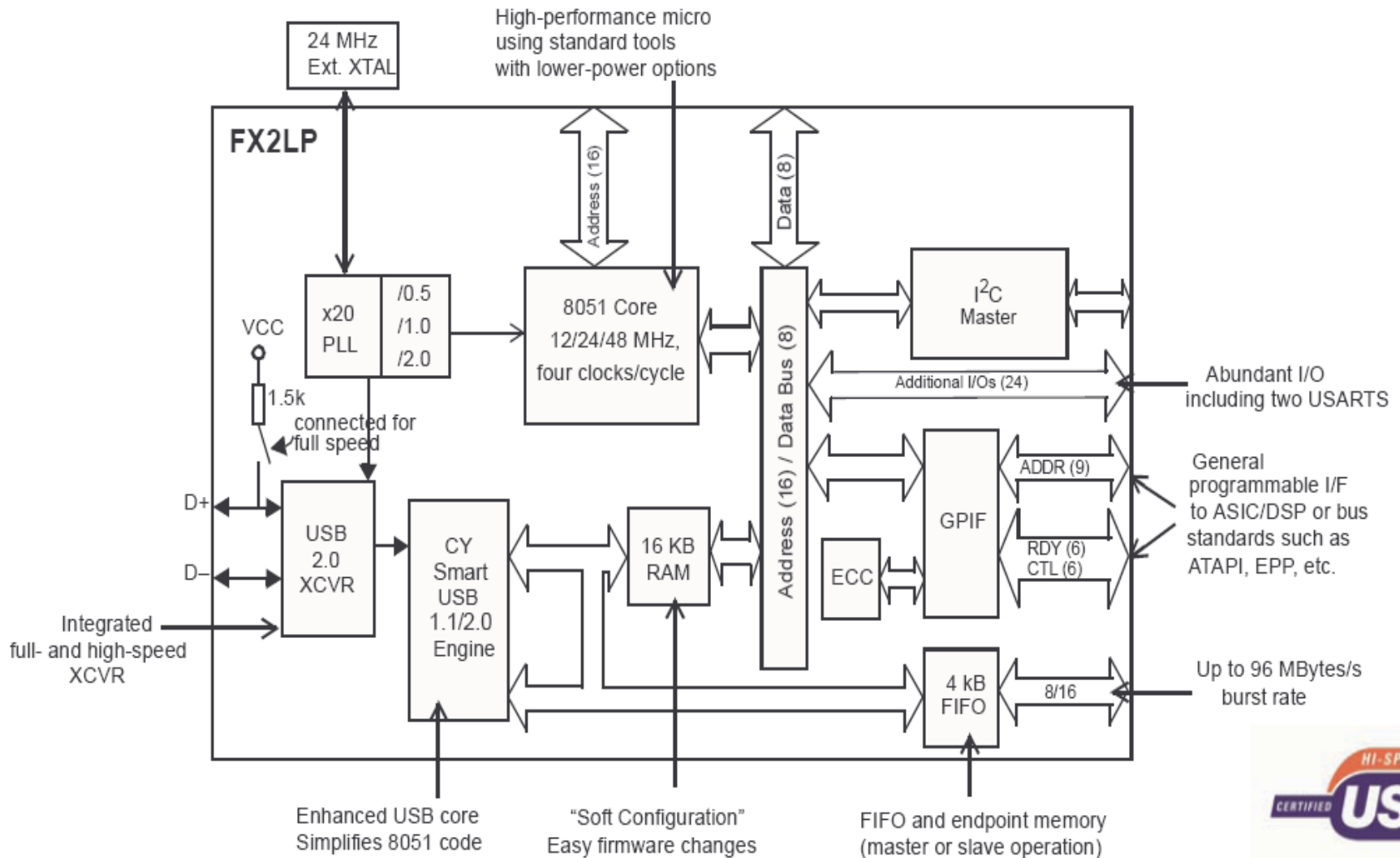
## Features of CY7C68013:

- ★ Compatible with USB 2.0–USB-IF high speed,
- ★ Based on **8051 core**,
- ★ Integrated 16 kB RAM (SRAM)
  - ➔ Memory can be loaded from USB,
  - ➔ Memory can be loaded from external EEPROM.
- ★ Four programmable endpoints (BULK/INTERRUPT/ISOCHRONOUS)
- ★ Additional 64 bytes endpoint (BULK/INTERRUPT),
- ★ Parallel 8- or 16-bits external interface,
- ★ DMA channel, GPIF (General Programmable Interface)





# Cypress CY7C68013A processor





USB

3.0

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SuperSpeed USB 3.0 Specification  
Revolutionizes An Established Standard



## USB 3.0

- Serial high speed, full-duplex interface
- Data transmission speed: 5 Gb/s (10 more than USB 2.0)
- Compatible with USB 2.0 (drivers and connector), however significantly differ from USB 2.0
- Two channels for full-duplex, power supply
- Intelligent power supply control, lower power consumption
- Physical and data layers similar to PCI express 2.0



# Physical Layer of USB 3.0

