```
" 4-bit licznik binarny rewersyjny z blokada liczenia, synchronicznym i asynchronicznym kasowaniem,
" sygnalizacja przepelnienia i wyjsciami do 7-segmentowego wyswietlacza LED ze wspolna anoda:
"
"      f
"     ---
"  a | g | e
"     ---
"  b | c | d
"     ---
"
"  sygnal  typ  funkcja
"  AR      wej  asynchroniczne kasowanie (aktywne 1)
"  SR      wej  synchroniczne kasowanie (aktywne 1)
"  CLK     wej  sygnal zegarowy
"  UP      wej  kierunek liczenia: 1 - w gore, 0 - w dol
"  EN      wej  wlaczanie wyswietlacza LED: 1 - wlaczony, 0 - wygaszony
"  Q3-Q0   wyj  stan licznika
"  OV      wyj  sygnalizacja przepelnienia licznika (aktywna 1)
"  a-g     wyj  sterowanie wyswietlaniem segmentow a-g (aktywne 0)

MODULE counter

TITLE '4-bitowy licznik binarny z dekoderem 7-segmentowym'

DECLARATIONS
       AR, SR, CLK, CE, UP, EN PIN;
       Q3..Q0, OV PIN ISTYPE 'reg,buffer';
       a, b, c, d, e, f, g PIN ISTYPE 'com';

       wa, wb, wc, wd, we, wf, wg NODE ISTYPE 'com';

       X, C, OFF, ON = .x., .c., 1, 0;
       CNT = [Q3..Q0];
       LED = [a, b, c, d, e, f, g];
       W = [wa, wb, wc, wd, we, wf, wg];

TRUTH_TABLE
       (CNT -> [ wa,  wb,  wc,  wd,  we,  wf,  wg])
        ^h0 -> [ ON,  ON,  ON,  ON,  ON,  ON, OFF];
        ^h1 -> [OFF, OFF, OFF,  ON, OFF, OFF, OFF];
        ^h2 -> [OFF,  ON,  ON, OFF,  ON,  ON,  ON];
        ^h3 -> [OFF, OFF,  ON,  ON,  ON,  ON,  ON];
        ^h4 -> [ ON, OFF, OFF,  ON,  ON, OFF,  ON];
        ^h5 -> [ ON, OFF,  ON,  ON, OFF,  ON,  ON];
        ^h6 -> [ ON,  ON,  ON,  ON, OFF,  ON,  ON];
        ^h7 -> [OFF, OFF, OFF,  ON,  ON,  ON, OFF];
        ^h8 -> [ ON,  ON,  ON,  ON,  ON,  ON,  ON];
        ^h9 -> [ ON, OFF,  ON,  ON,  ON,  ON,  ON];
        ^hA -> [ ON,  ON, OFF,  ON,  ON,  ON,  ON];
        ^hB -> [ ON,  ON,  ON,  ON, OFF, OFF,  ON];
        ^hC -> [ ON,  ON,  ON, OFF, OFF,  ON, OFF];
        ^hD -> [OFF,  ON,  ON,  ON,  ON, OFF,  ON];
        ^hE -> [ ON,  ON,  ON, OFF, OFF,  ON,  ON];
        ^hF -> [ ON,  ON, OFF, OFF, OFF,  ON,  ON];

EQUATIONS
       LED = W # !EN;
       [CNT, OV].CLK = CLK;
       [CNT, OV].AR = AR;

       WHEN SR THEN
              CNT := 0;
       ELSE WHEN !CE THEN
              CNT := CNT;
       ELSE WHEN UP THEN
              CNT := CNT + 1;
       ELSE
              CNT := CNT - 1;

       OV := !SR & CE & (UP & (CNT == ^hF) # !UP & (CNT == ^h0));
```

```
TEST_VECTORS
       ([AR, SR, CLK, CE, UP, EN] -> [CNT, OV,    a,    b,    c,    d,    e,    f,    g])
        [ 1,  X,   0,  X,  X,  1] -> [^h0,  0,  ON,   ON,   ON,   ON,   ON,   ON,  OFF];
        [ 0,  0,   C,  1,  1,  1] -> [^h1,  0, OFF,  OFF,  OFF,   ON,  OFF,  OFF,  OFF];
        [ 0,  0,   C,  1,  1,  1] -> [^h2,  0, OFF,   ON,   ON,  OFF,   ON,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h3,  0, OFF,  OFF,   ON,   ON,   ON,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h4,  0,  ON,  OFF,  OFF,   ON,   ON,  OFF,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h5,  0,  ON,  OFF,   ON,   ON,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h6,  0,  ON,   ON,   ON,   ON,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h7,  0, OFF,  OFF,  OFF,   ON,   ON,   ON,  OFF];
        [ 0,  0,   C,  1,  1,  1] -> [^h8,  0,  ON,   ON,   ON,   ON,   ON,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h9,  0,  ON,  OFF,   ON,   ON,   ON,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hA,  0,  ON,   ON,  OFF,   ON,   ON,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hB,  0,  ON,   ON,   ON,   ON,  OFF,  OFF,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hC,  0,  ON,   ON,   ON,  OFF,  OFF,   ON,  OFF];
        [ 0,  0,   C,  1,  1,  1] -> [^hD,  0, OFF,   ON,   ON,   ON,   ON,  OFF,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hE,  0,  ON,   ON,   ON,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hF,  0,  ON,   ON,  OFF,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h0,  1,  ON,   ON,   ON,   ON,   ON,   ON,  OFF];
        [ 0,  0,   C,  1,  1,  1] -> [^h1,  0, OFF,  OFF,  OFF,   ON,  OFF,  OFF,  OFF];
        [ 0,  0,   C,  1,  0,  1] -> [^h0,  0,  ON,   ON,   ON,   ON,   ON,   ON,  OFF];
        [ 0,  0,   C,  1,  0,  1] -> [^hF,  1,  ON,   ON,  OFF,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  0,  1] -> [^hE,  0,  ON,   ON,   ON,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  0,  1,  1] -> [^hE,  0,  ON,   ON,   ON,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  0,  0,  1] -> [^hE,  0,  ON,   ON,   ON,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^hF,  0,  ON,   ON,  OFF,  OFF,  OFF,   ON,   ON];
        [ 0,  0,   C,  1,  1,  1] -> [^h0,  1,  ON,   ON,   ON,   ON,   ON,   ON,  OFF];
        [ 0,  0,   C,  1,  0,  1] -> [^hF,  1,  ON,   ON,  OFF,  OFF,  OFF,   ON,   ON];
        [ 0,  1,   C,  X,  X,  0] -> [^h0,  0, OFF,  OFF,  OFF,  OFF,  OFF,  OFF,  OFF];

END
```