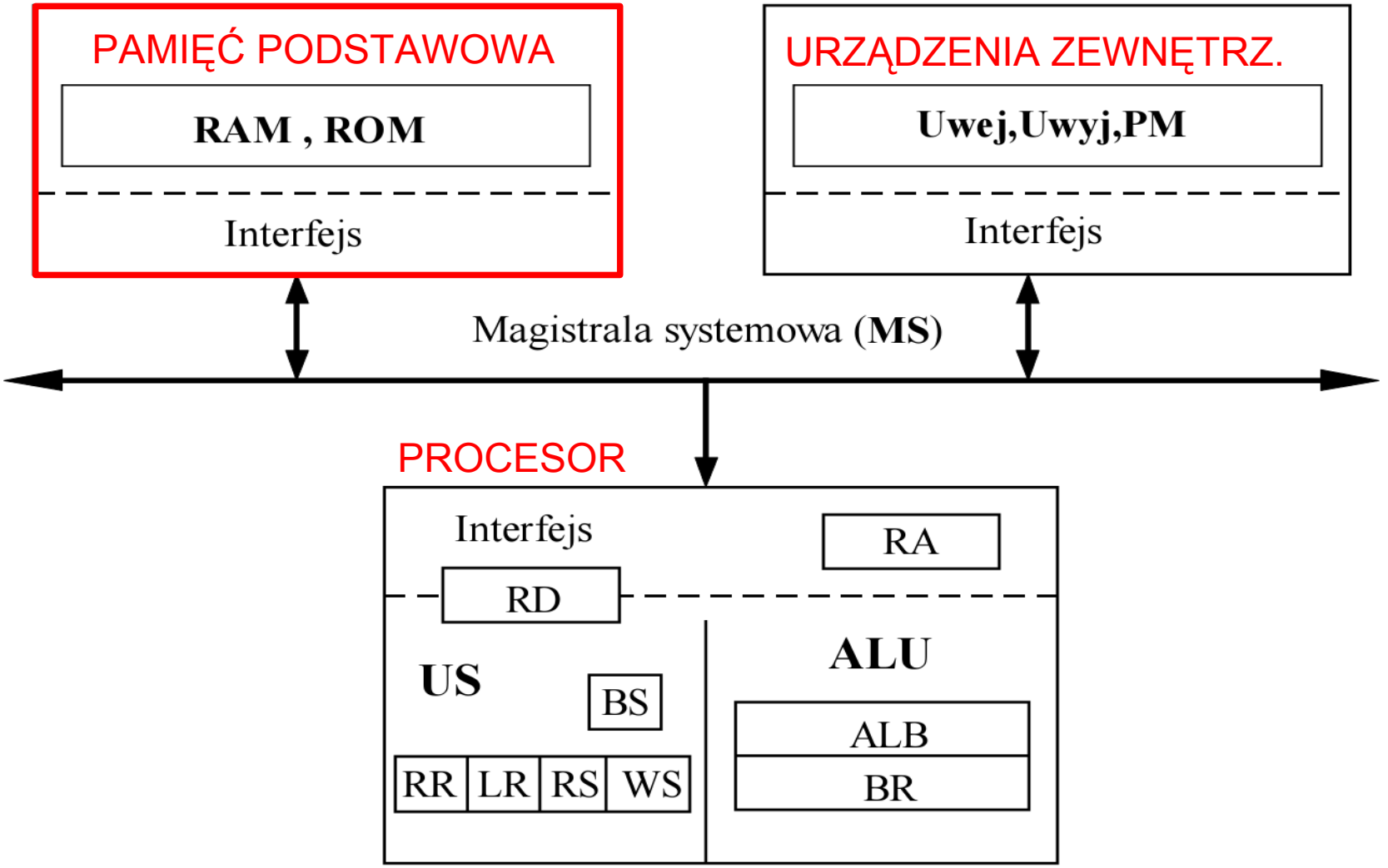
Współpraca procesora pamięcią

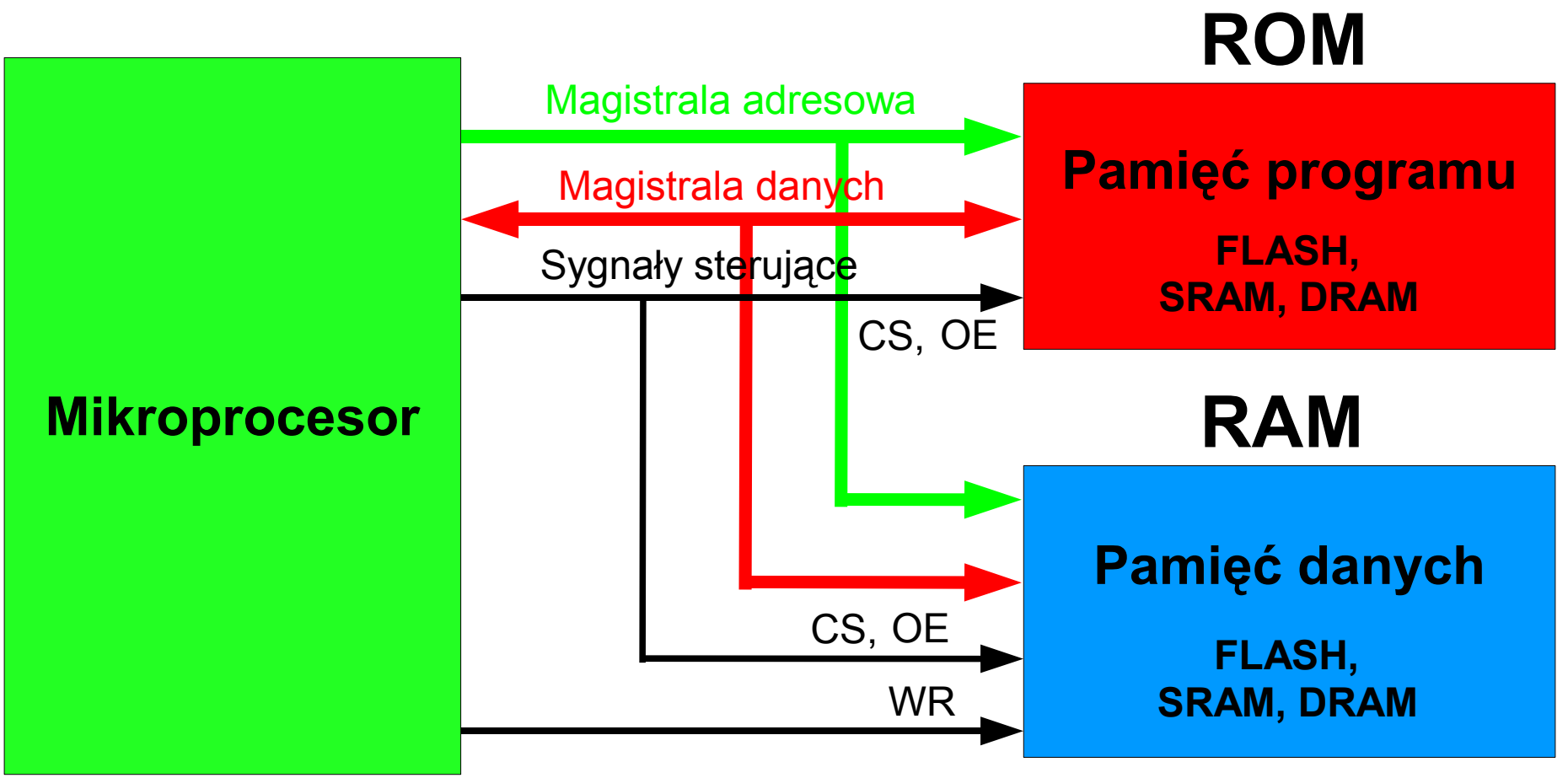
Architektura systemu komputerowego

Architektura polega na ścisłym podziale komputera na trzy podstawowe części:

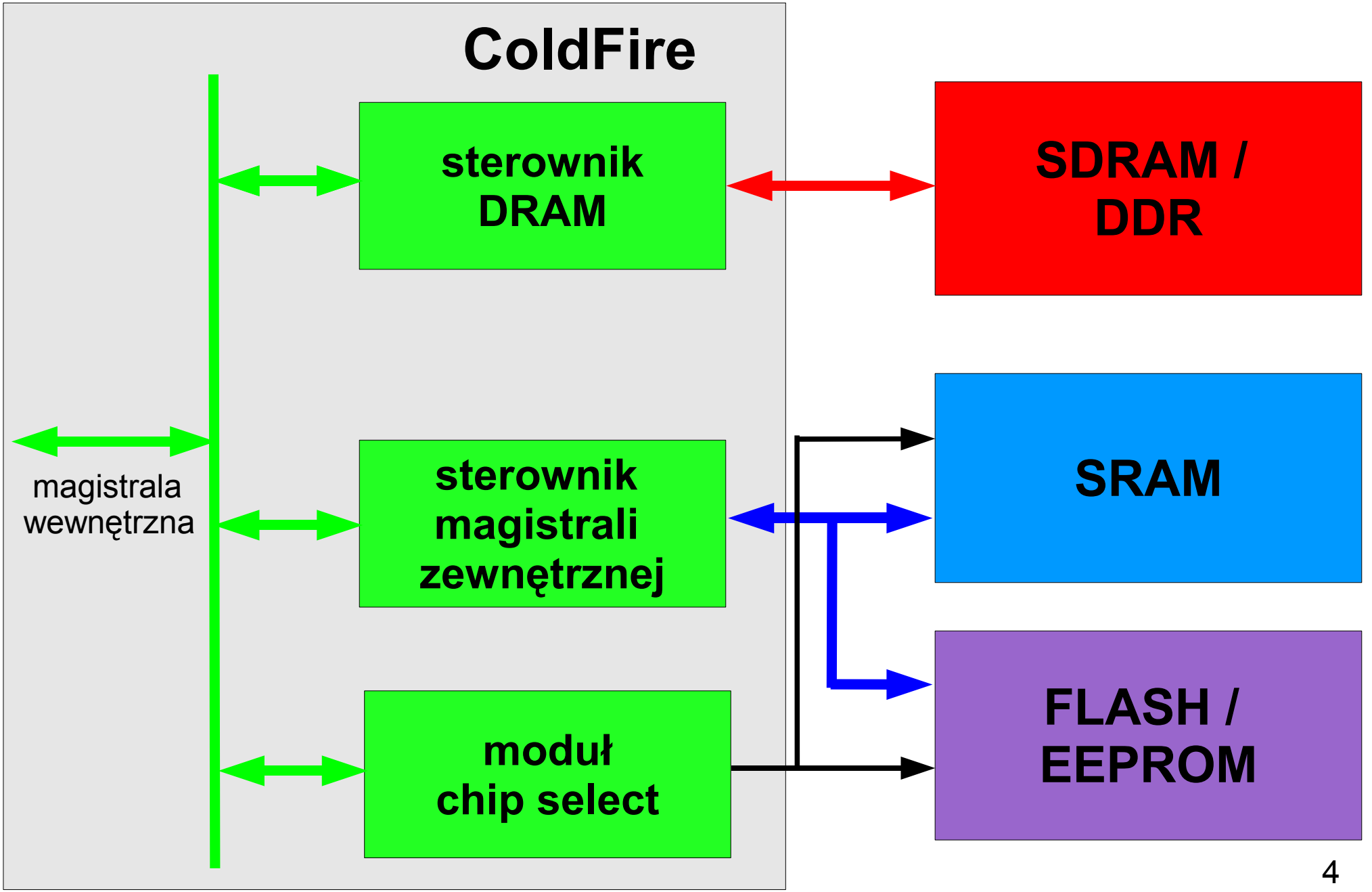
- procesor,
- pamięć (zawierająca dane oraz program),
- urządzenia wejścia/wyjścia (I/O).



Współpraca procesora z pamięcią zewnętrzną (1)



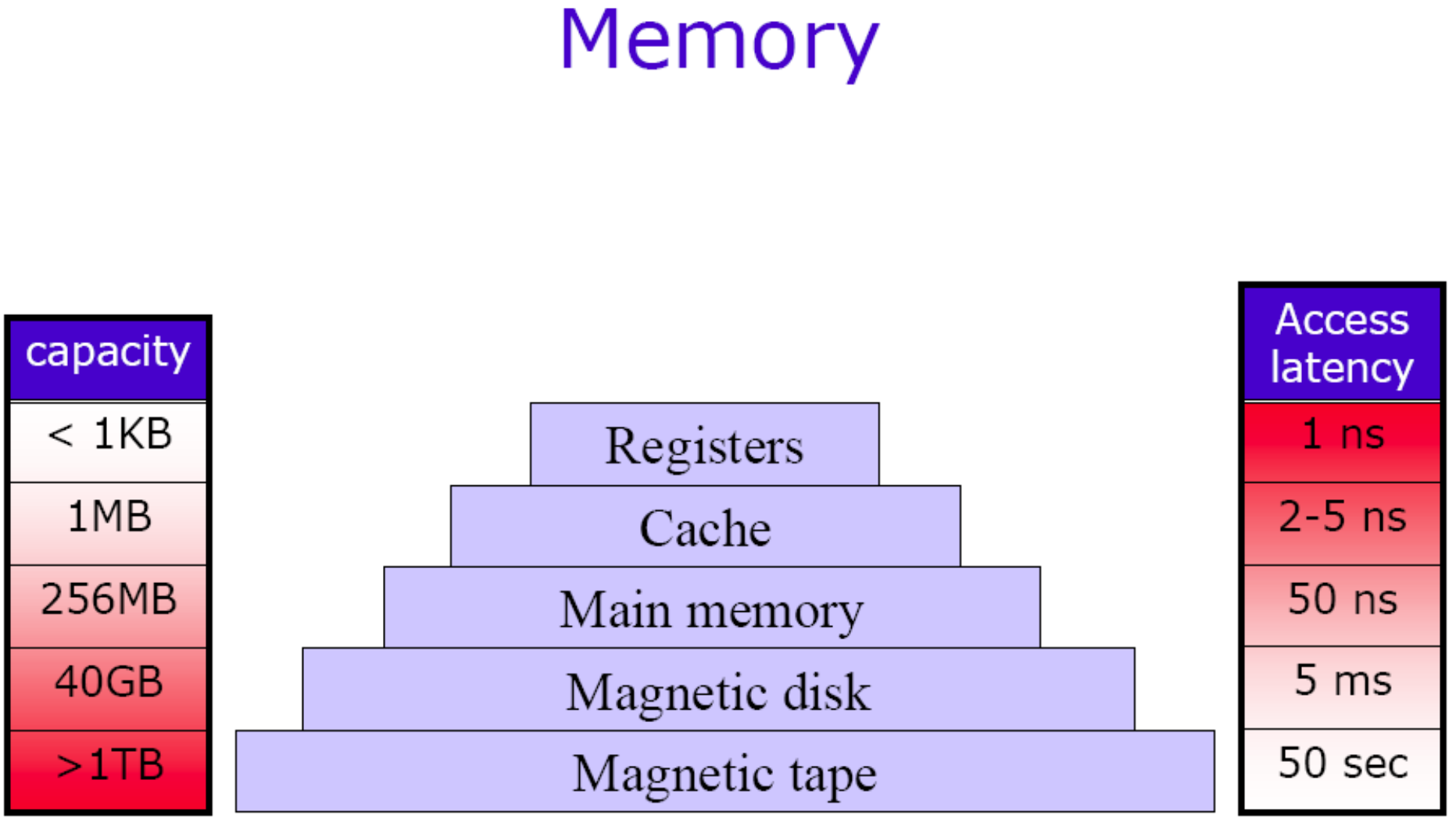
Współpraca procesora z pamięcią zewnętrzną (2)



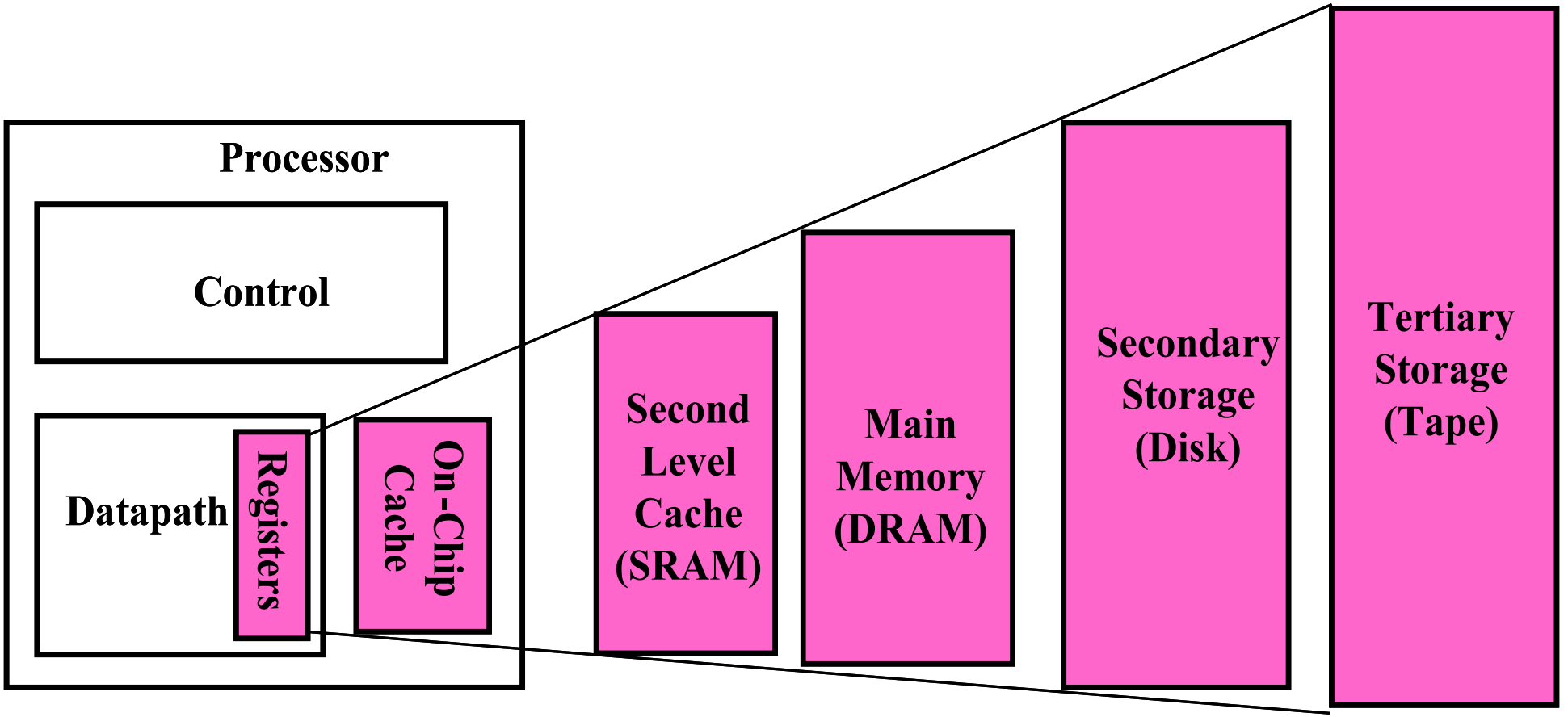
Podział pamięci

<table>
<tr><th colspan="2">Pamięci ulotne</th><th>Pamięci nieulotne</th></tr>
<tr><th>Pamięci o dostępie swobodnym
RAM</th><th>Pamięci
bez swobodnego
dostępu</th><th rowspan="2">■ programowane maską – ROM
■ programowane jednorazowo – PROM
■ kasowalne i programowalne wielokrotnie – EPROM
■ elektrycznie kasowalne i programowalne wielokrotnie – EEPROM
■ elektrycznie kasowalne w całości i programowalne wielokrotnie – FLASH
■ pamięci S-RAM z podtrzymującą baterią litową</th></tr>
<tr><td>■ statyczne S-RAM
■ dynamiczne D-RAM</td><td>■ stosowe – LIFO
■ kolejkowe – FIFO
■ skojarzeniowe – CAM
■ rejestry przesuwające</td></tr>
</table>

Hierarchia pamięci (1)



Hierarchia pamięci (2)



Speed:	~1 ns	~10 ns-100 ns	~100 ns	~10 ms	~10 sec
Size:	~100 B	~kB-MB	~MB	~GB	~TB

Tera 10^12 => TB
Peta 10^15 => PB
Exa 10^18 => EB

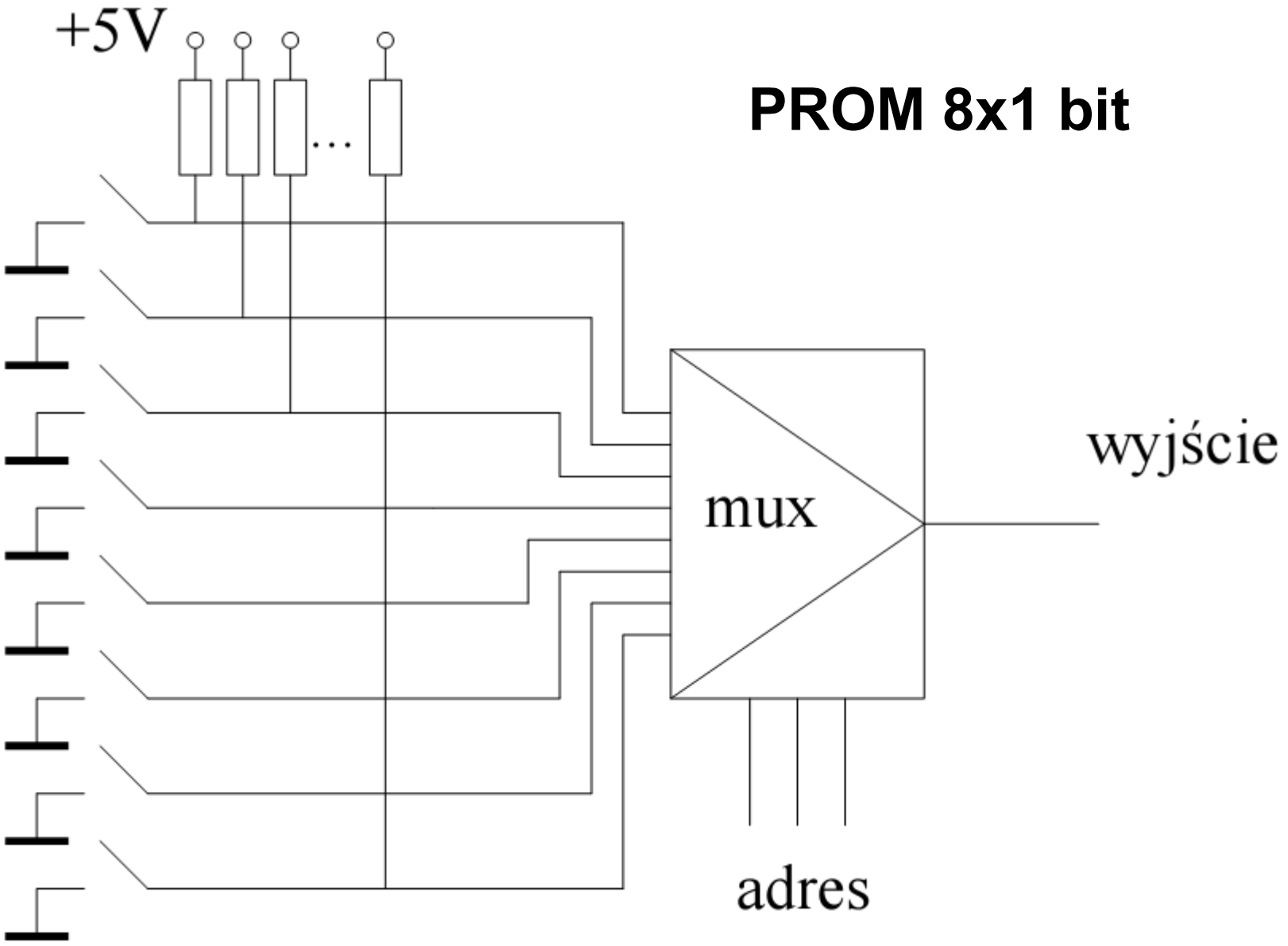
Pamięci tylko do odczytu (Read Only Memory)

Pamięci stałe ROM w systemach mikroprocesorowych

Pamięci ROM wykorzystuje się do:

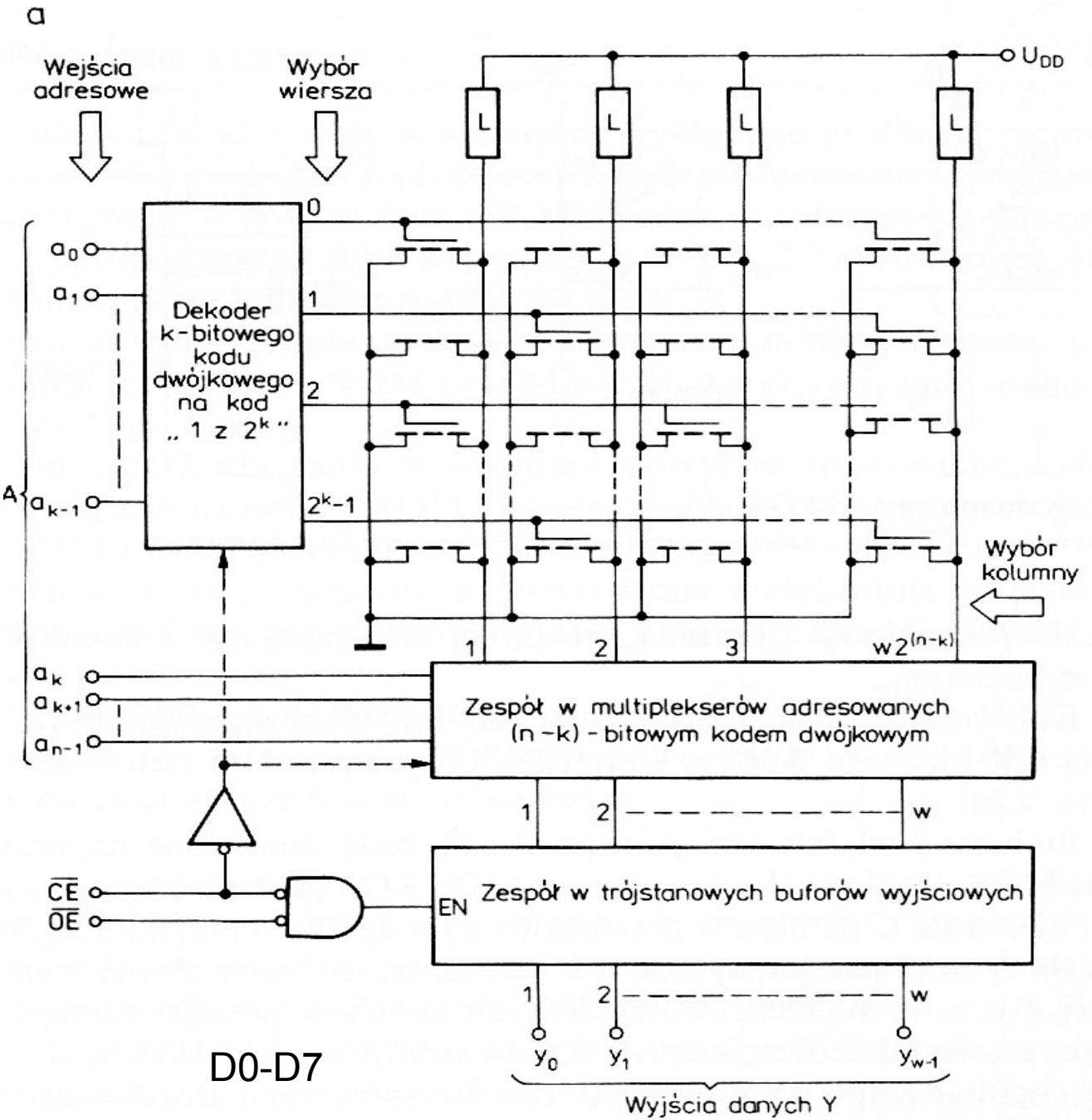
- Przechowywania programu,
- Budowy dekoderów adresowych
- Przechowywania stałych (parametrów)
- Przechowywania ustawień systemowych
- Realizacji funkcji nieliniowych, trygonometrycznych, itp., (np. tablicowanie)

Pamięć stała (1)



Pamięć stała (2)

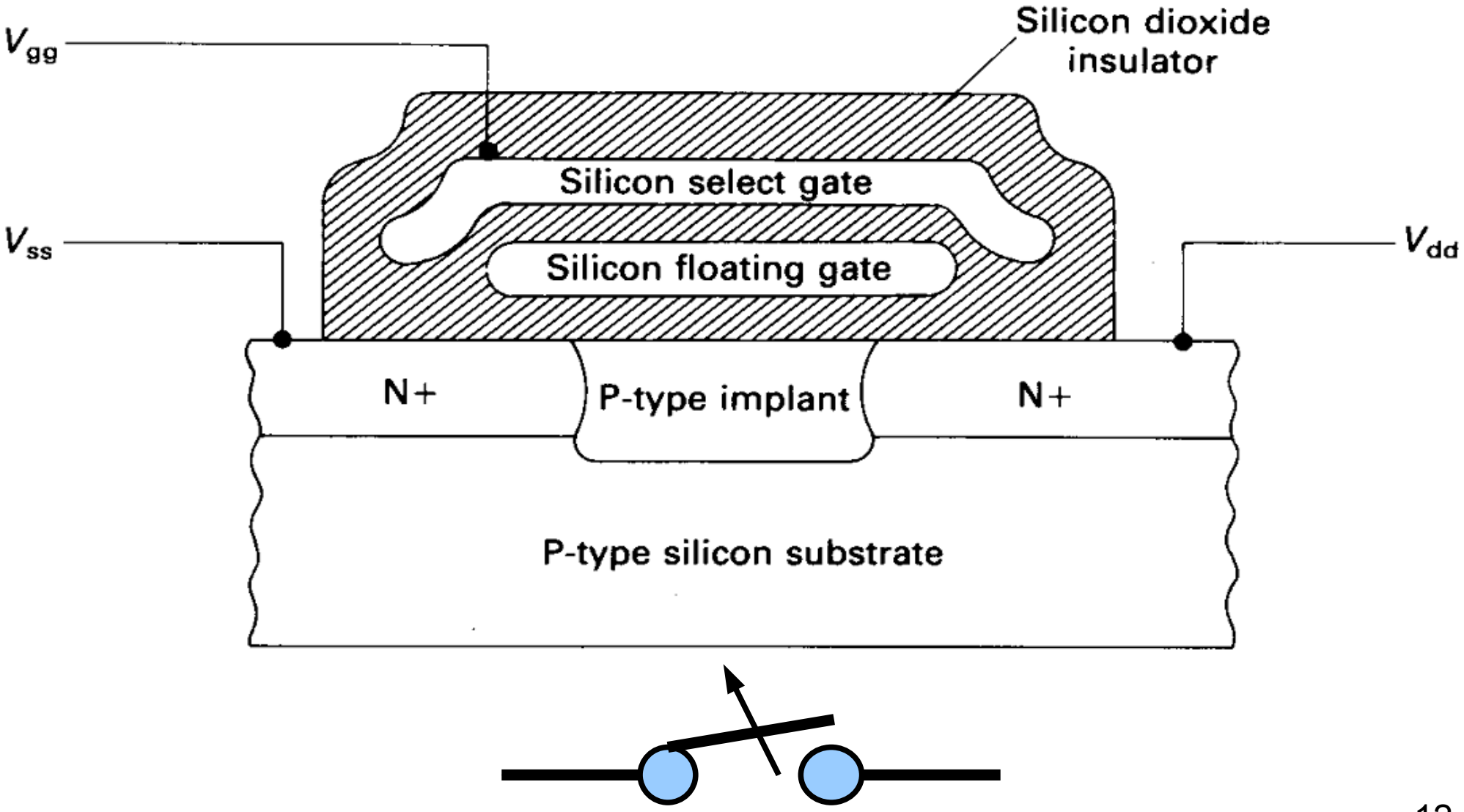
A0-A19 - 1MB



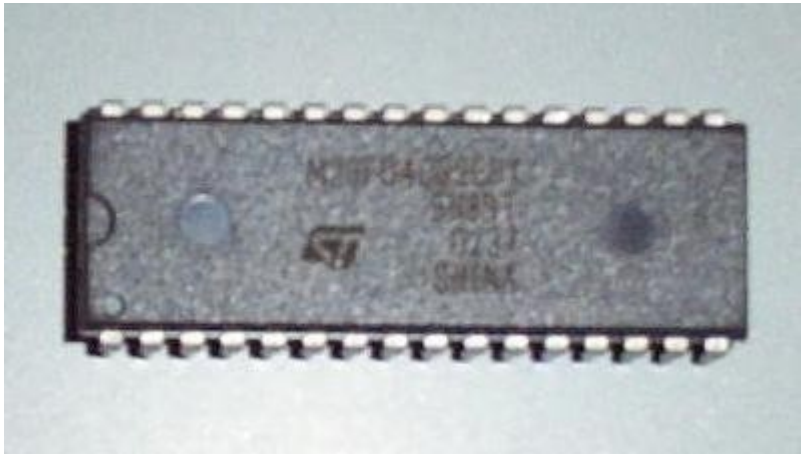
D0-D7

Pamięć EPROM

Structure of an EPROM memory cell

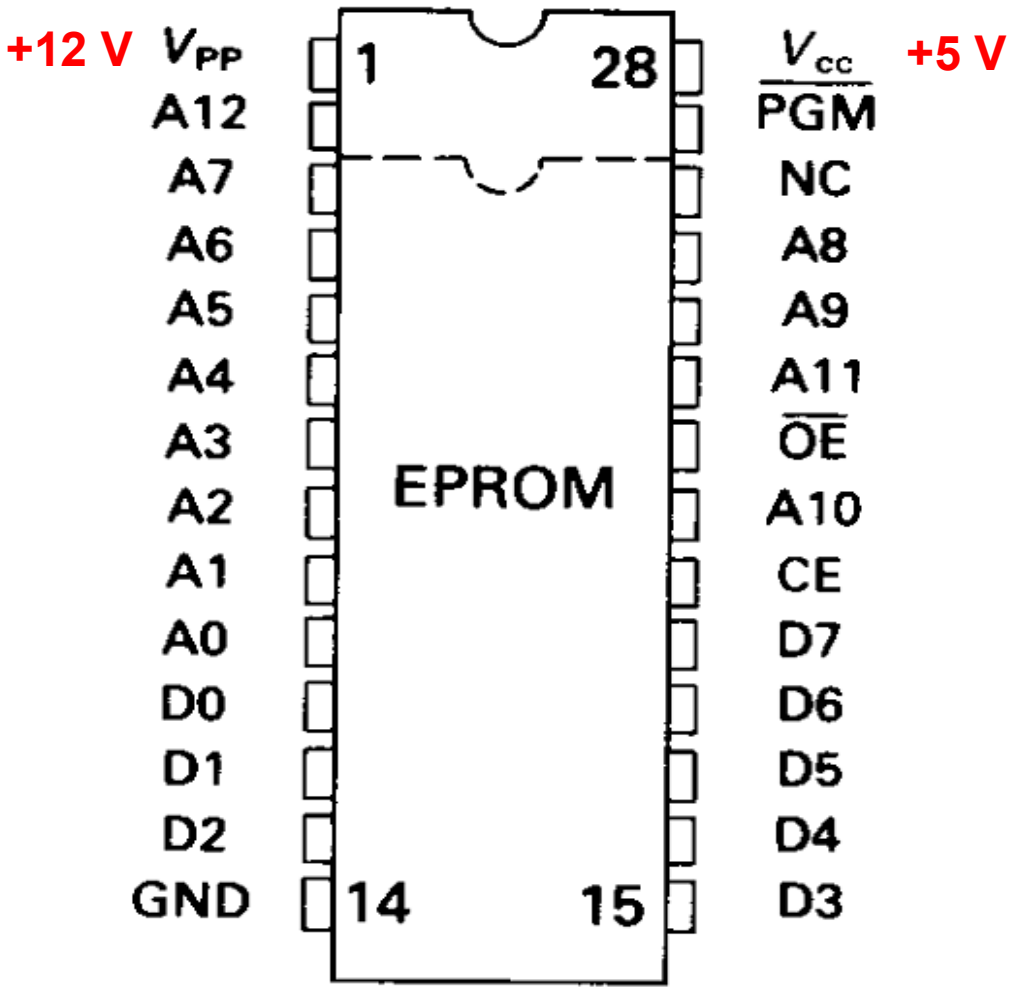


Pamięci EPROM



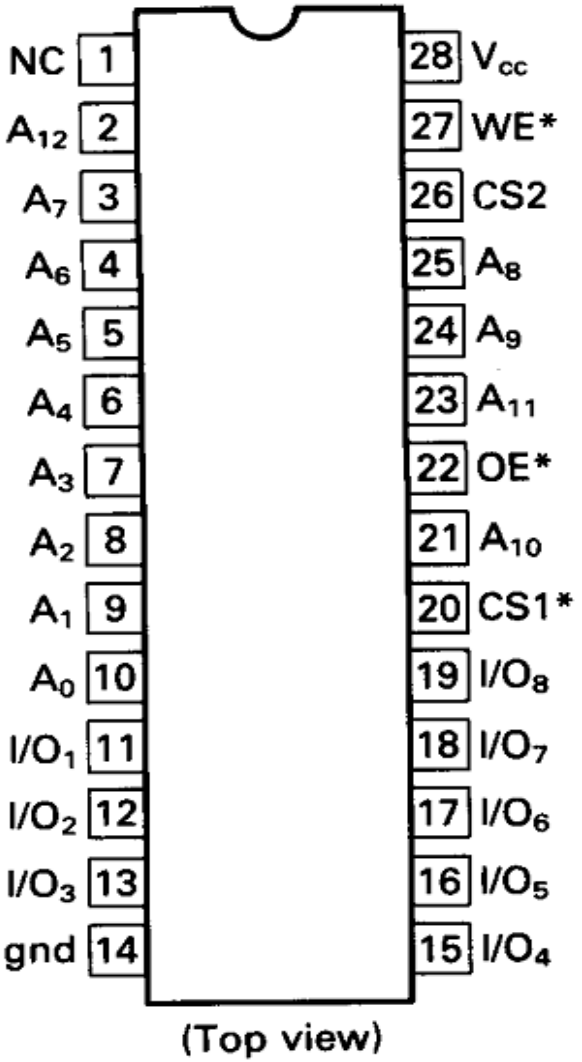
Pamięci EPROM / SRAM

2764



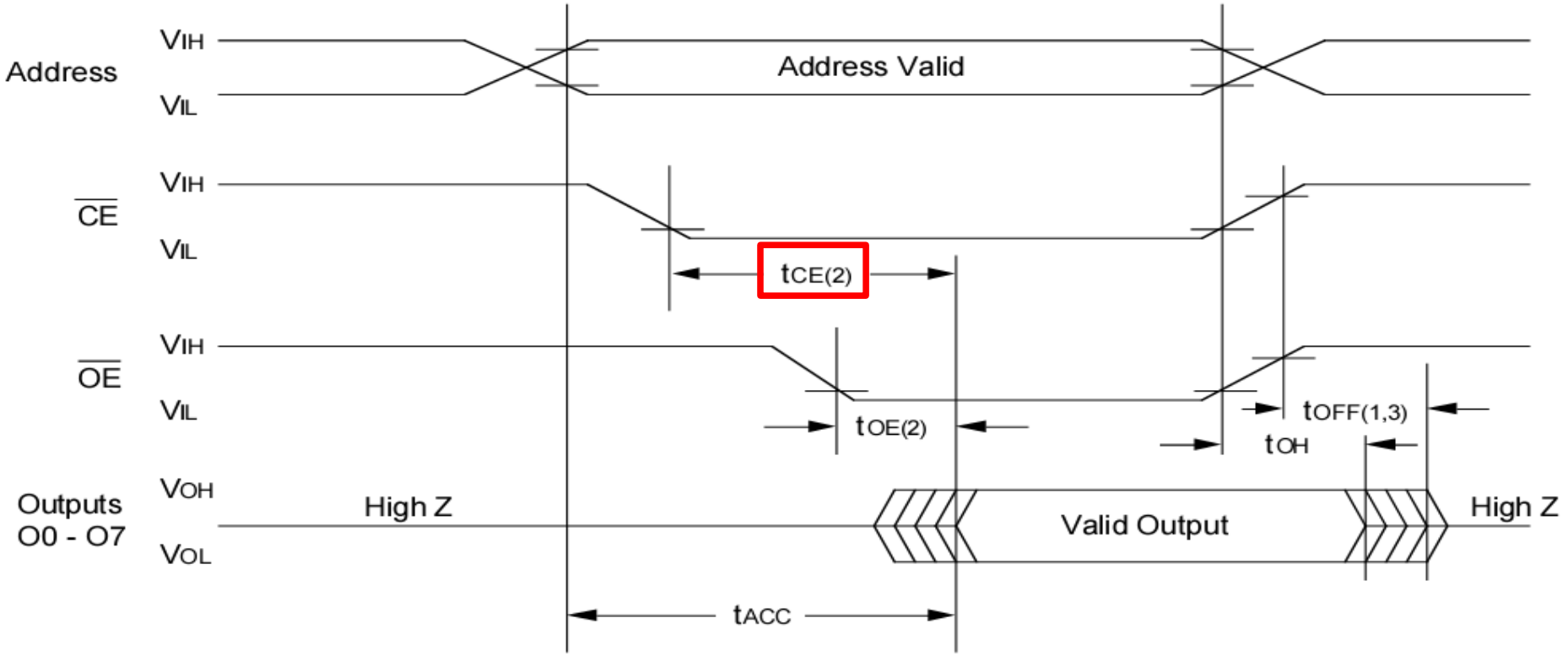
EPROM

6264



SRAM

Odczyt danej z pamięci EPROM

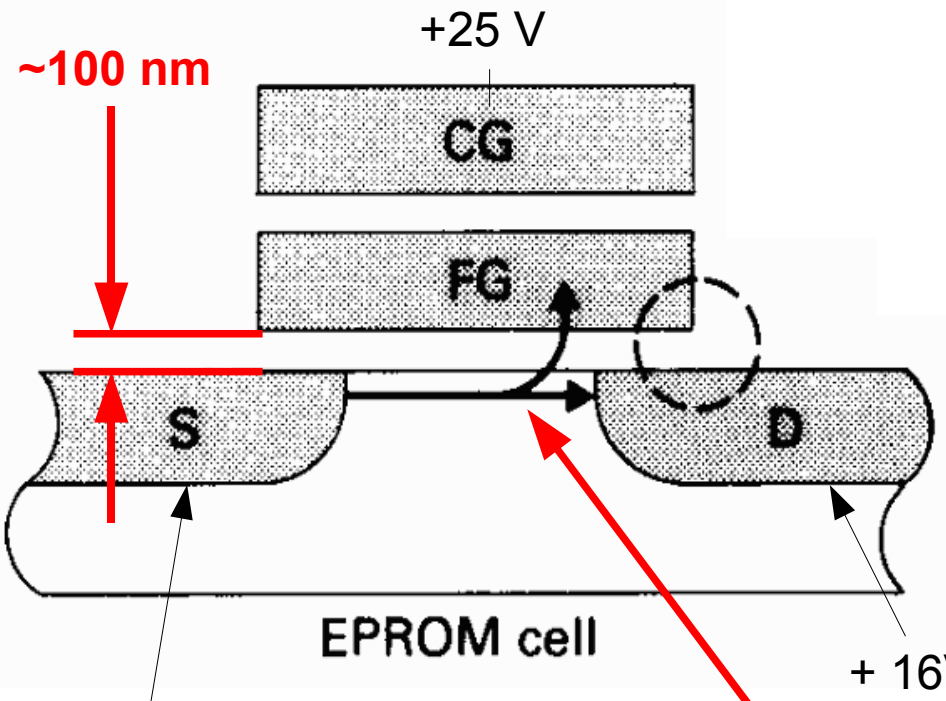


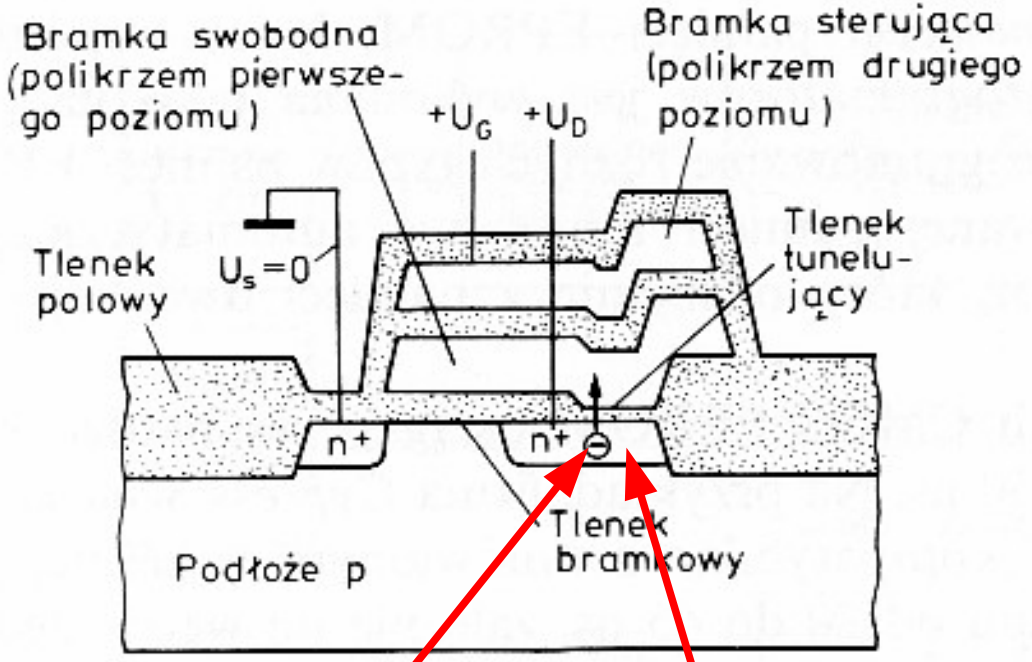
Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$=$\overline{OE}$ =VIL
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = VIL
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = VIL
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

Pamięci EPROM <=> EEPROM

Structure of EPROM and flash EEPROM memory cells

CG — control gate
FG — floating gate
S — source
D — drain





Elektrony gorące: 10^5 V/cm

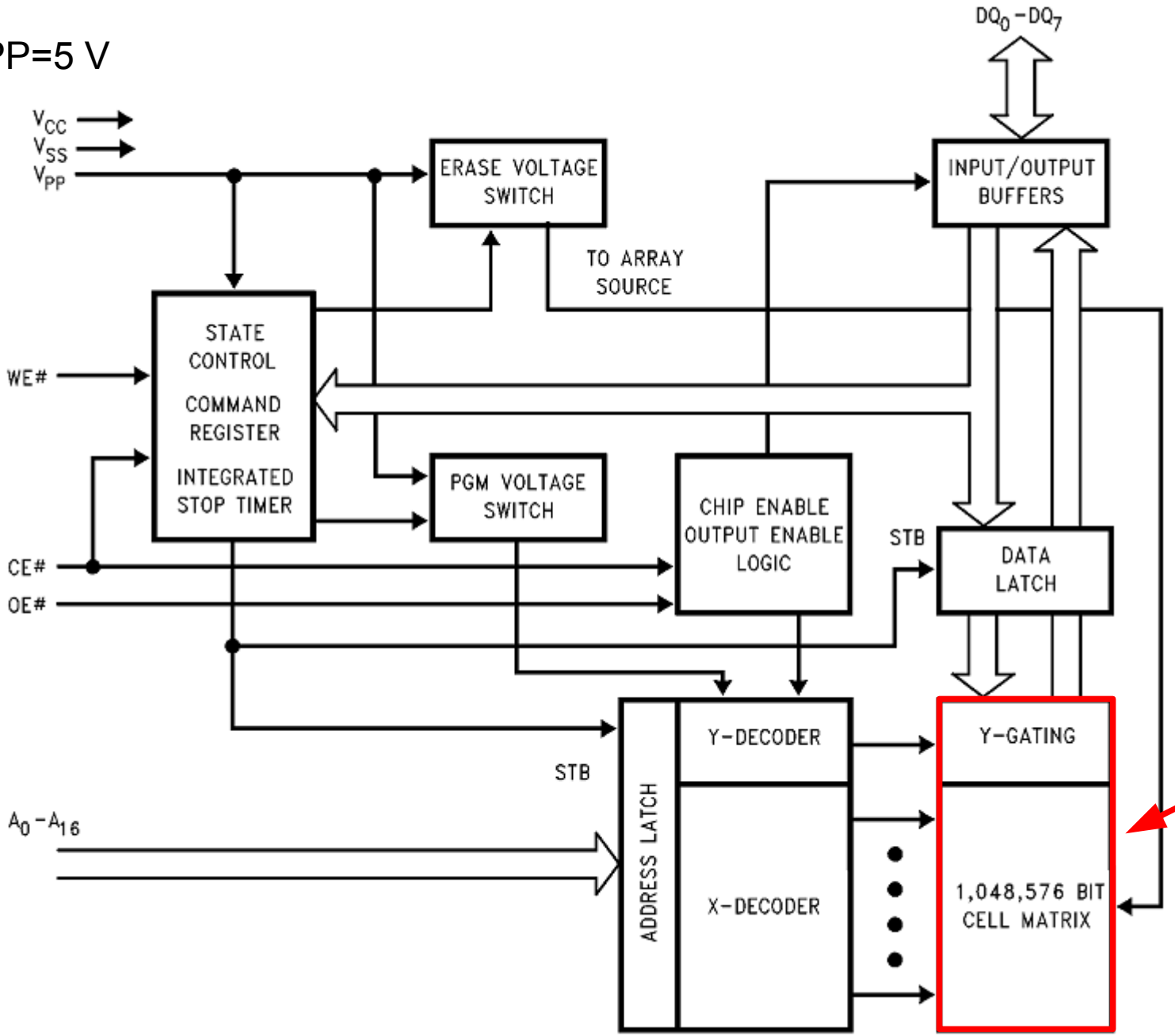
Kasowanie

Programowanie

Programowanie = wpisanie zer do komórek pamięci

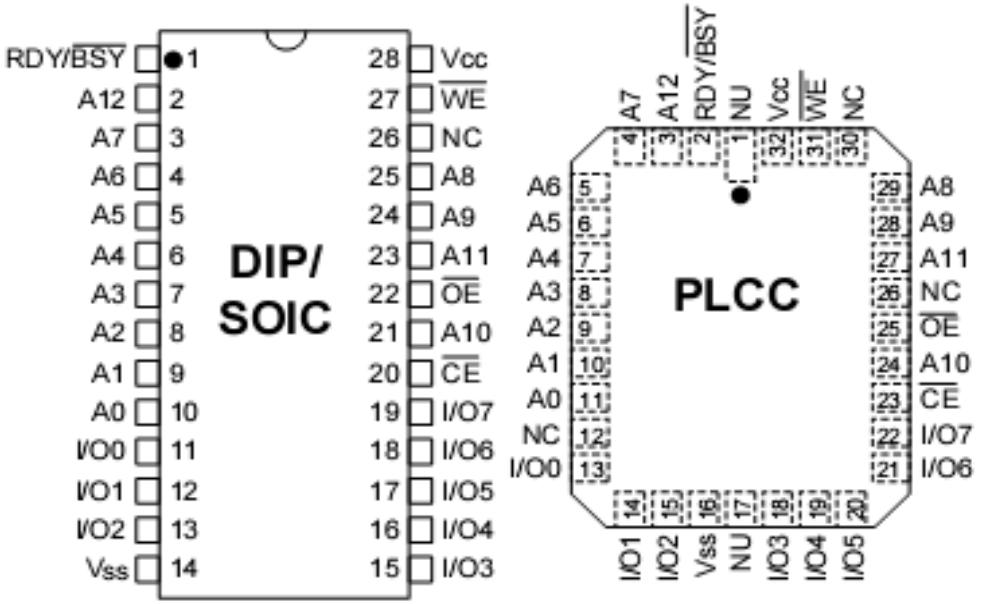
Pamięć EEPROM

VCC=VPP=5 V

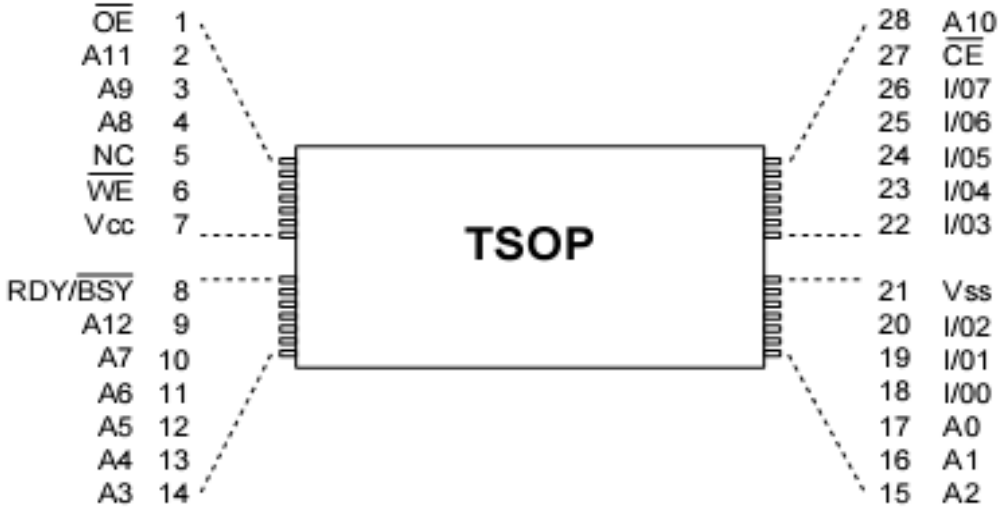


Matryca pamięci

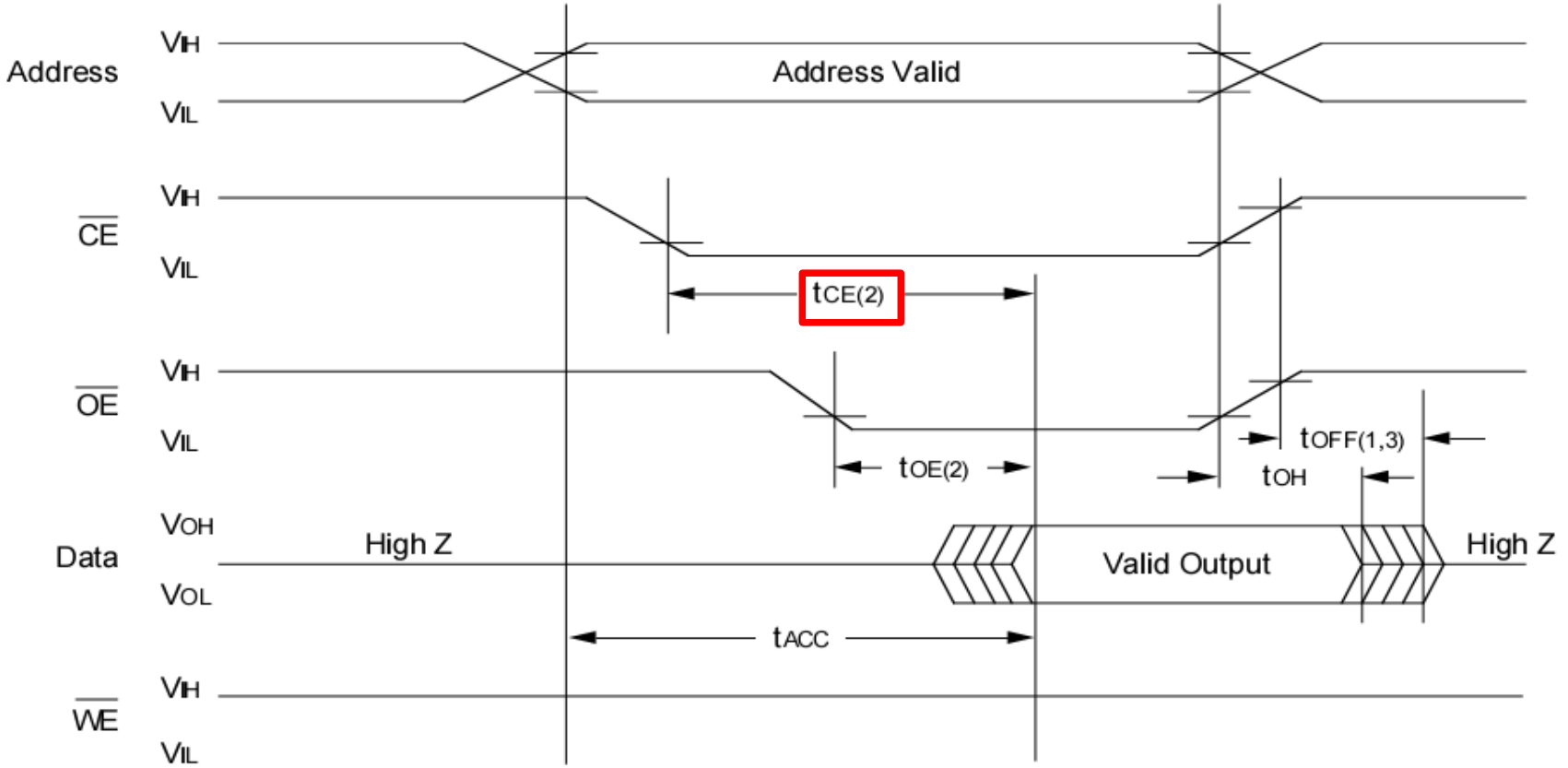
EEPROM 28C64A



● Pin 1 indicator on PLCC on top of package

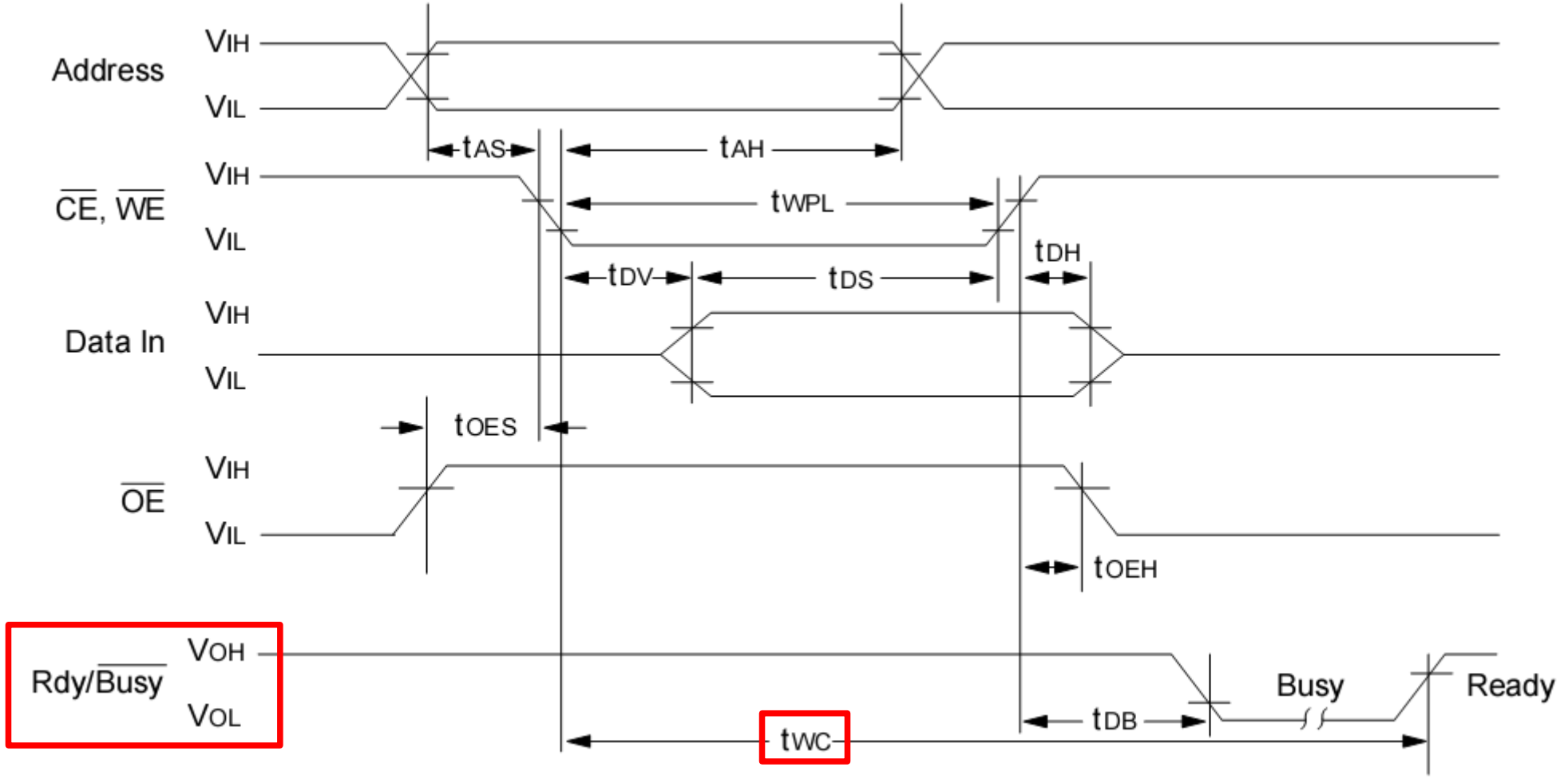


Odczyt pamięci EEPROM



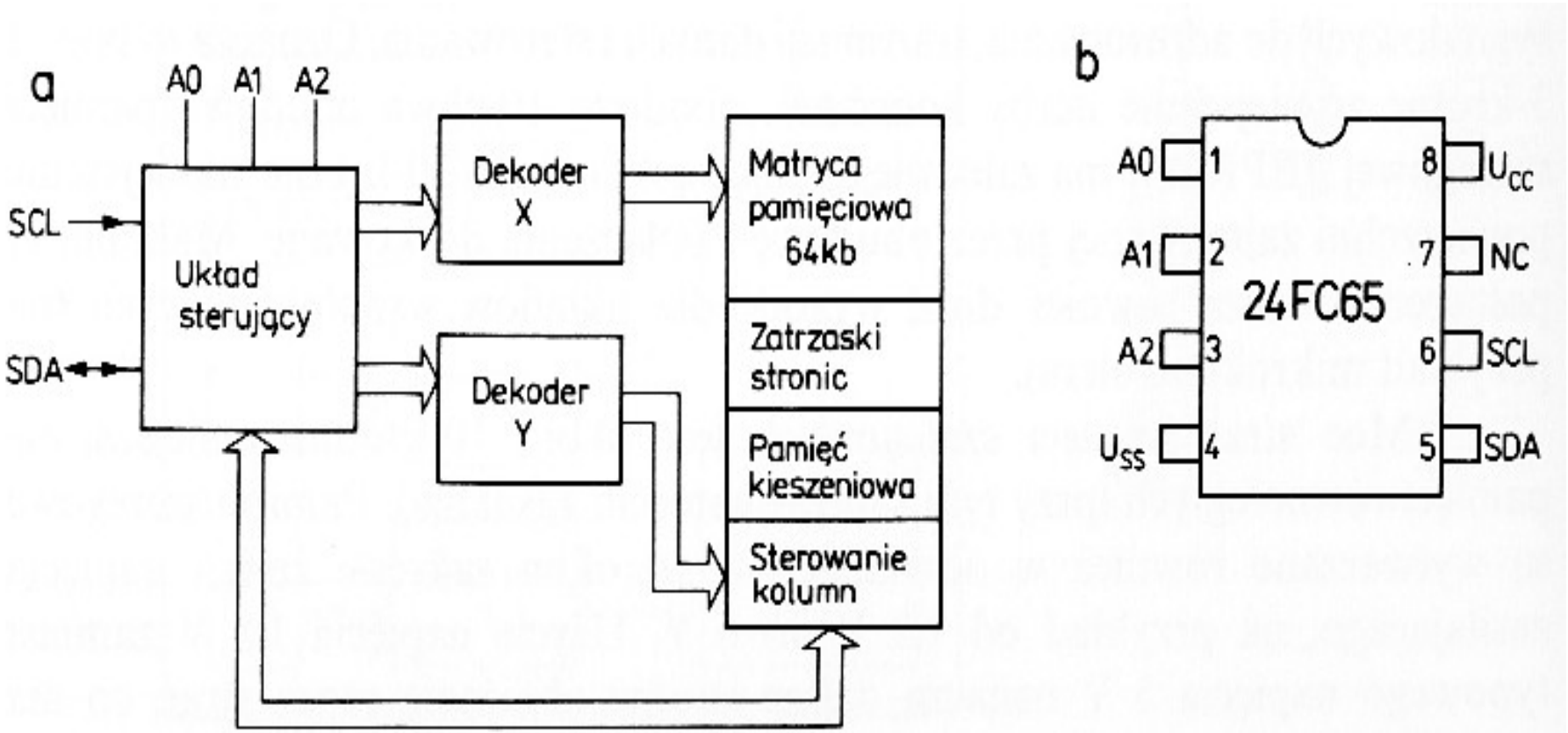
Parameter	Symbol	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = VIL
$\overline{CE}$ to Output Delay	tCE	—	150	—	200	—	250	ns	$\overline{OE}$ = VIL
$\overline{OE}$ to Output Delay	tOE	—	70	—	80	—	100	ns	$\overline{CE}$ = VIL
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	50	0	55	0	70	ns	Note 1
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	tOH	0	—	0	—	0	—	ns	Note 1

Zapis pamięci EEPROM



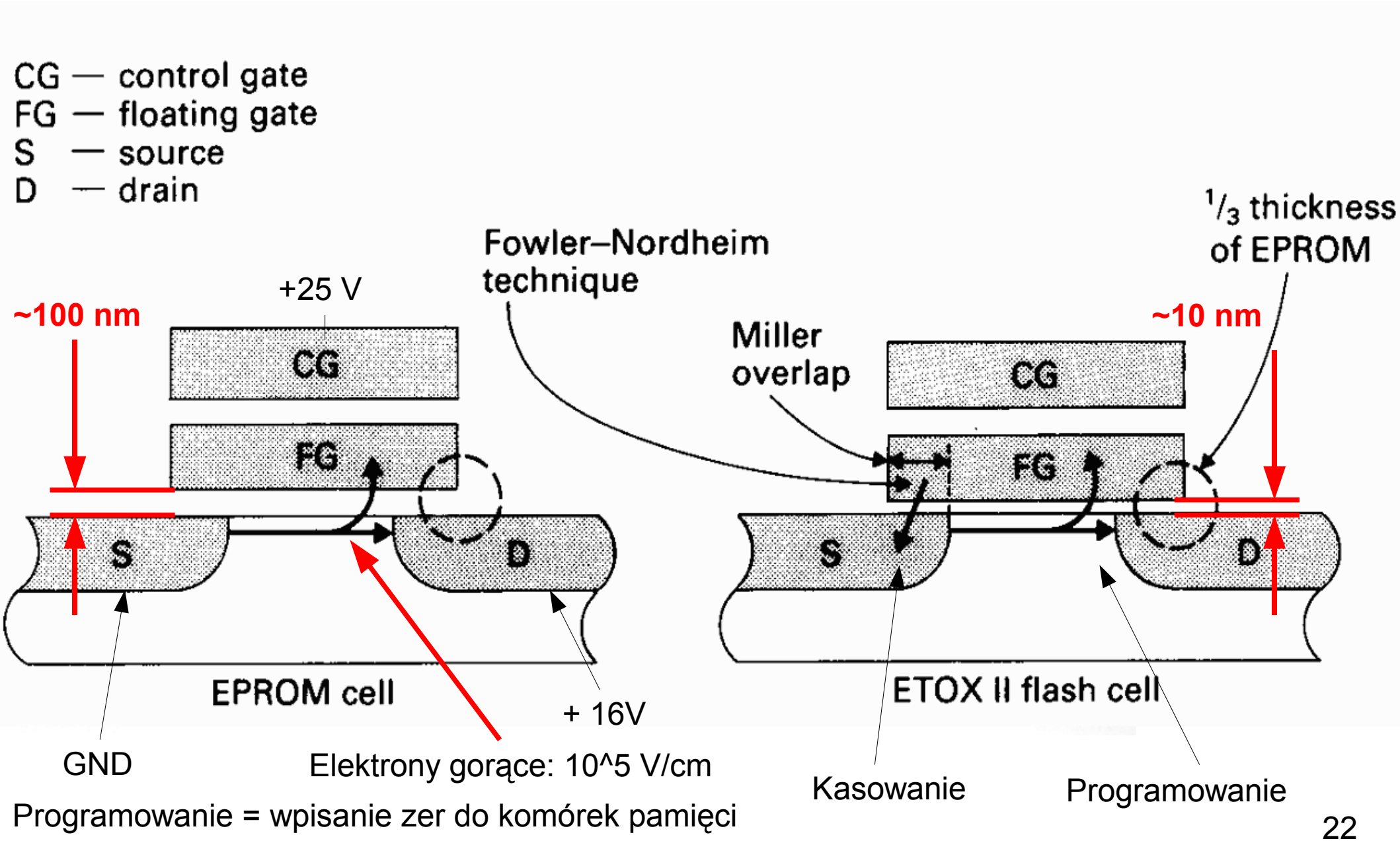
Parameter	Symbol	Min	Max	Units	Remarks
Time to Device Busy	tDB	2	50	ns	
Write Cycle Time (28C64A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	tWC	—	200	µs	100 µs typical

Pamięć EEPROM z interfejsem I^2C



Niewielka pamięć z interfejsem szeregowym 8k x 8 = 64 kb

Pamięci EPROM <=> FLASH



Programowanie = wpisanie zer do komórek pamięci

Pamięci FLASH (1)

Zalety:

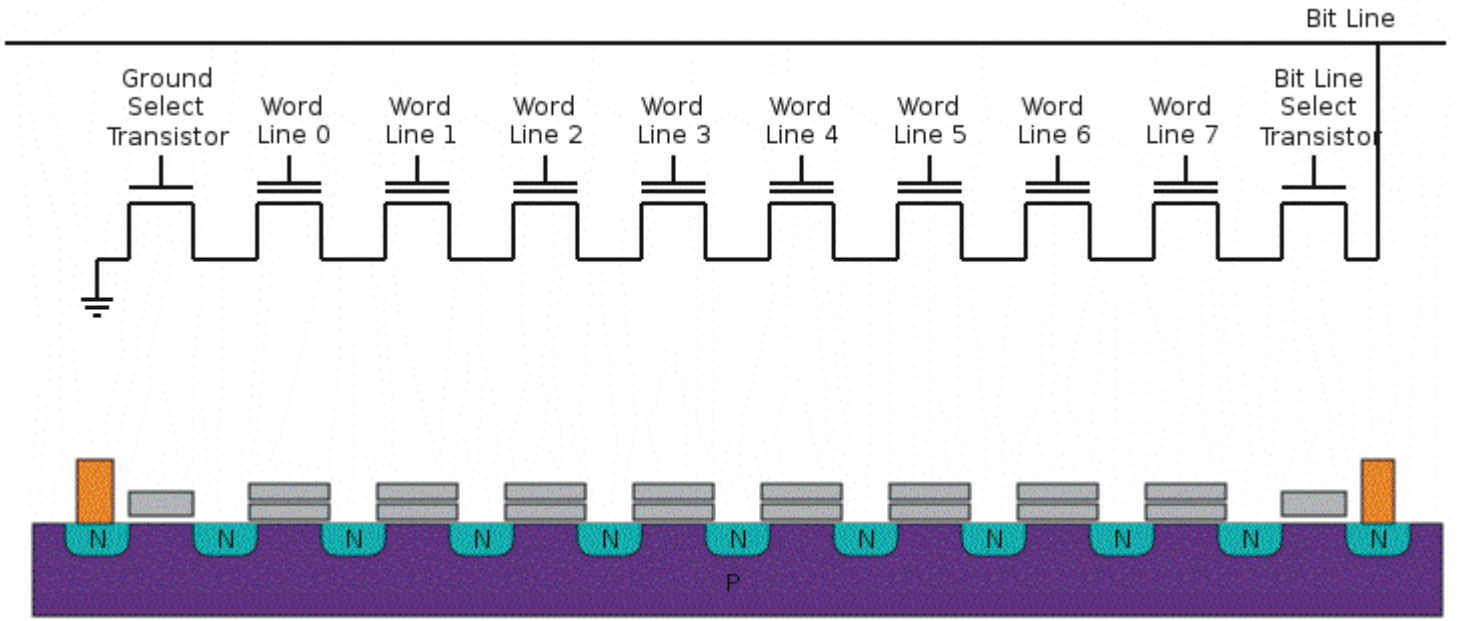
- Możliwość szybkiego kasowania sektorów (bloków) pamięci,
- Duża pojemność pamięci (jednotranzystorowe komórki),
- Niskie napięcie zasilania (3,3 V, 5 V),
- Krótki czas odczytu danych (~10 ns).
- Niewielkie rozmiary,
- Duża odporność na wstrząsy,
- Mały pobór energii.

Wady:

- Brak możliwości kasowania pojedynczych bajtów.

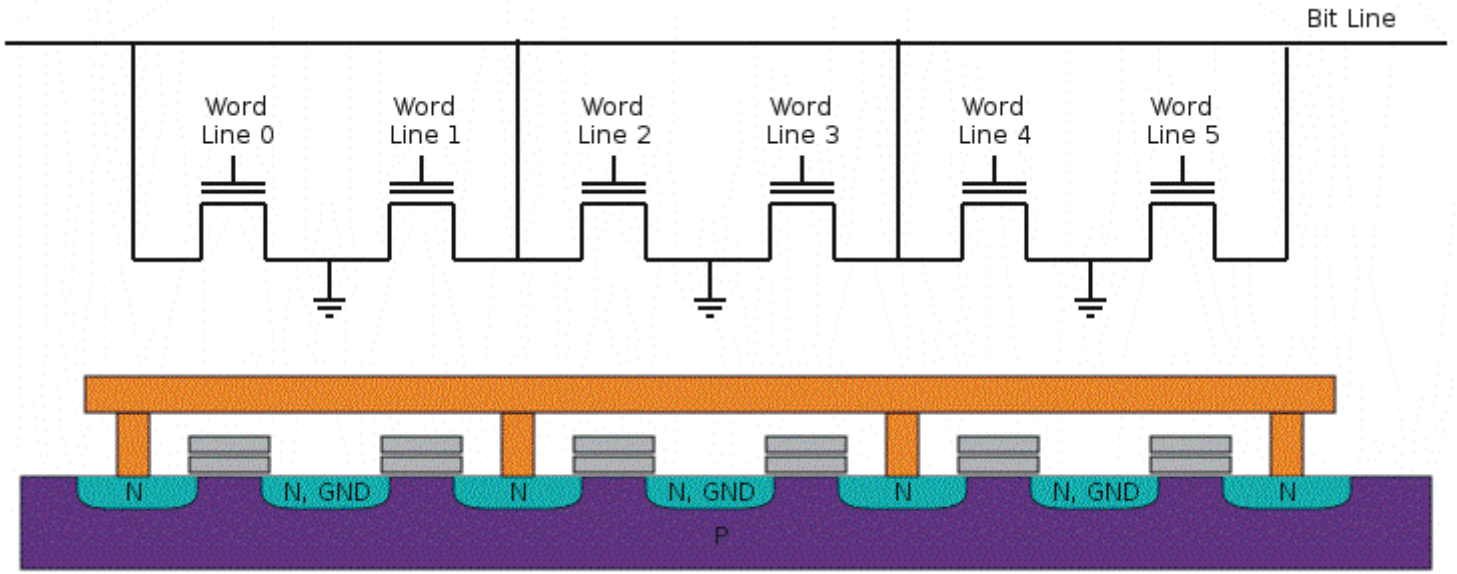
Pamięci FLASH (2)

Pamięć FLASH NAND vs NOR



NAND FLASH

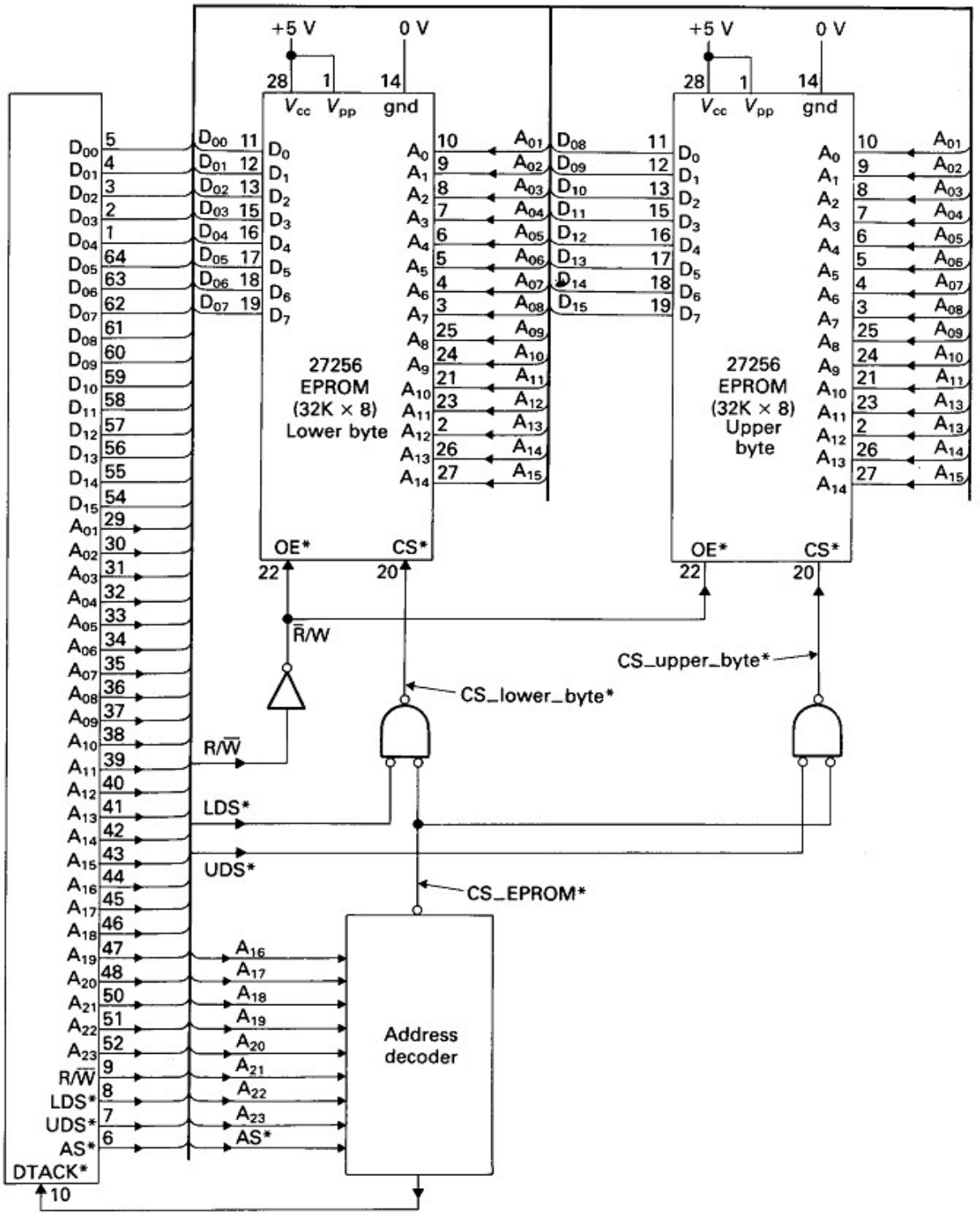
NOR FLASH



Kasowanie zawartości pamięci

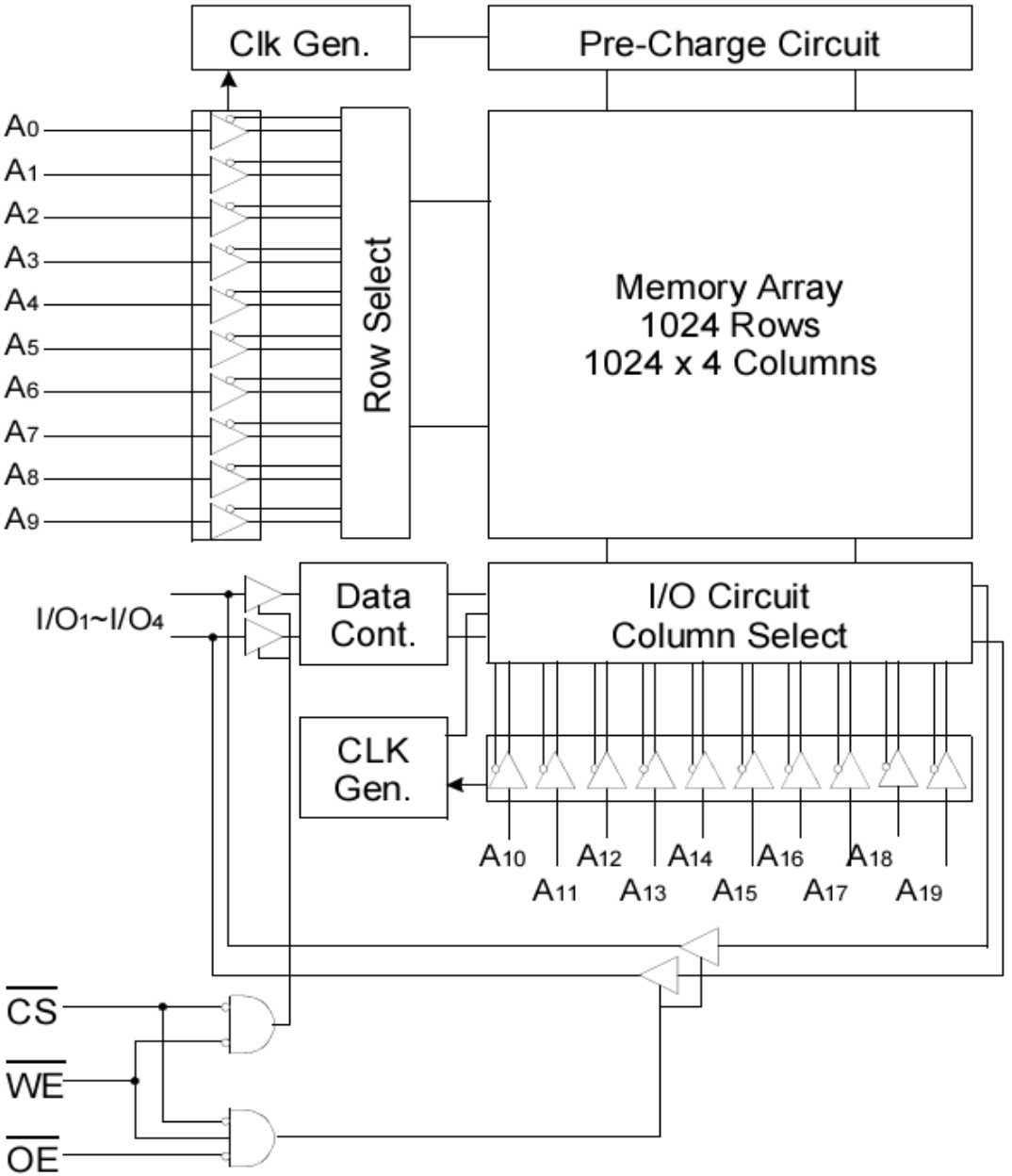
- PROM - niemożliwe
- EPROM - ultrafiolet (cała pamięć, ok. 20 min)
- EEPROM - elektrycznie (cała pamięć lub pojedyncze bloki, kasowane poprzez specyficzną sekwencję)
- Flash EEPROM - podobne jak EEPROM

Connecting a 27256 EPROM to a 68000 CPU



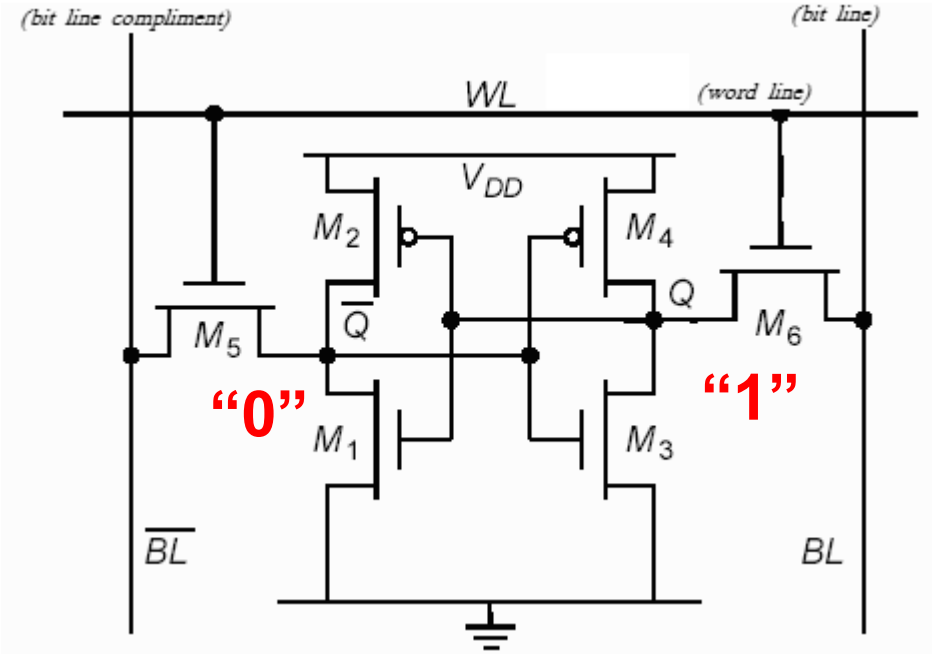
Pamięci o dostępie swobodnym (Random Access Memory)

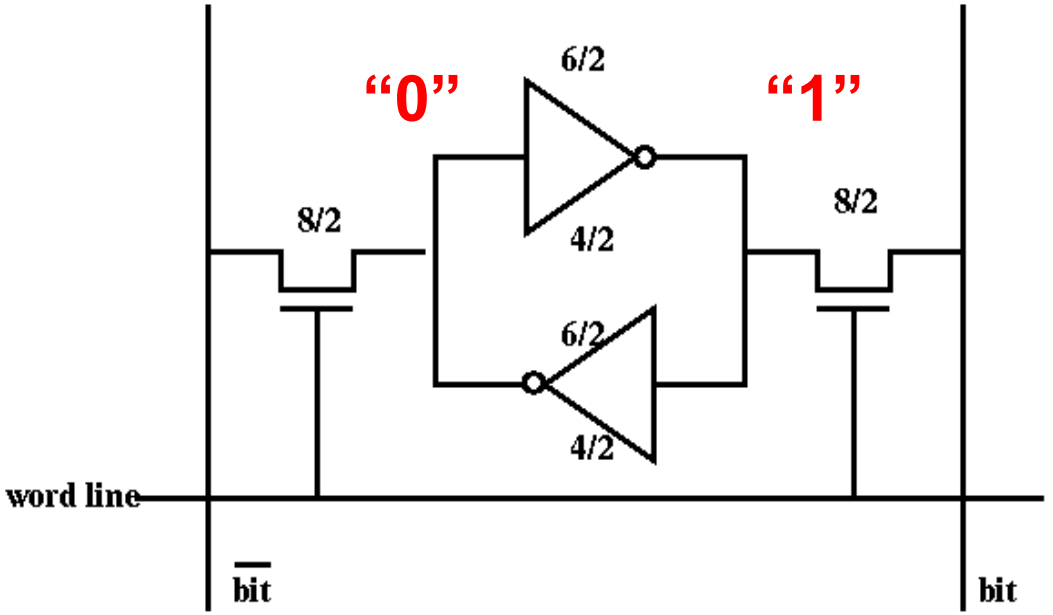
Schemat blokowy pamięci SRAM

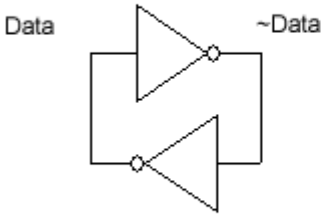


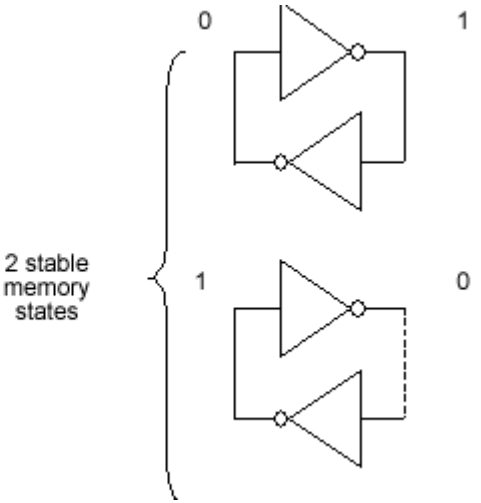
Pin Name	Pin Function
A_0 - A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_4	Data Inputs/Outputs
V_{CC}	Power(+5.0V)
V_{SS}	Ground
N.C	No Connection

Komórka pamięci statycznej

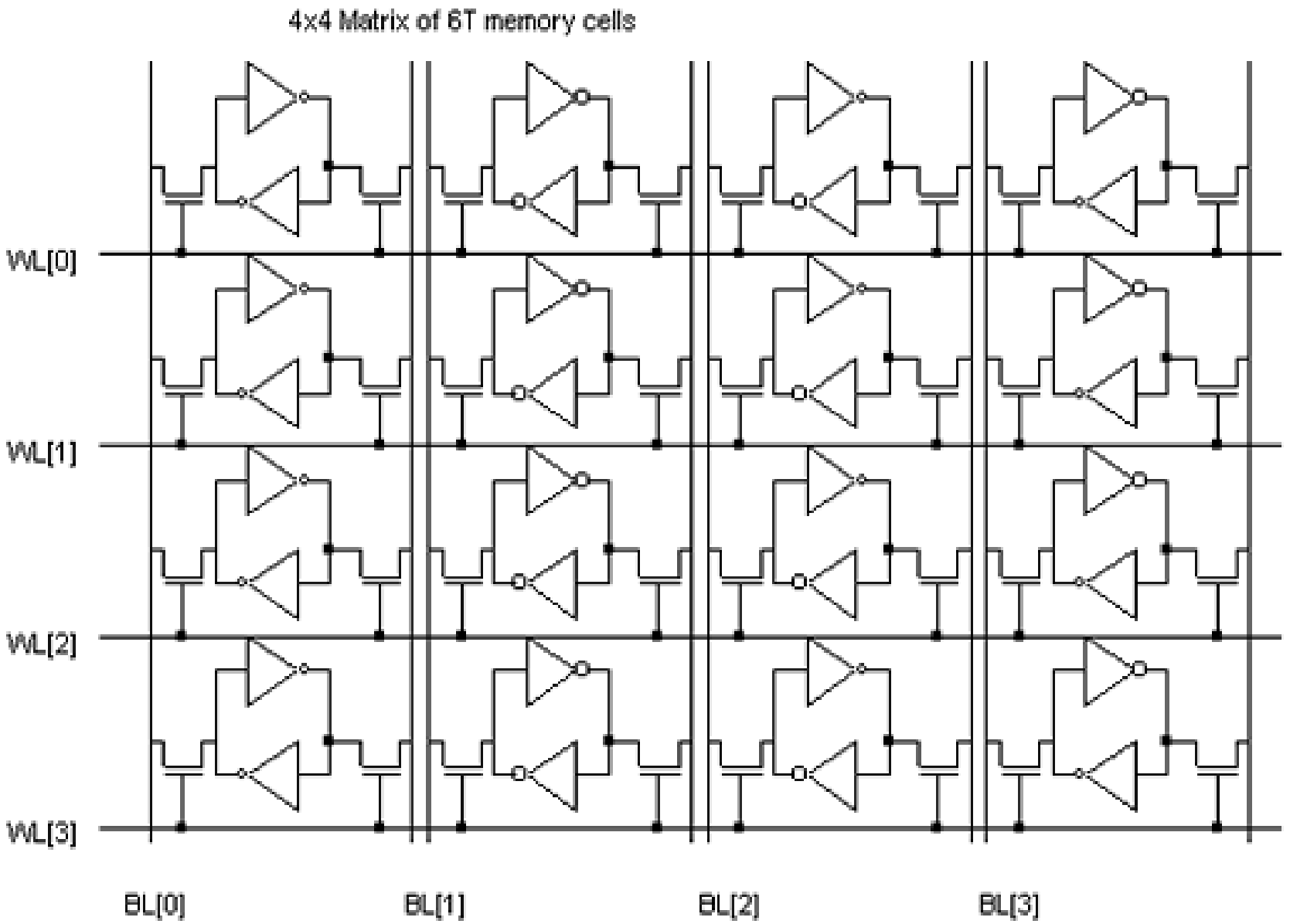








Matryca pamięci statycznej



Pamięci SRAM

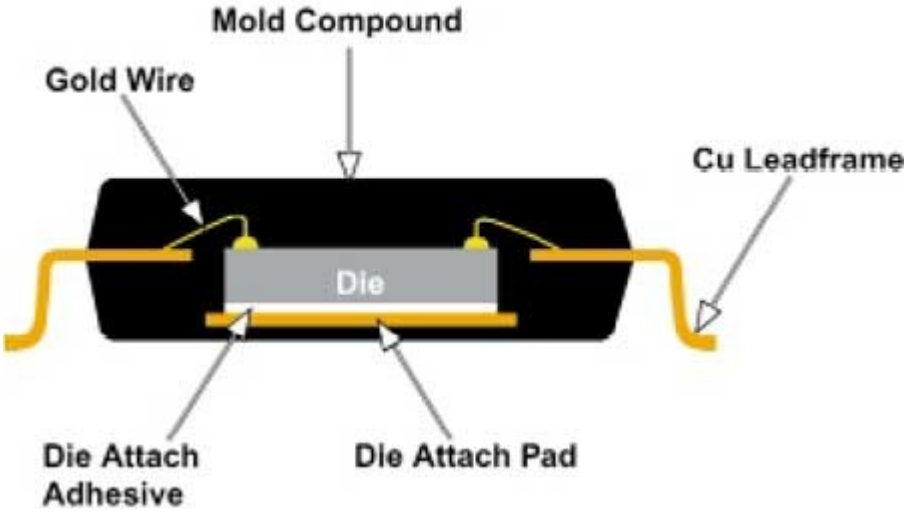
Zalety:

- Szybki czas zapisu oraz odczytu (~10 ns),
- Niskie napięcie zasilania (~1.2V - 5 V),
- Niewielkie rozmiary,
- Mały pobór energii.

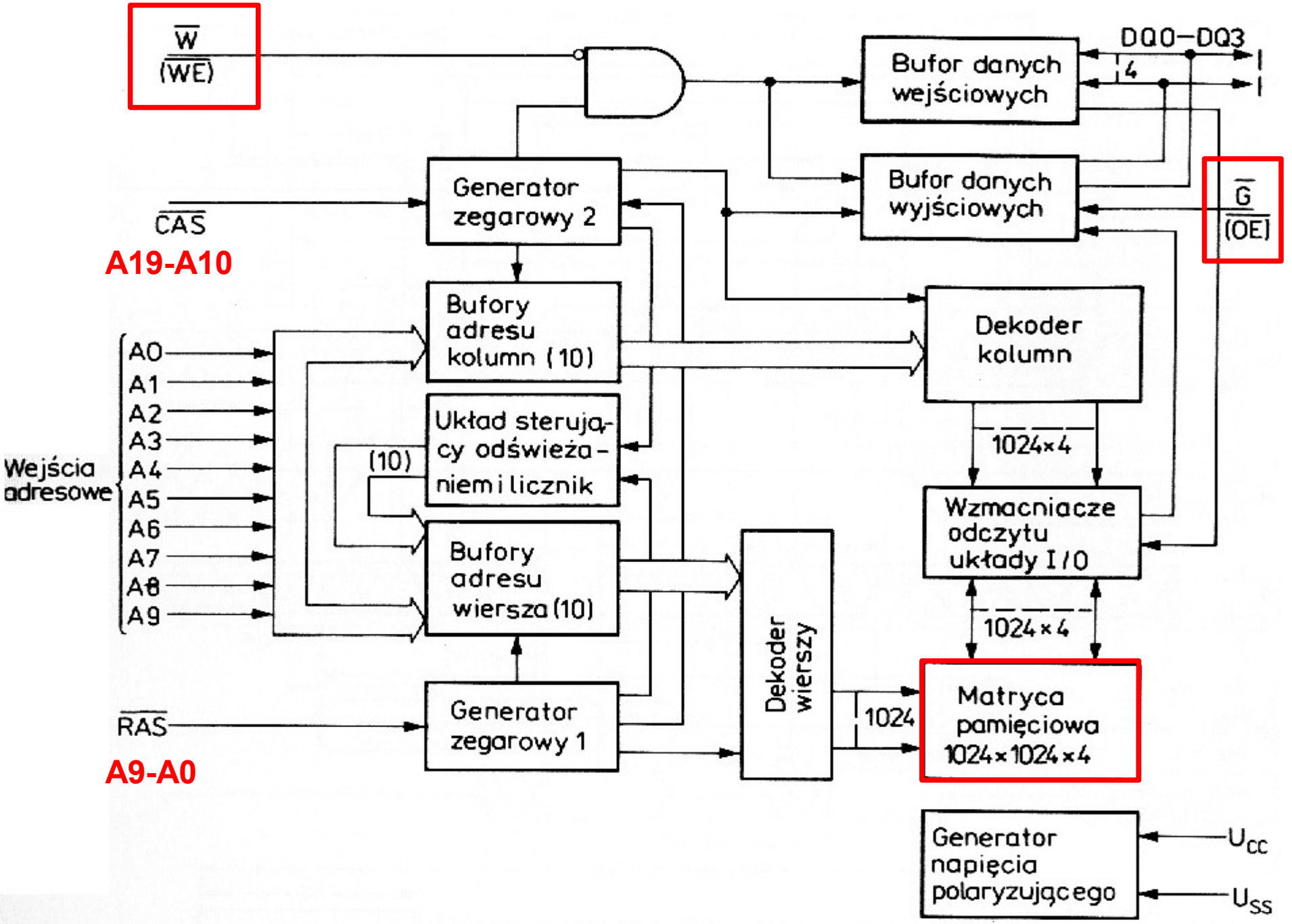
Wady:

- Stosunkowo niewielkie pojemności pamięci (< 4 MB),
- Wysoka cena pamięci.

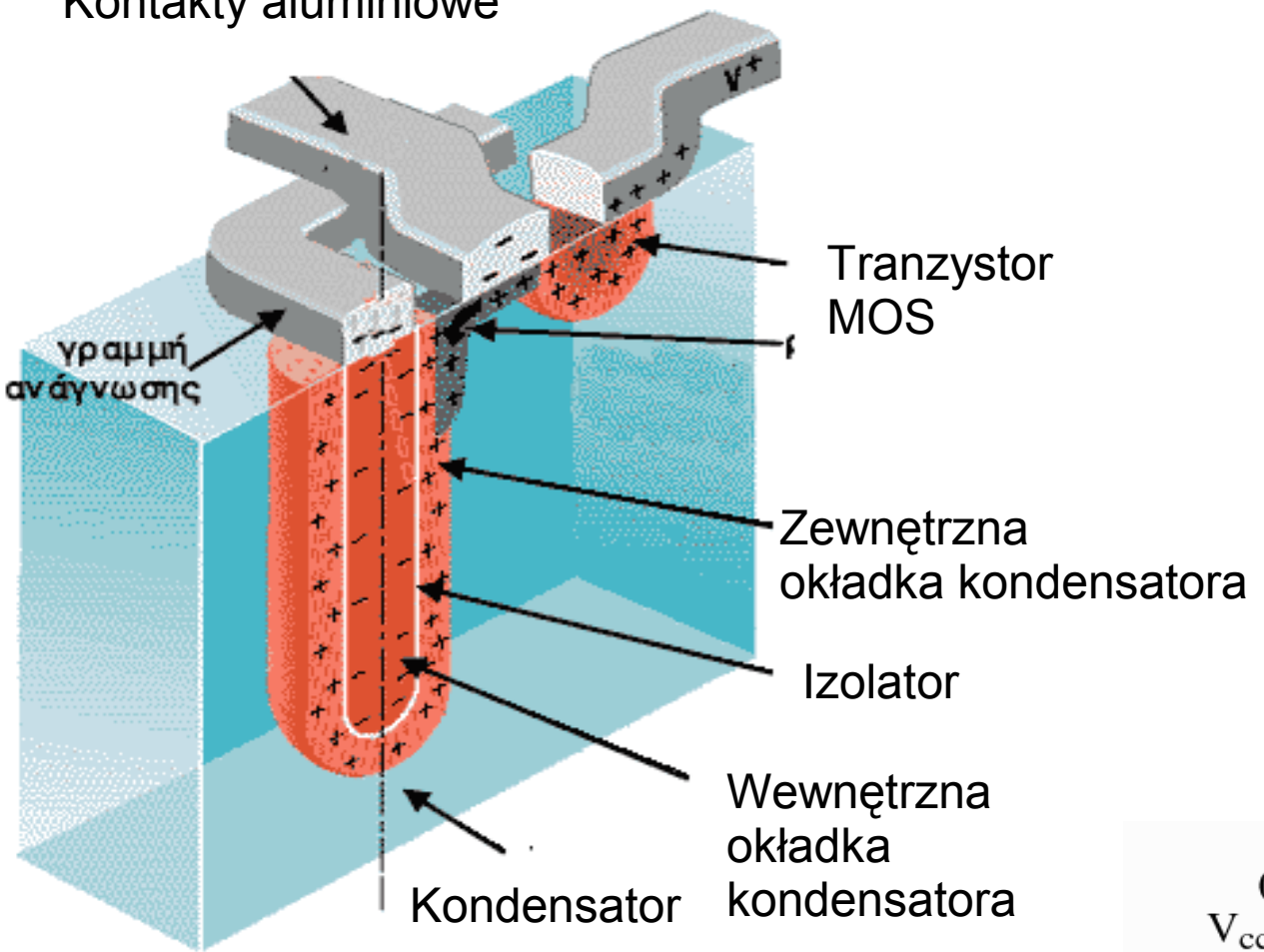
Pamięci statyczne

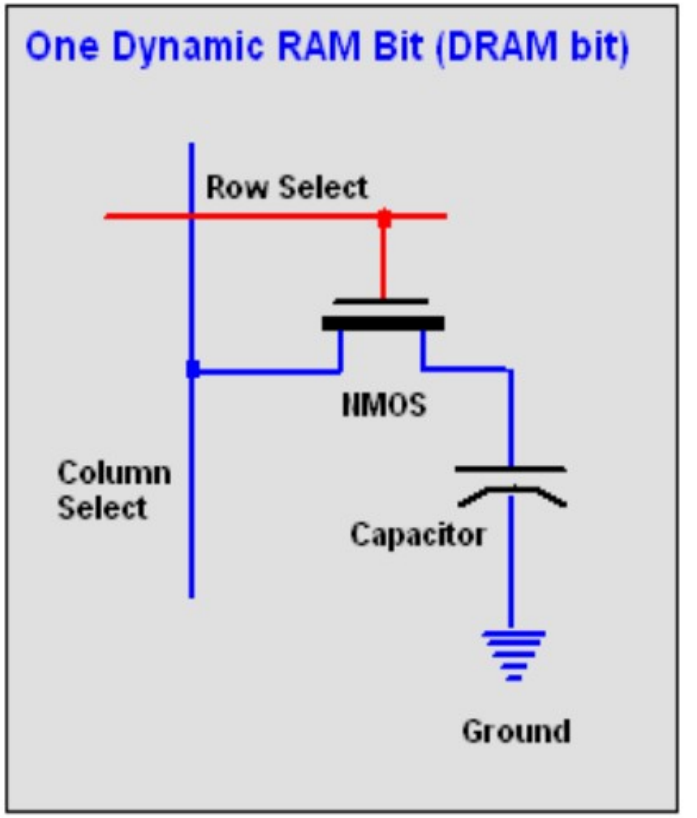


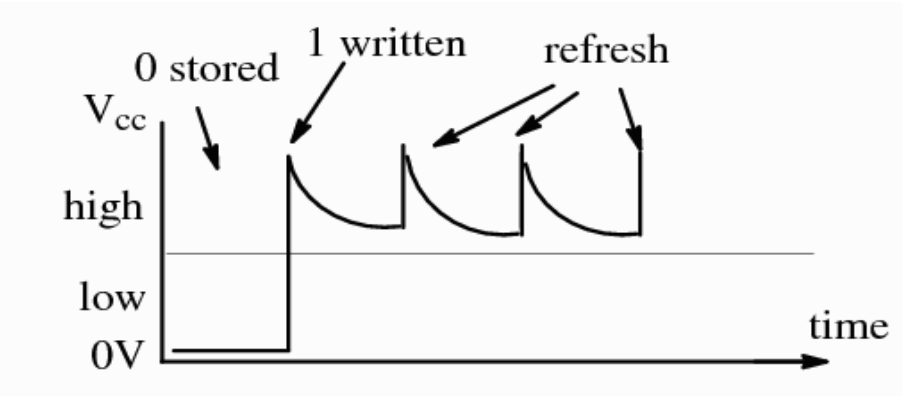
Pamięci dynamiczne DRAM



Komórka pamięci dynamicznej

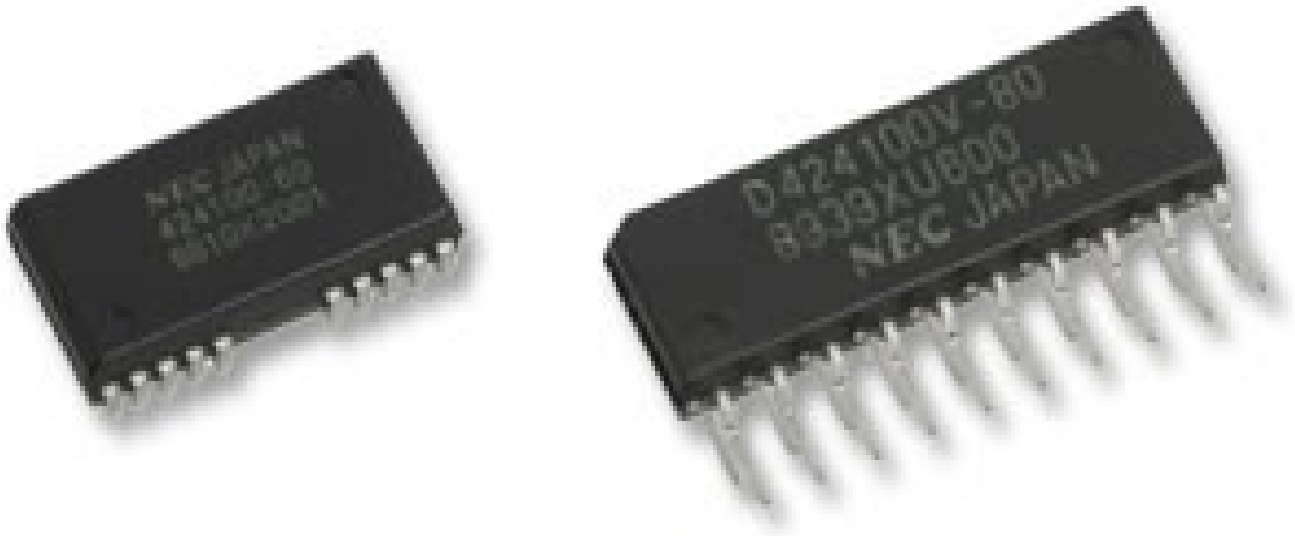


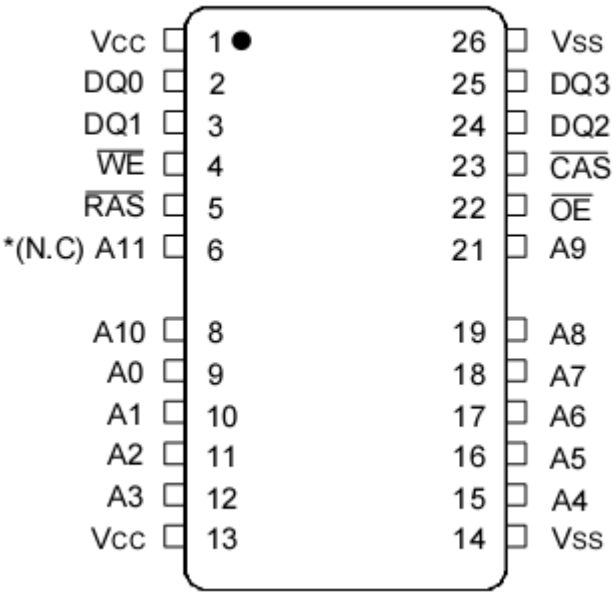




Czas odświeżania: 4 – 16 ms

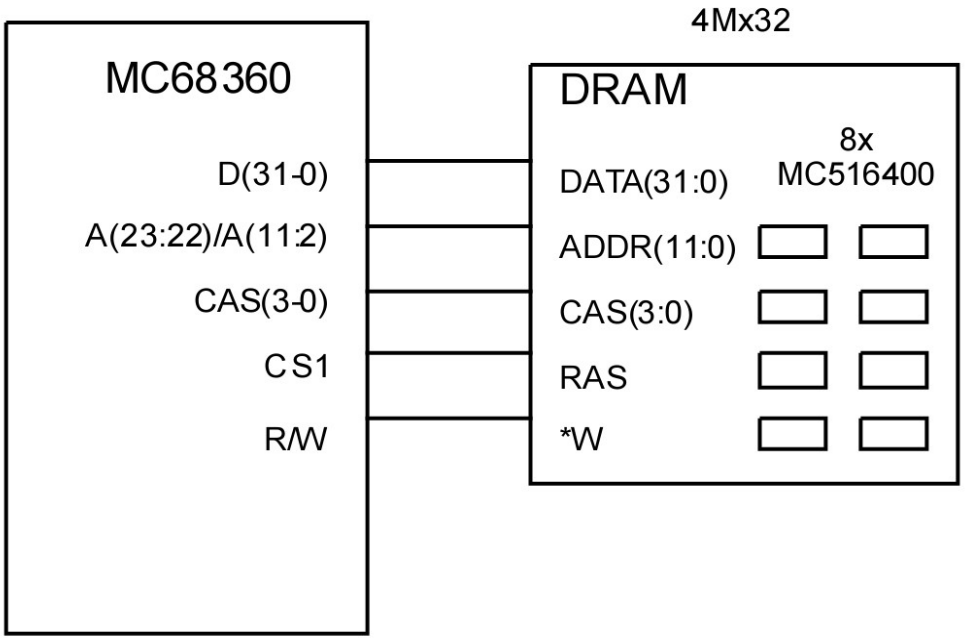
Pamięć DRAM 1 Mx4

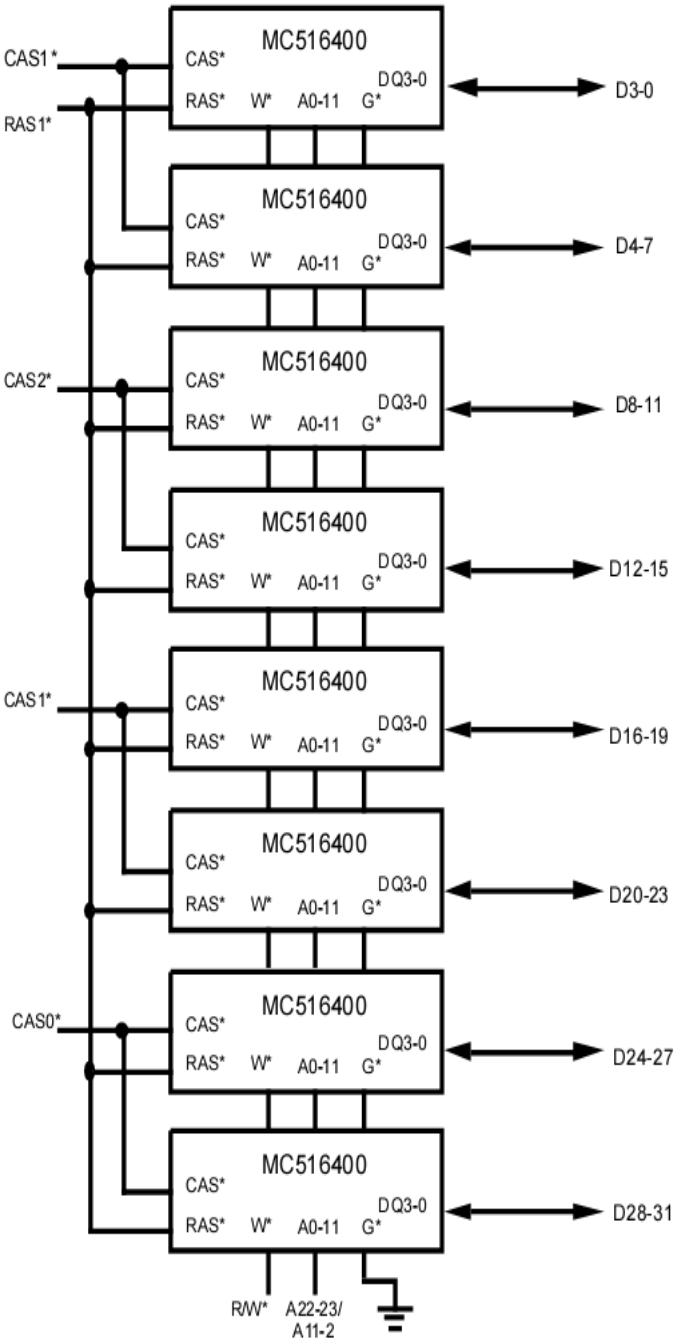




Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A11	Address Input (4K Refresh Product)
A0~A10	Address Input (2K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

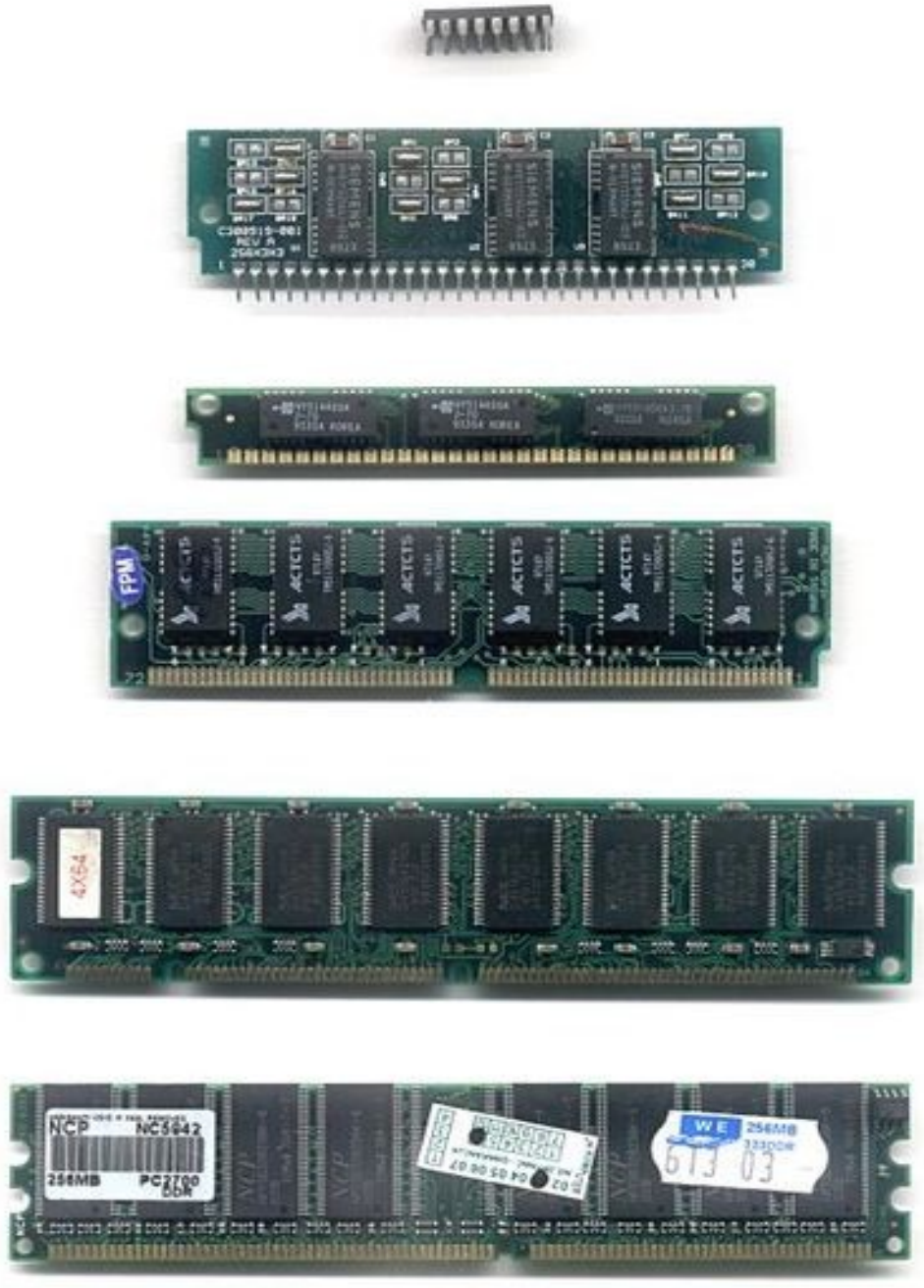
Pamięci 32-bitowe





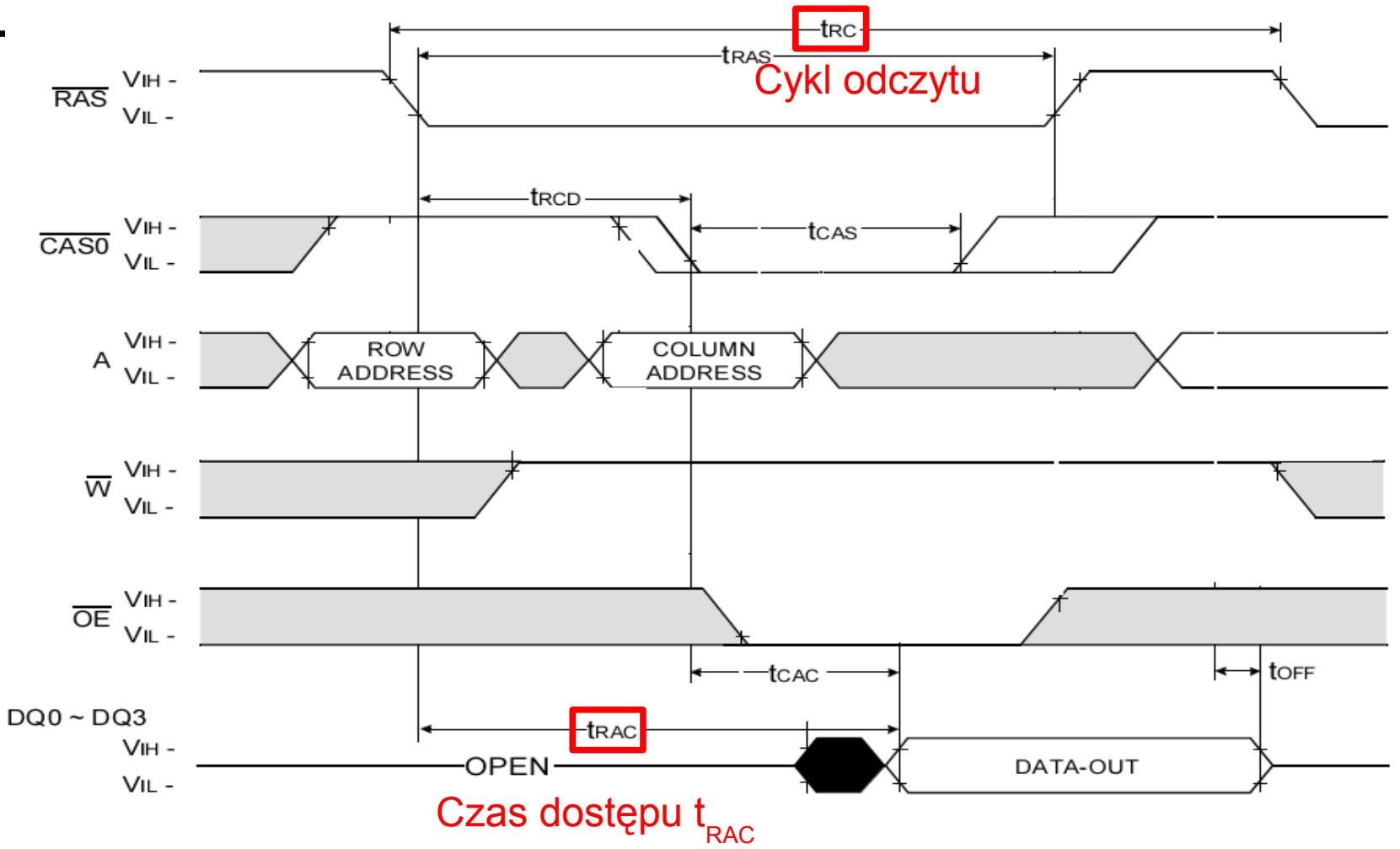
VAX 8600 memory board

Pamięci dynamiczne



Procesor z dwoma pamięciami SDRAM

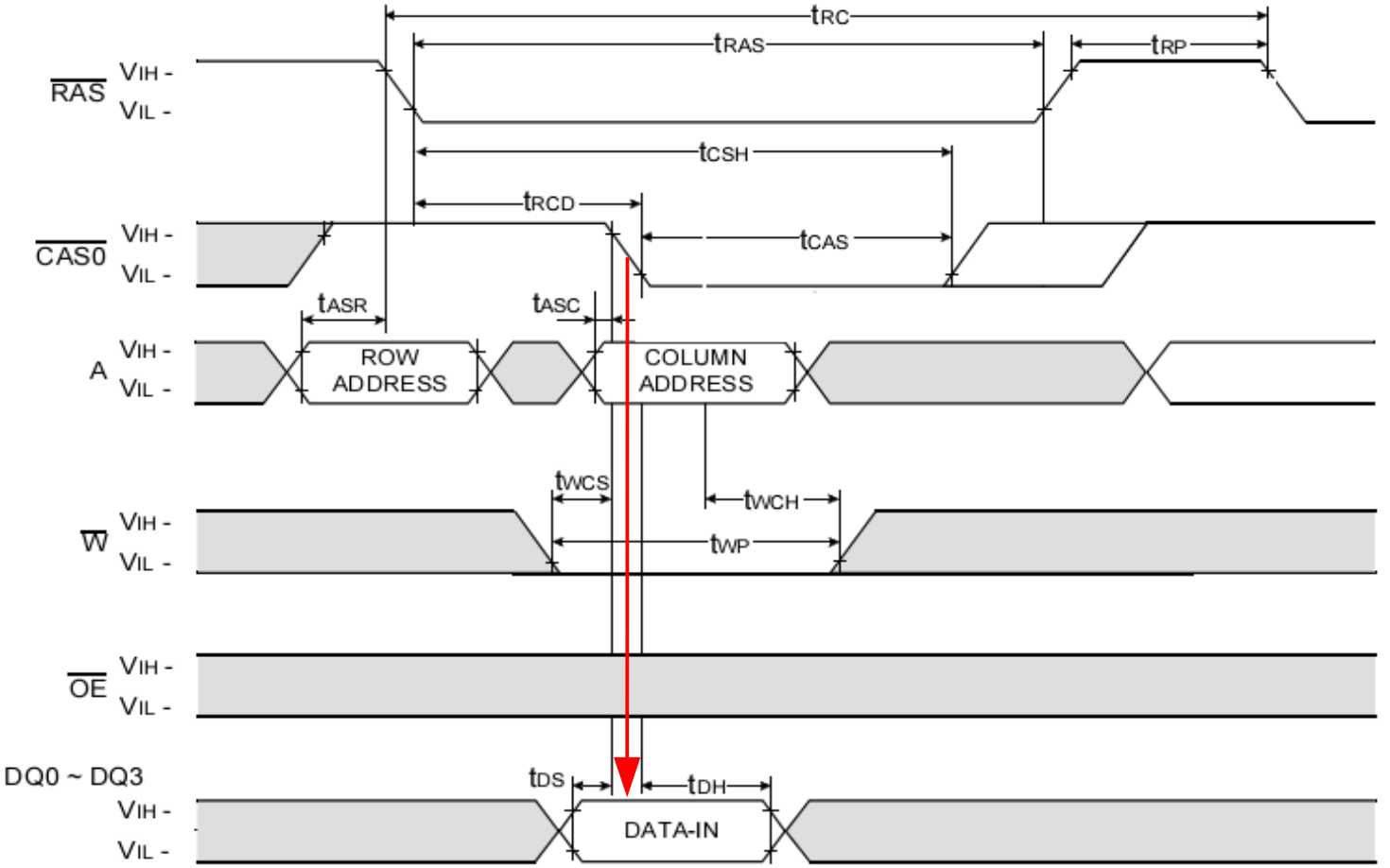
Cykl odczytu z pamięci dynamicznej



Czas dostępu t_{RAC}

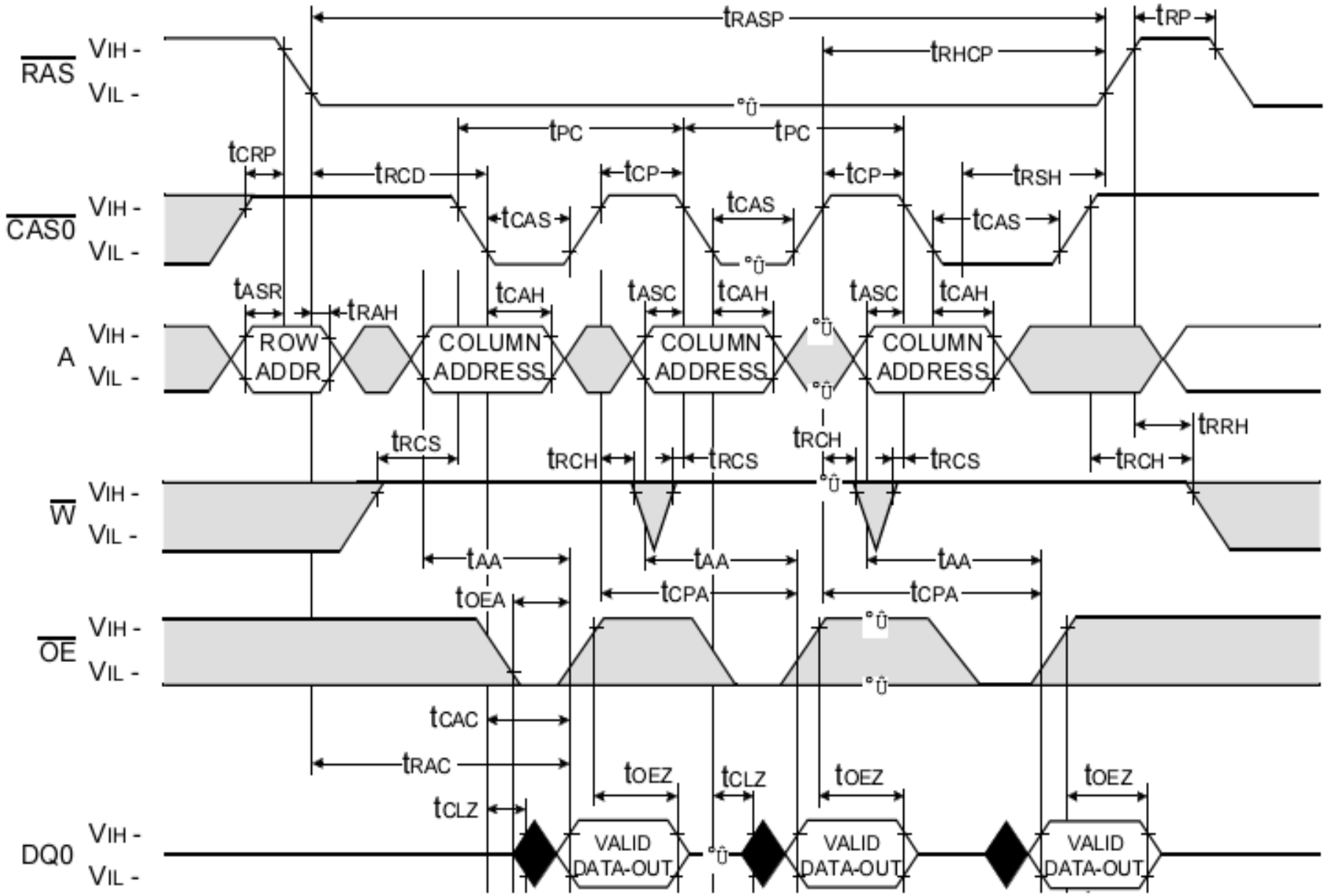
MNEMONIC	SIGNAL NAME	VALUE (ns)
t_{RCD}	Row-to-column strobe lead time	25–75
t_{CAC}	Access time from column address strobe	25 max.
t_{RAC}	Access time from row address strobe	100 max.
t_{OFF}	Output buffer turn off time	0–20

Cykl zapisu do pamięci dynamicznej



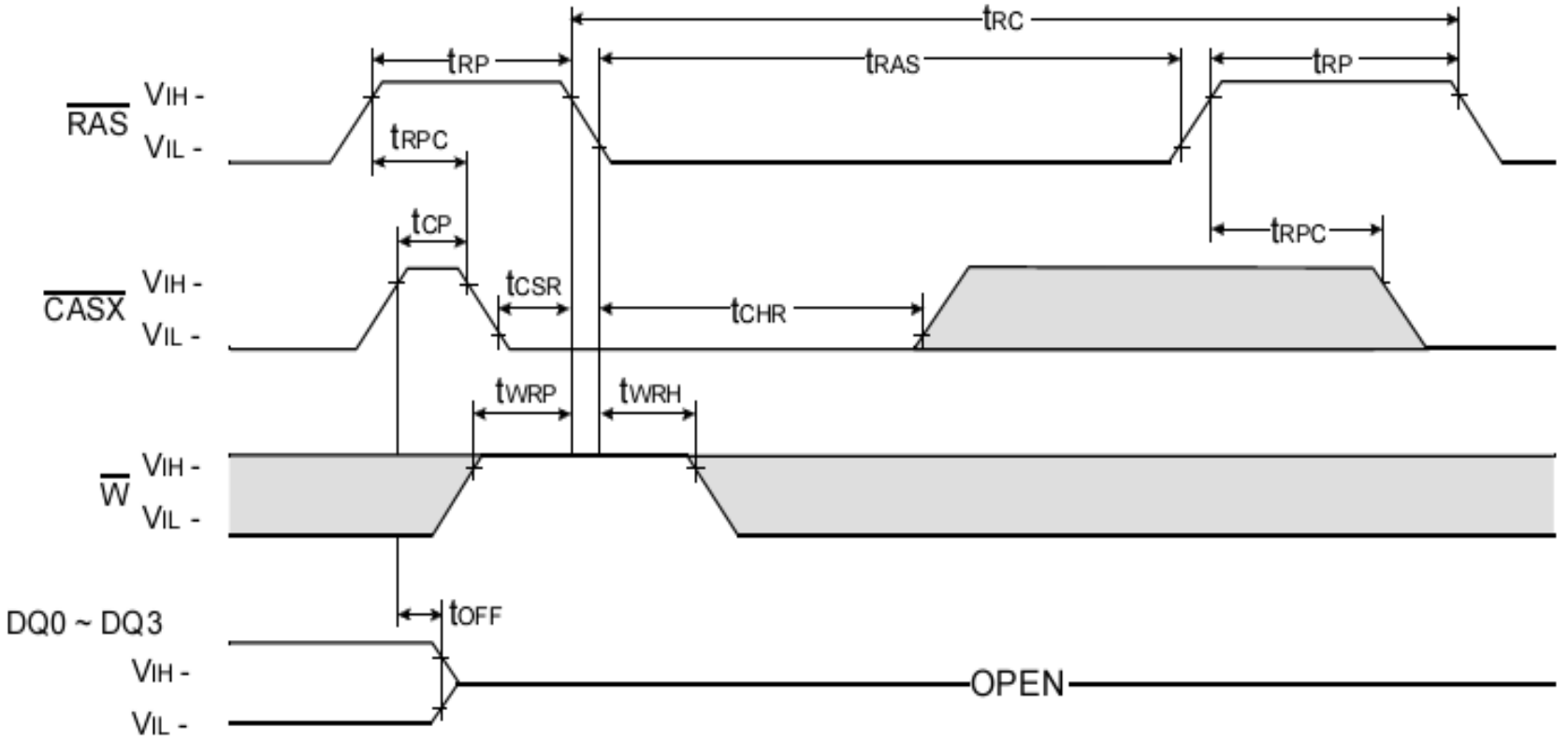
MNEMONIC	NAME	VALUE (ns)
t_{WCS}	Write command setup time	0 min.
t_{WCH}	Write command hold time	20 min.
t_{WP}	Write command pulse width	20 min.
t_{DS}	Data setup time	0 min.
t_{DH}	Data hold time	20 min.

Cykl szybkiego stronicowania (odczyt)



Cykl odświeżania

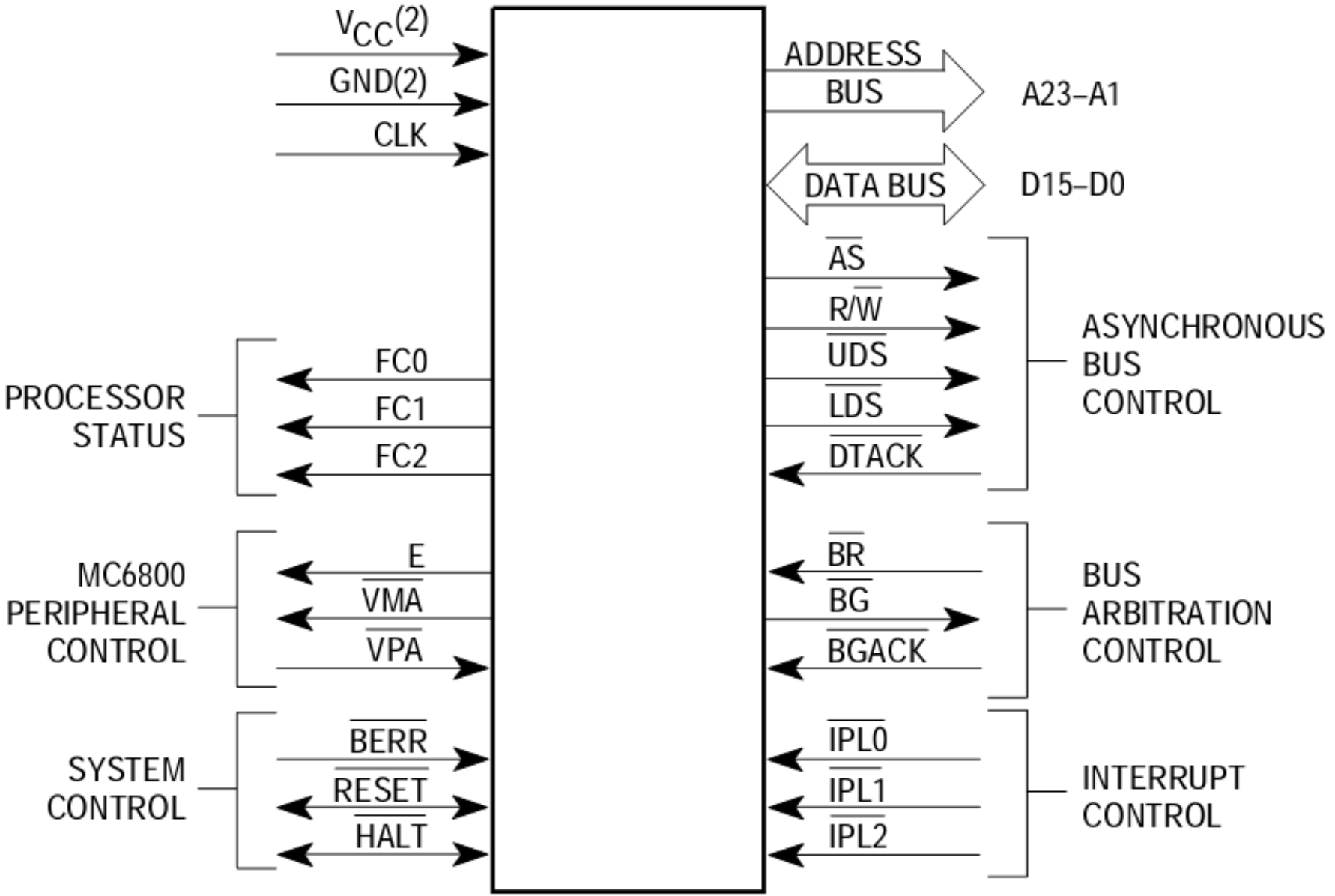
Odświeżanie typu CAS przed RAS



Pamięć MCM54400A-60 (1 Mx4):
Cykl odświeżania: T_R=16 ms, czas dostępu: t_{RAC}=60 ns, cykl odczytu: t_{RC}=110 ns,
Czas potrzebny na odświeżenie 1024 wierszy: 1024 * 110 ns = 113 us (0,7 % cyklu T_R)

Współpraca pocesora rodziny 68k z pamięcią

Motorola MC 68000

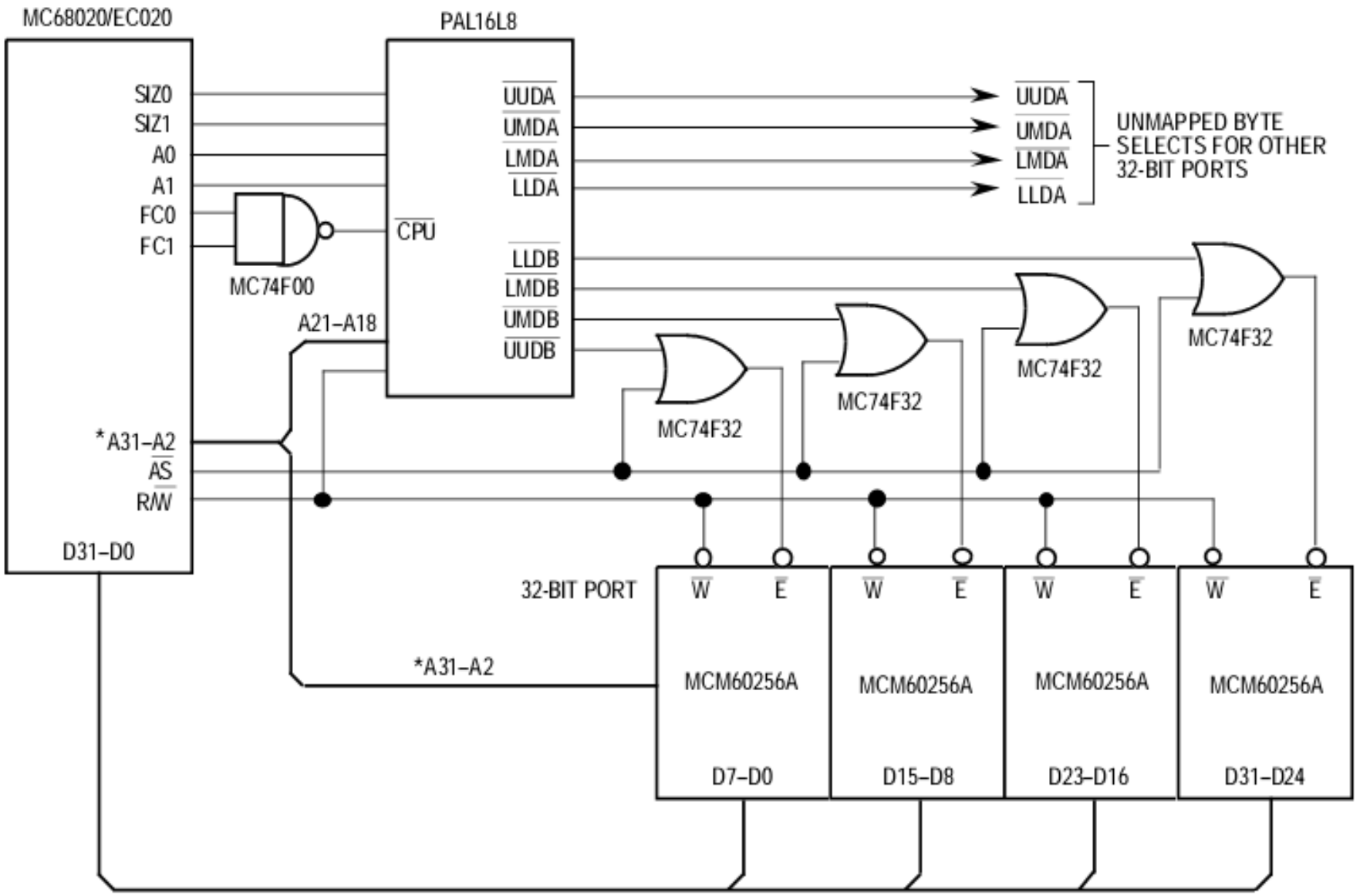


Przestrzenie adresowe procesora Motorola z rodziny 68k

Function Code Output			Address Space Type
FC2	FC1	FC0	
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	CPU Space

CPU space – przestrzeń adresowa procesora (obsługa rejestrów specjalnych RAMBAR, FLASHBAR, konfiguracja pamięci cache, kooprocesor, itp...), instrukcja MOVES

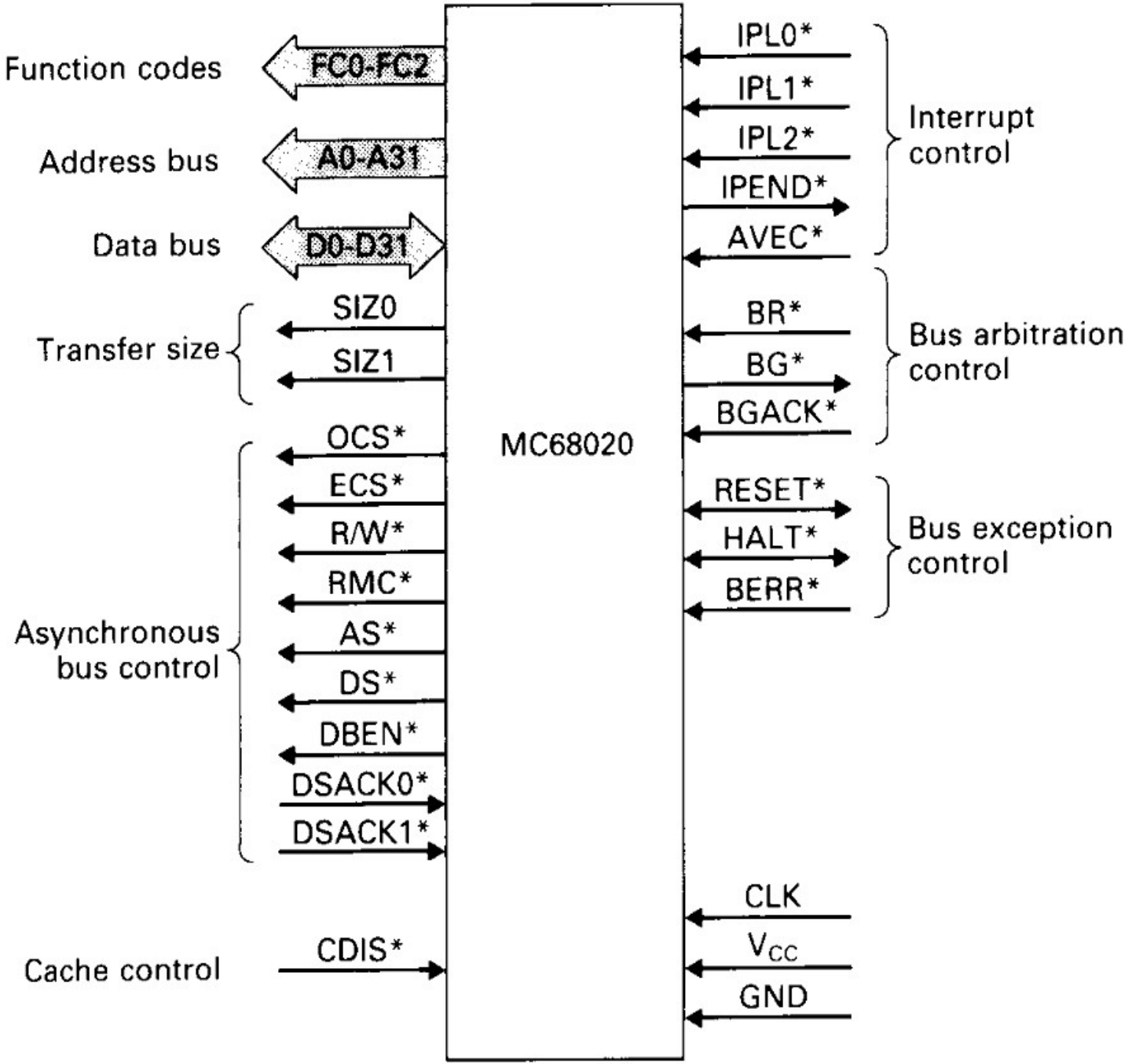
Dekoder adresowy procesora MC68020 - CPU space



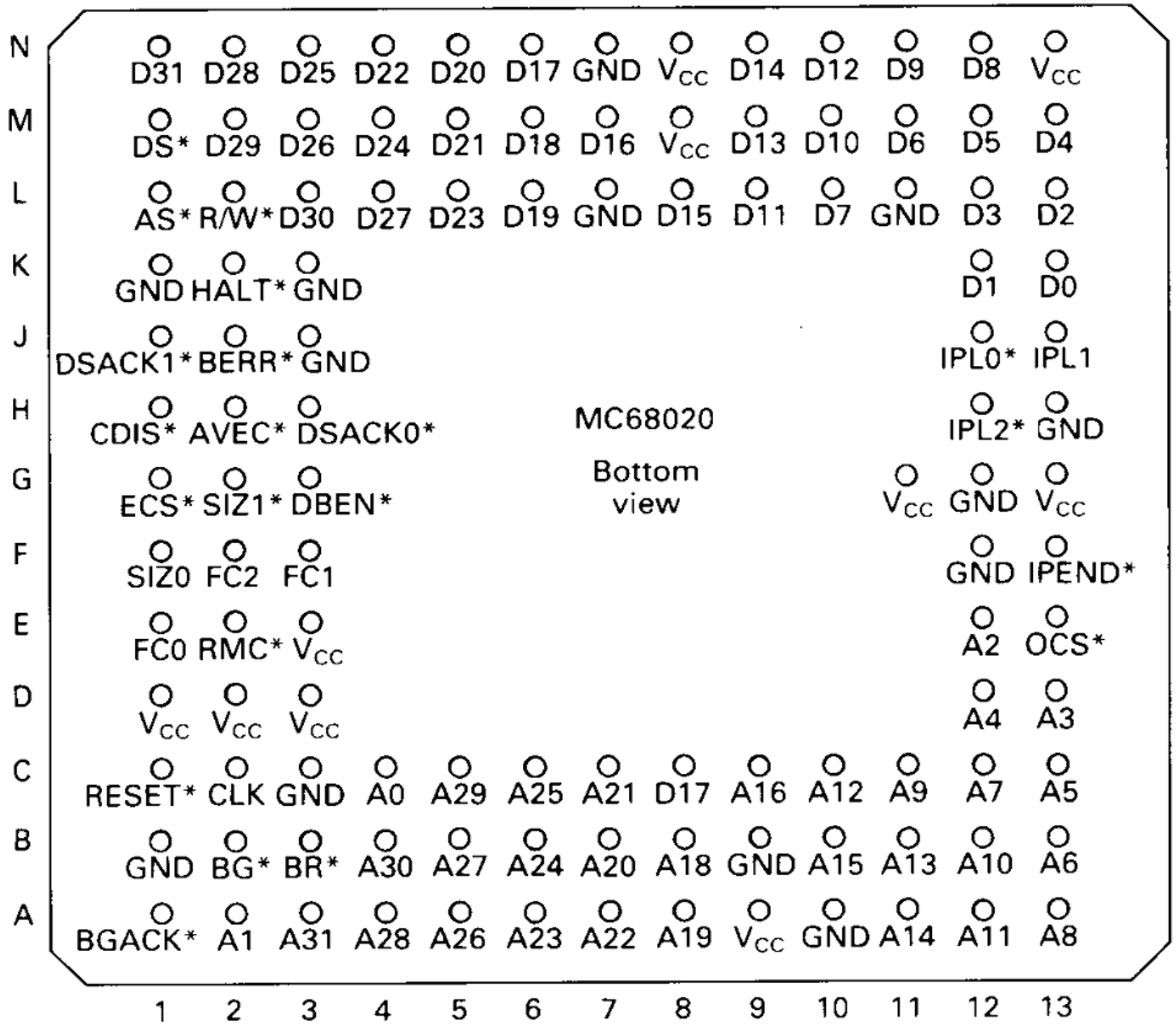
Sygnały procesora Motorola (2)

Signal Name	Mnemonic	Input/Output	Active State	Hi-Z	
				On $\overline{\text{HALT}}$	On Bus Relinquish
Address Bus	A0–A23	Output	High	Yes	Yes
Data Bus	D0–D15	Input/Output	High	Yes	Yes
Address Strobe	$\overline{\text{AS}}$	Output	Low	No	Yes
Read/Write	R/$\overline{\text{W}}$	Output	Read-High Write-Low	No	Yes
Data Strobe	$\overline{\text{DS}}$	Output	Low	No	Yes
Upper and Lower Data Strobes	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{\text{DTACK}}$	Input	Low	No	No
Bus Request	$\overline{\text{BR}}$	Input	Low	No	No
Bus Grant	$\overline{\text{BG}}$	Output	Low	No	No
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	Input	Low	No	No
Interrupt Priority Level	$\overline{\text{IPL}}$0, $\overline{\text{IPL}}$1, $\overline{\text{IPL}}$2	Input	Low	No	No
Bus Error	$\overline{\text{BERR}}$	Input	Low	No	No
Mode	MODE	Input	High	—	—
Reset	$\overline{\text{RESET}}$	Input/Output	Low	No*	No*
Halt	$\overline{\text{HALT}}$	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	$\overline{\text{VMA}}$	Output	Low	No	Yes
Valid Peripheral Address	$\overline{\text{VPA}}$	Input	Low	No	No
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Power Input	V_{CC}	Input	—	—	—
Ground	GND	Input	—	—	—

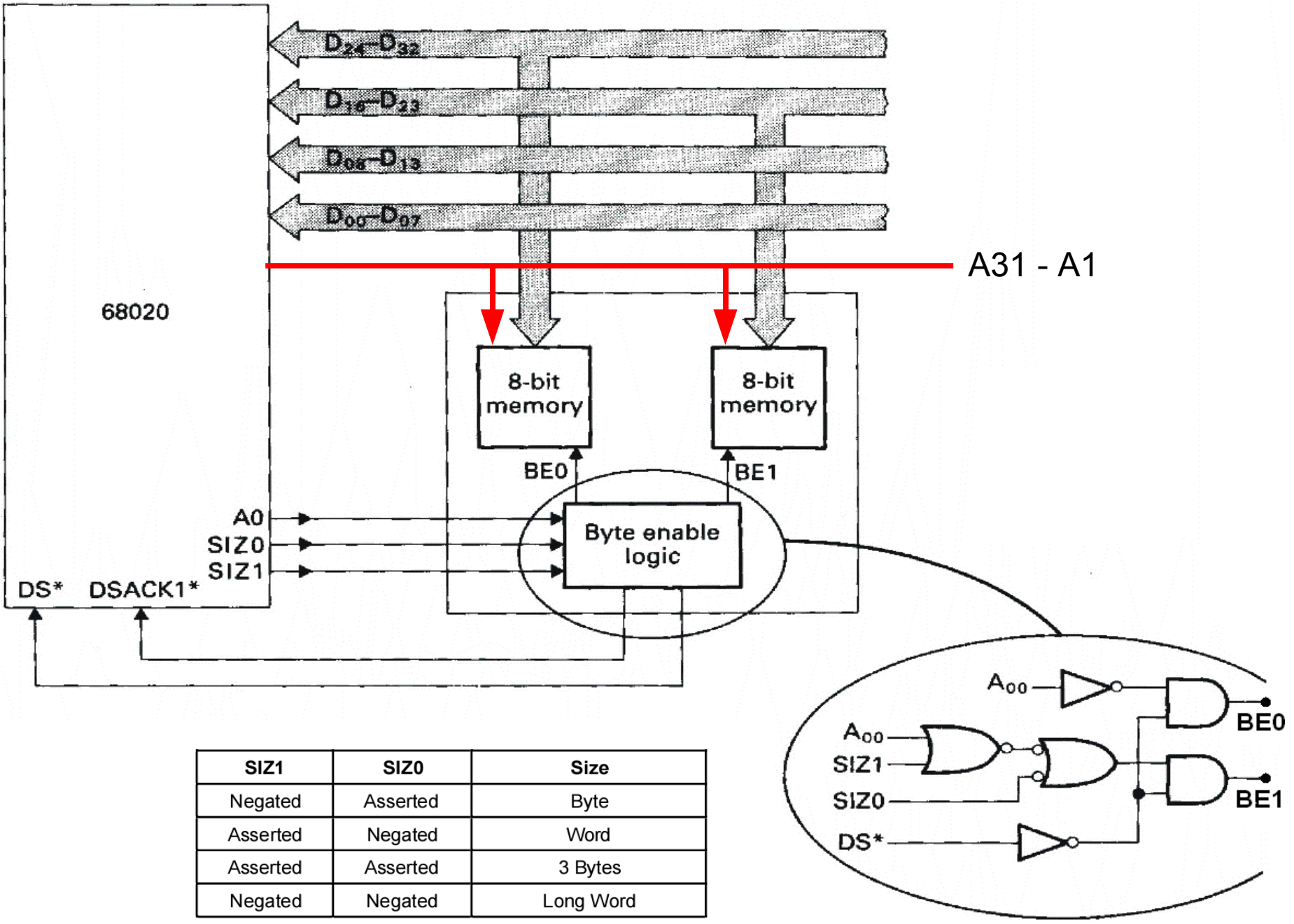
Motorola MC 68020



Obudowa procesora MC 68020

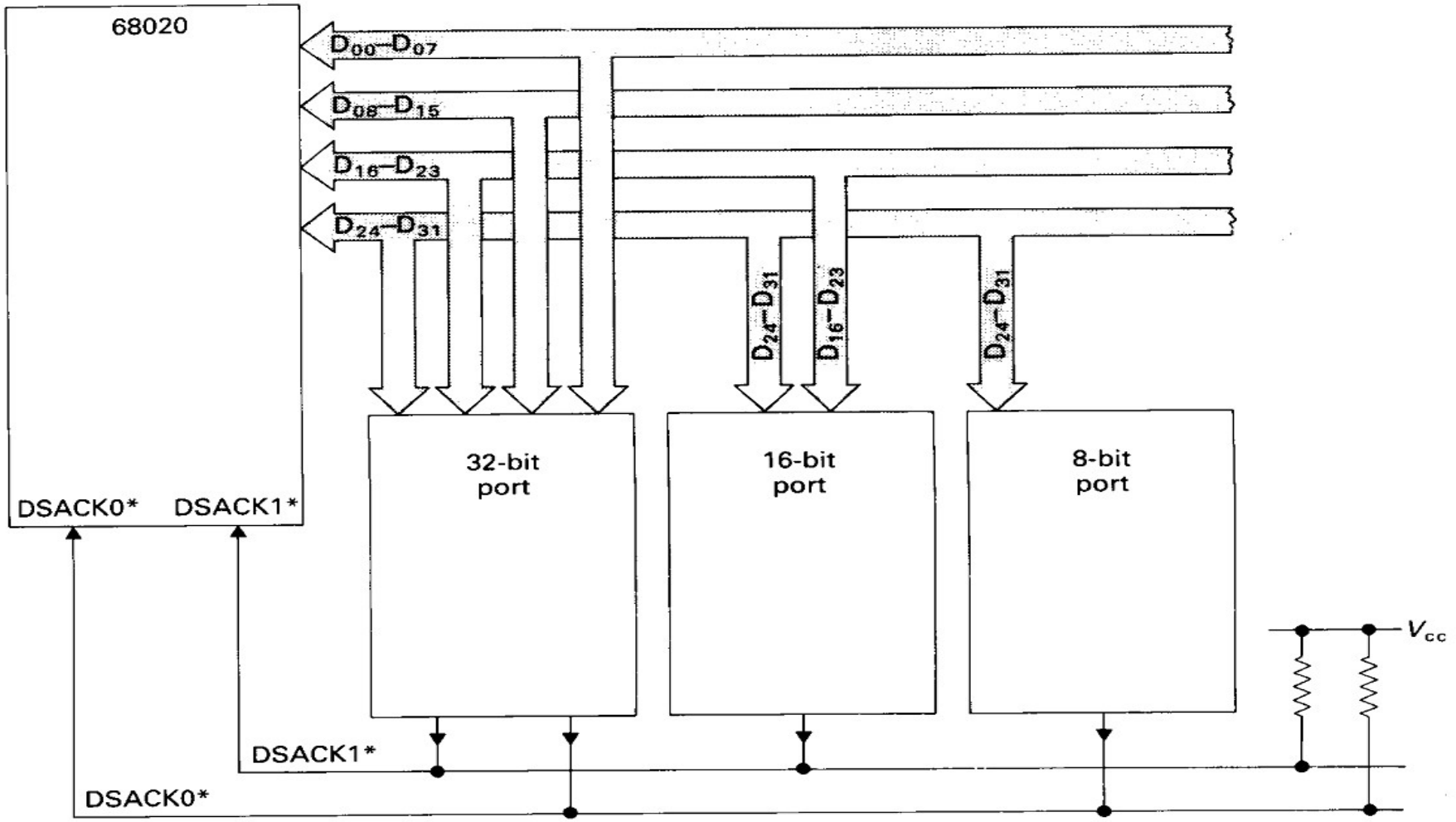


Współpraca procesora 68020 z pamięcią z magistralą 16 bitową



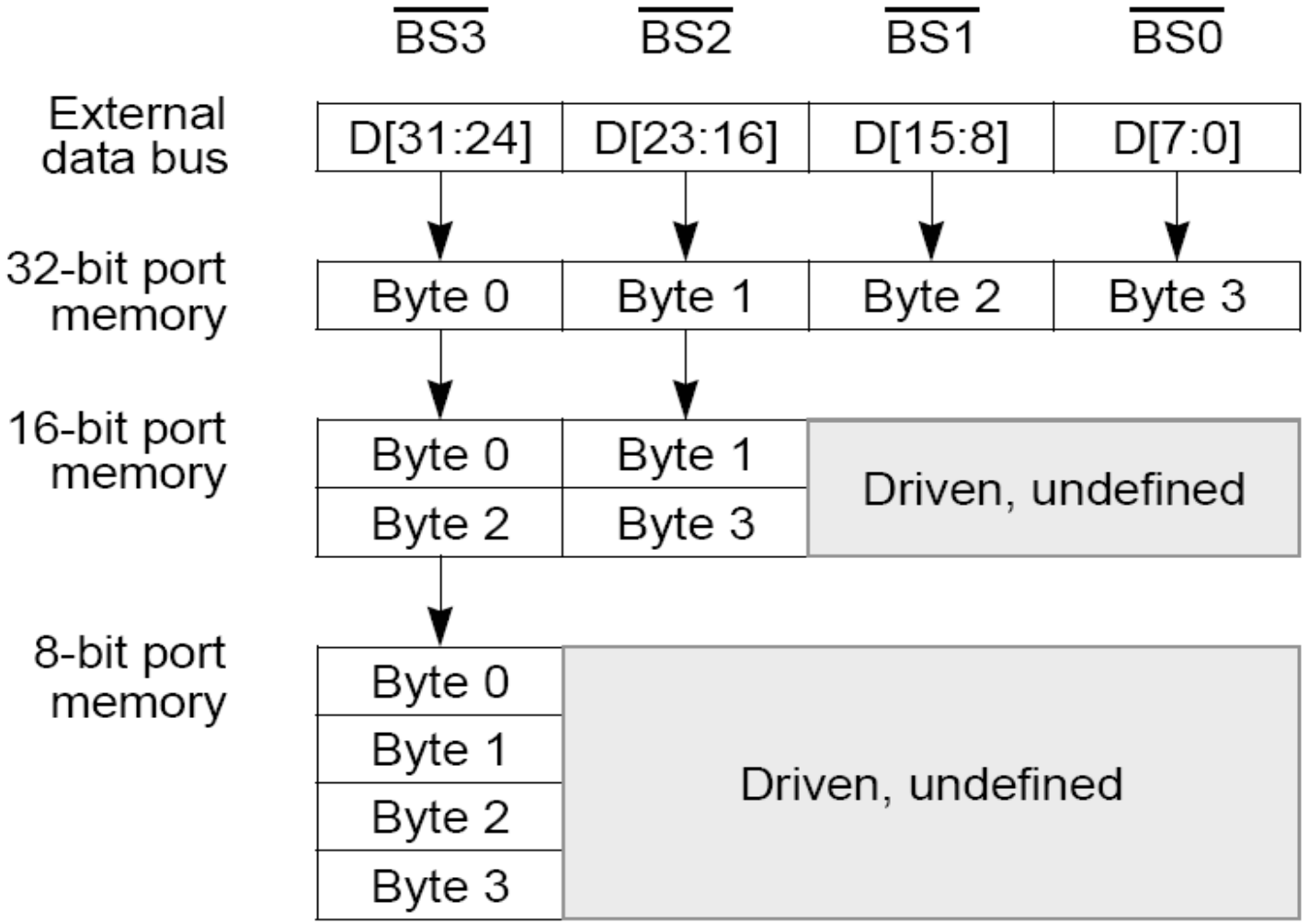
SIZ1	SIZ0	Size
Negated	Asserted	Byte
Asserted	Negated	Word
Asserted	Asserted	3 Bytes
Negated	Negated	Long Word

Współpraca procesora z urządzeniami o różnych magistralach danych



DSACK1*	DSACK0*	INTERPRETATION
1	1	No data acknowledge—insert wait states.
1	0	Data acknowledge—data bus port size is 8 bits.
0	1	Data acknowledge—data bus port size is 16 bits.
0	0	Data acknowledge—data bus port size is 32 bits.

Transfery danych procesora motorola



Dynamic Bus Sizing

A1	A0	Offset
Negated	Negated	+0 Bytes
Negated	Asserted	+1 Byte
Asserted	Negated	+2 Bytes
Asserted	Asserted	+3 Bytes

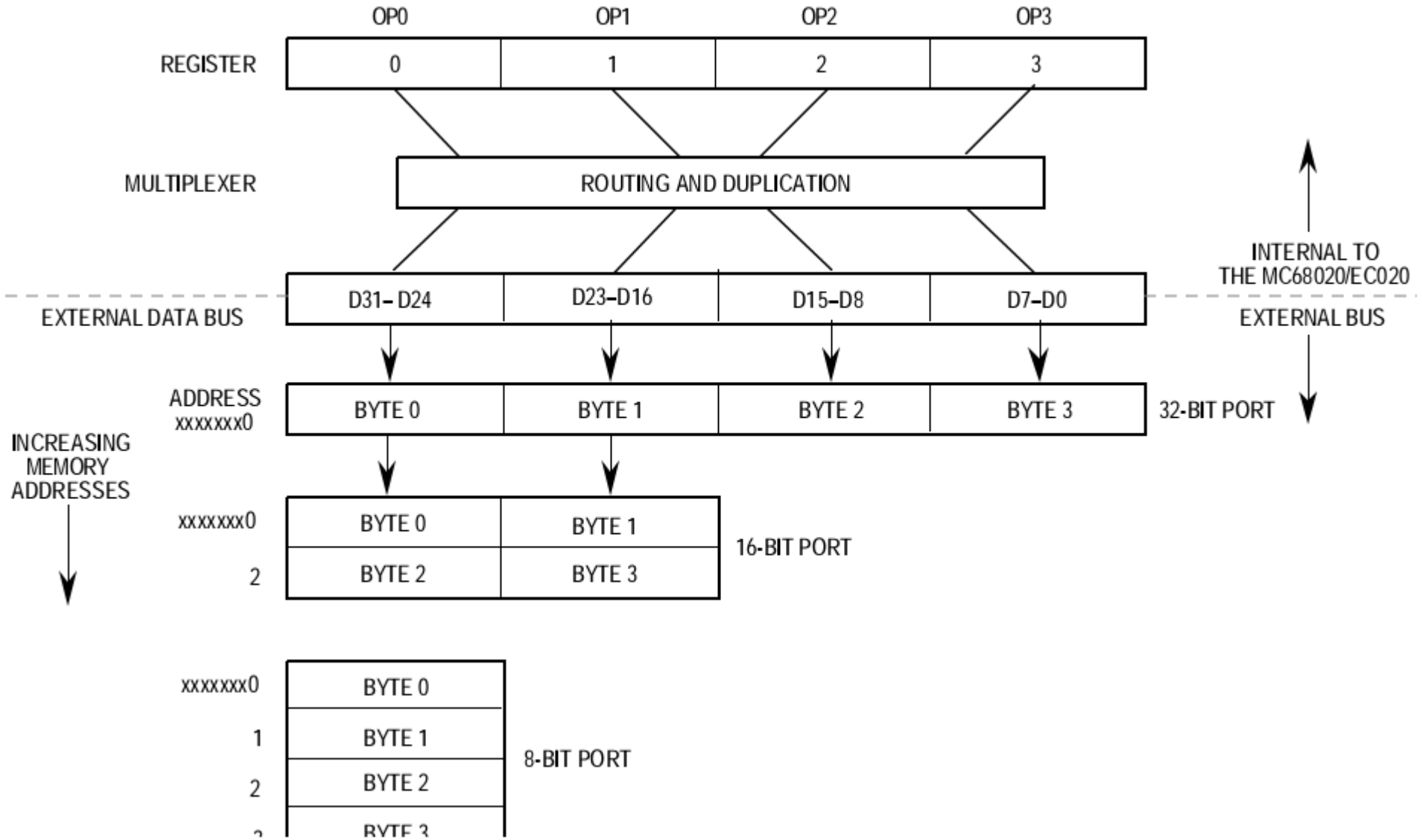
SIZ1	SIZ0	Size
Negated	Asserted	Byte
Asserted	Negated	Word
Asserted	Asserted	3 Bytes
Negated	Negated	Long Word

DSACK1*	DSACK0*	INTERPRETATION
1	1	No data acknowledge—insert wait states.
1	0	Data acknowledge—data bus port size is 8 bits.
0	1	Data acknowledge—data bus port size is 16 bits.
0	0	Data acknowledge—data bus port size is 32 bits.

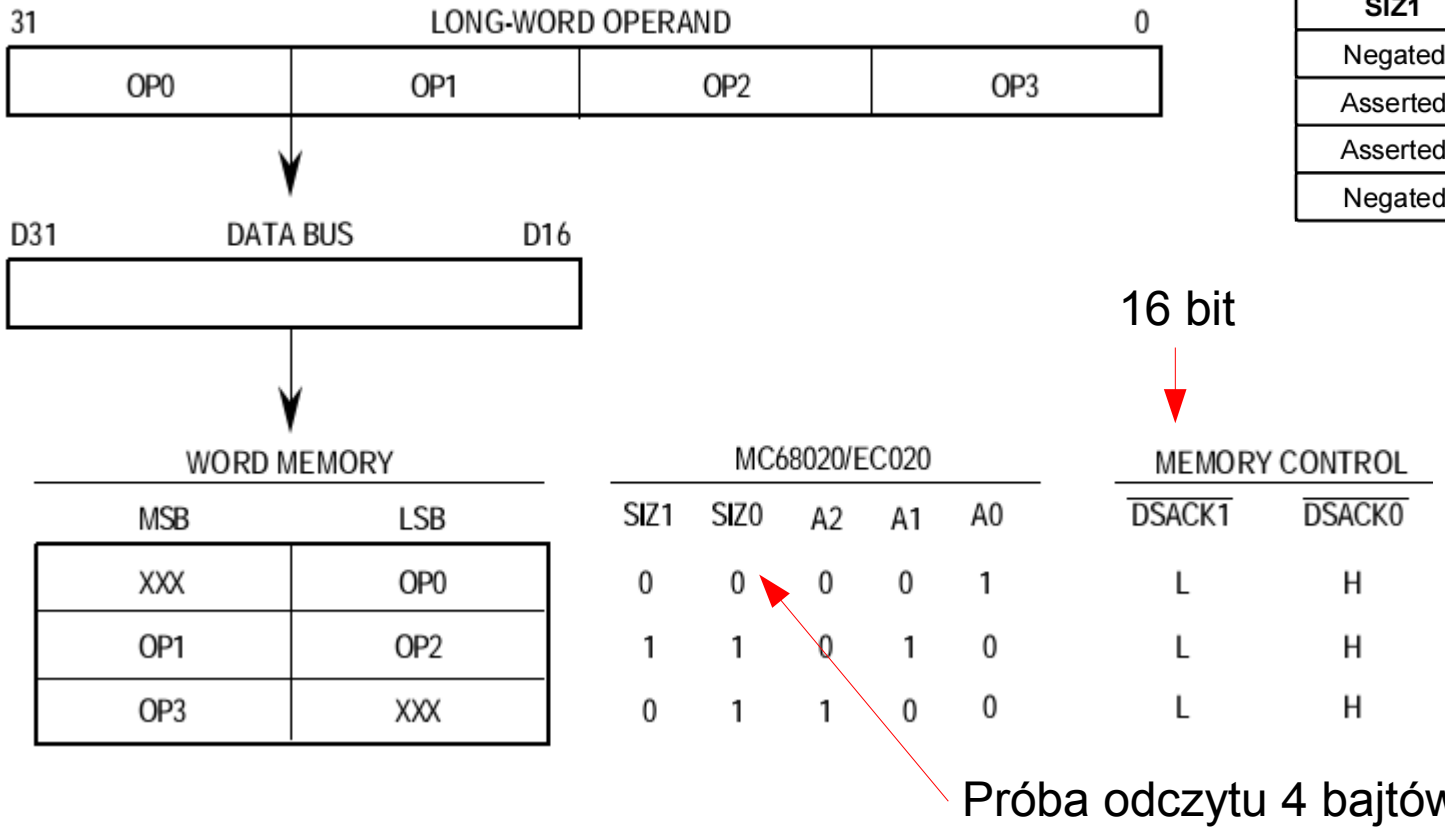
Zależności pomiędzy ilością przesyłanych bajtów, a magistralą

Transfer Size	Size		Address		Long-Word Port External Data Bytes Required				Word Port External Data Bytes Required		Byte Port External Data Bytes Required
	SIZ1	SIZ0	A1	A0	D31–D24	D23–D16	D15–D8	D7–D0	D31–D24	D23–D16	D31–D24
Byte	0	1	0	0	OP3				OP3		OP3
	0	1	0	1		OP3				OP3	OP3
	0	1	1	0			OP3		OP3		OP3
	0	1	1	1				OP3		OP3	OP3
Word	1	0	0	0	OP2	OP3			OP2	OP3	OP2
	1	0	0	1		OP2	OP3			OP2	OP2
	1	0	1	0			OP2	OP3	OP2	OP3	OP2
	1	0	1	1				OP2		OP2	OP2
3 Bytes	1	1	0	0	OP1	OP2	OP3		OP1	OP2	OP1
	1	1	0	1		OP1	OP2	OP3		OP1	OP1
	1	1	1	0			OP1	OP2	OP1	OP2	OP1
	1	1	1	1				OP1		OP1	OP1
Long Word	0	0	0	0	OP0	OP1	OP2	OP3	OP0	OP1	OP0
	0	0	0	1		OP0	OP1	OP2		OP0	OP0
	0	0	1	0			OP0	OP1	OP0	OP1	OP0
	0	0	1	1				OP0		OP0	OP0

Dynamic Bus Sizing



Transfer danej spod nieparzystego adresu przez 16-bitową magistralę

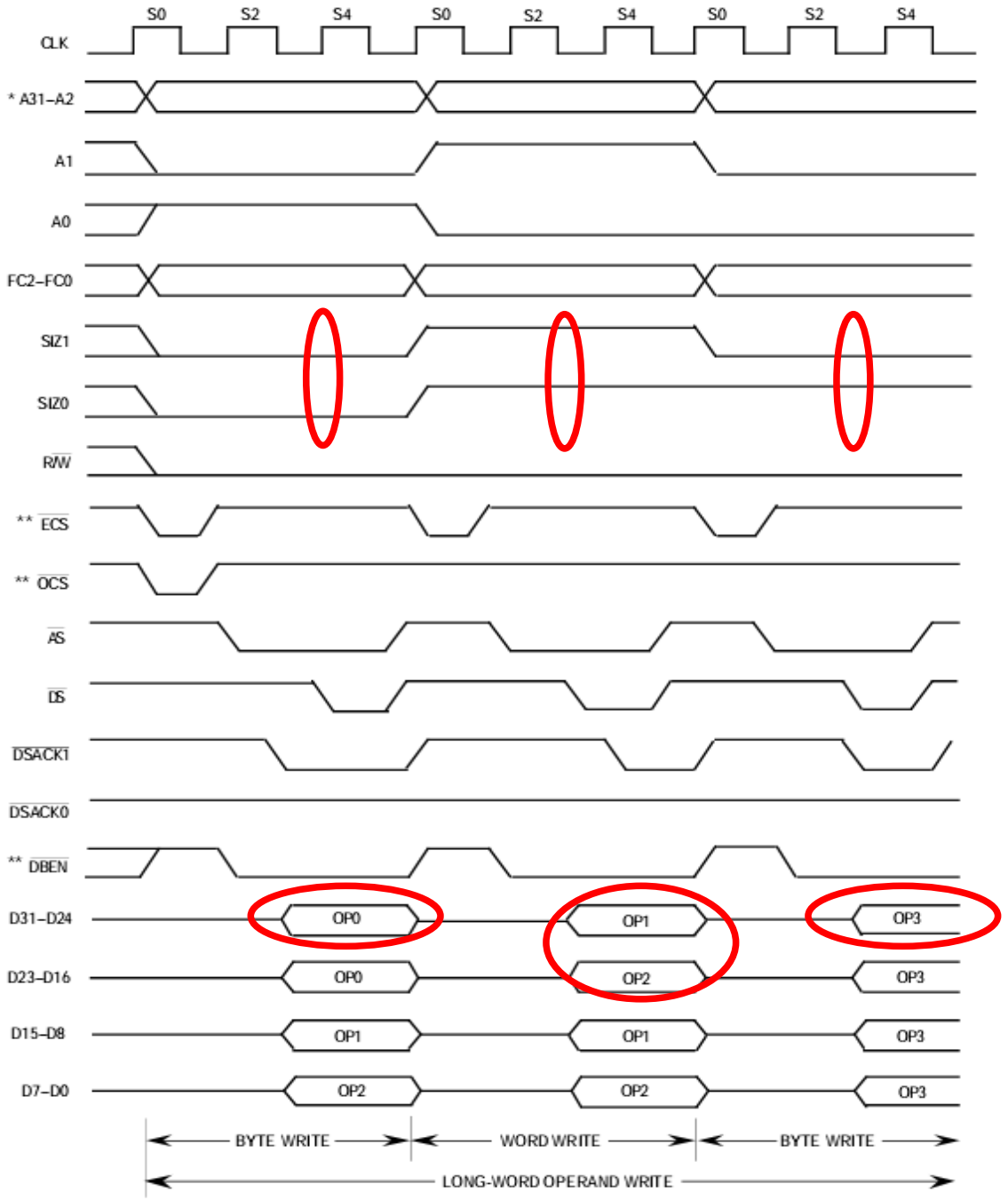


SIZ1	SIZ0	Size
Negated	Asserted	Byte
Asserted	Negated	Word
Asserted	Asserted	3 Bytes
Negated	Negated	Long Word

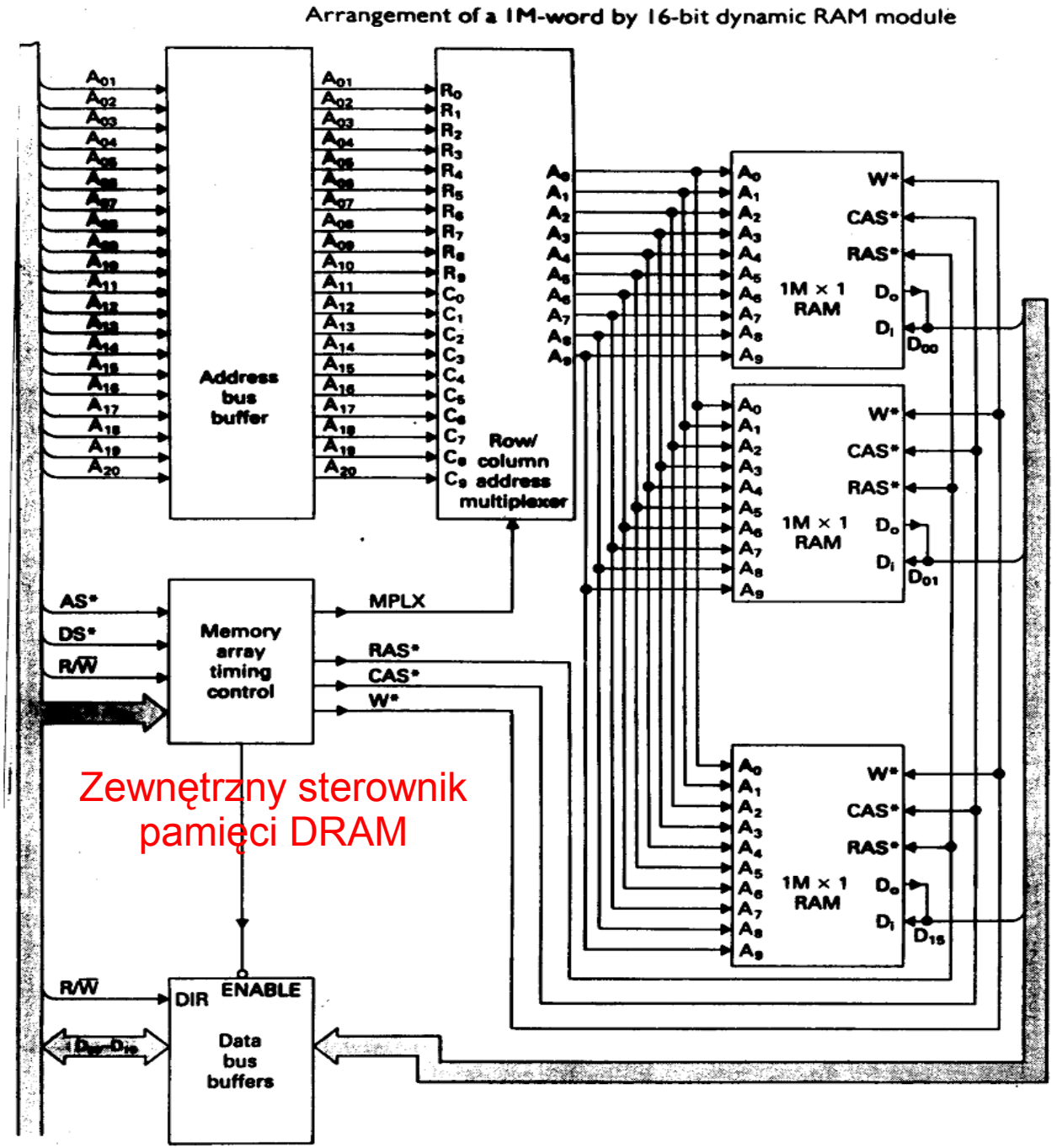
Próba odczytu rozkazu umieszczonego pod nieparzystym adresem w pamięci programu powoduje wystąpienie wyjątku (Address Error Exception).

Rozwiązanie problemu:
Rozkazy powinny być wyrównane do granicy 2 bajtów lub 4 bajtów (dyrektywa asemblera ALIGN).

Przebiegi obrazujące zapis danych pod nieparzysty adres



Współpraca pamięci DRAM z procesorem 68k

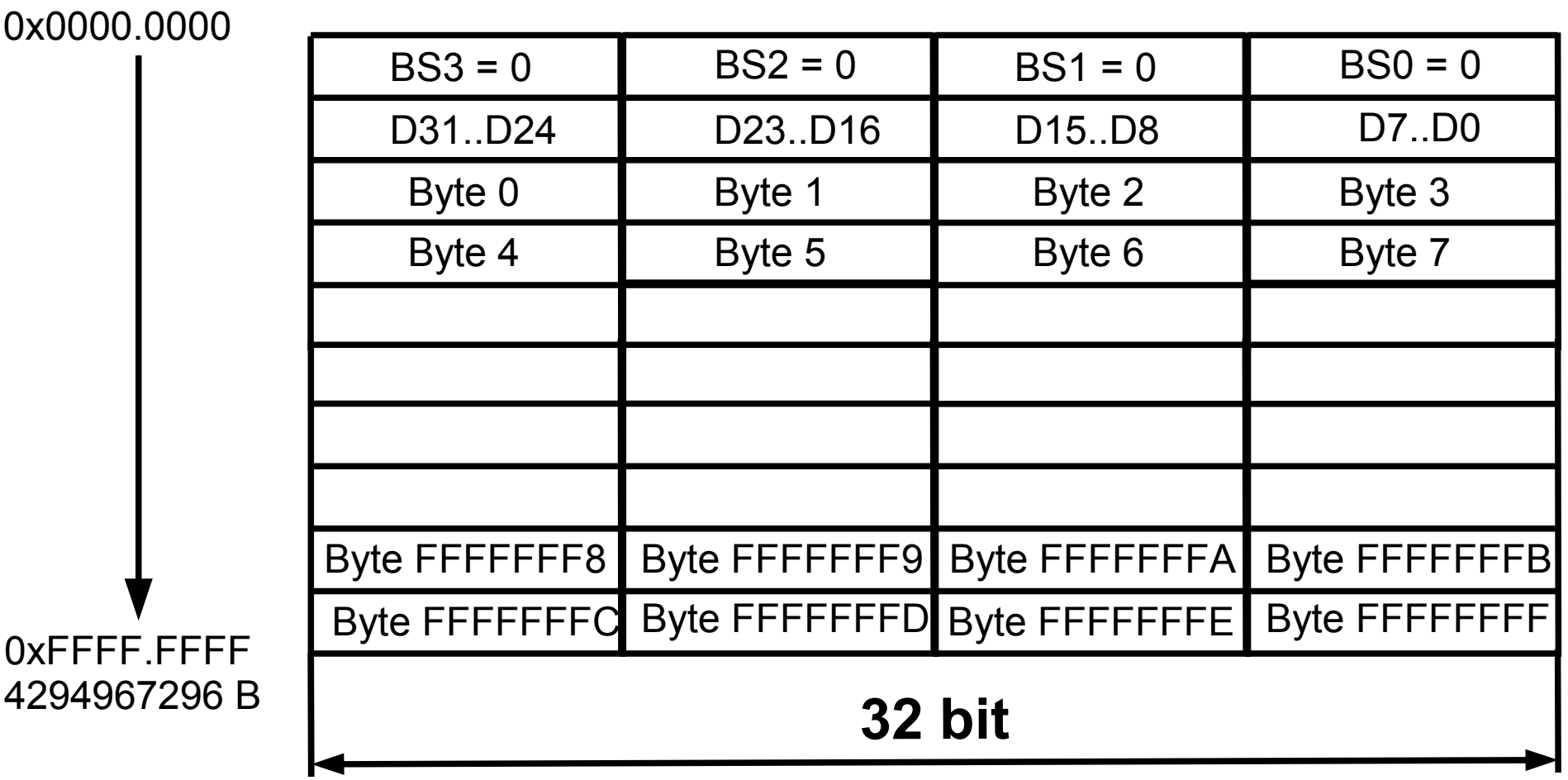


Address strobe
Data strobe
Read/Write

Zewnętrzny sterownik pamięci DRAM

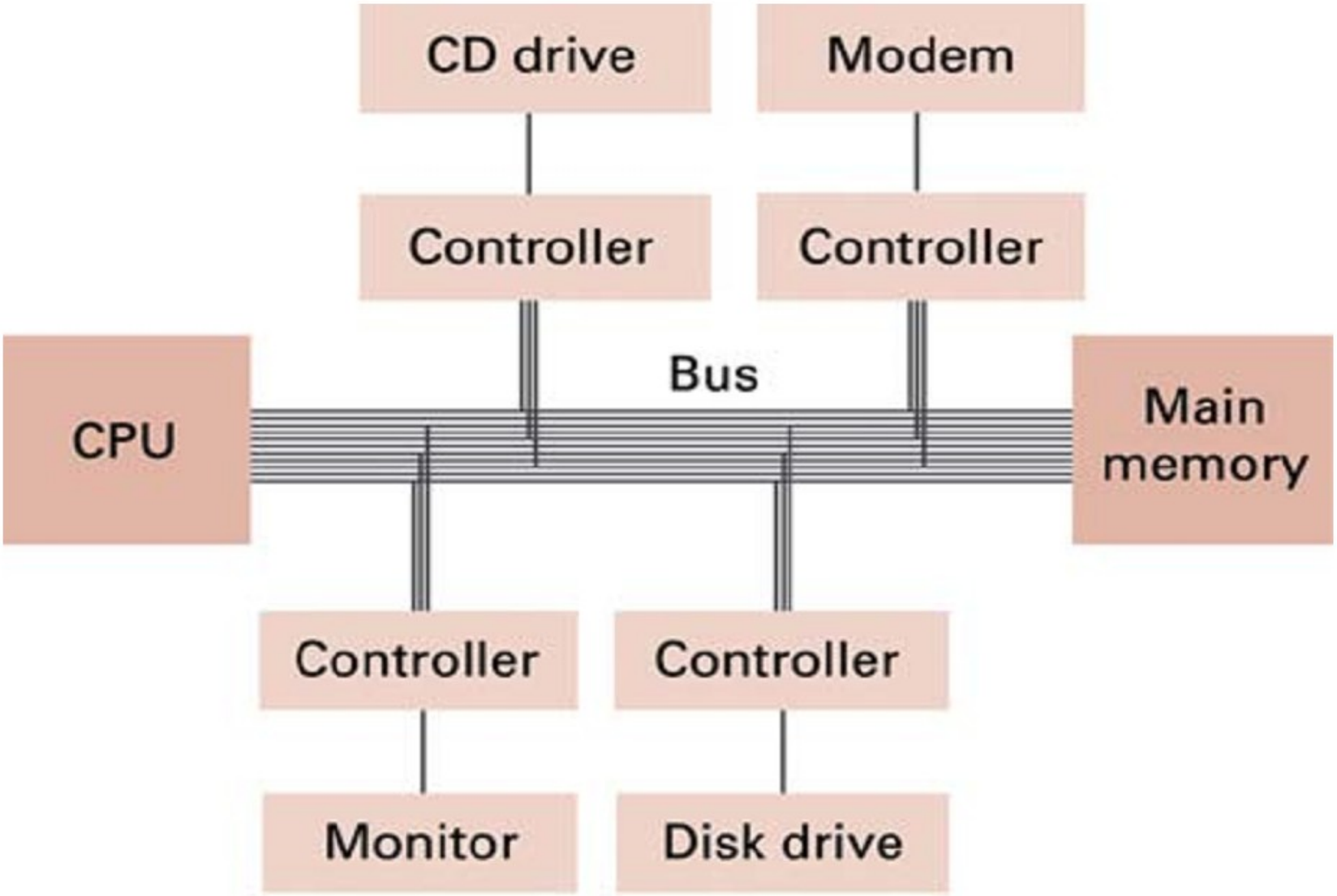
Współpraca pocesora rodziny ColdFire z pamięcią

Przestrzeń adresowa procesora ColdFire

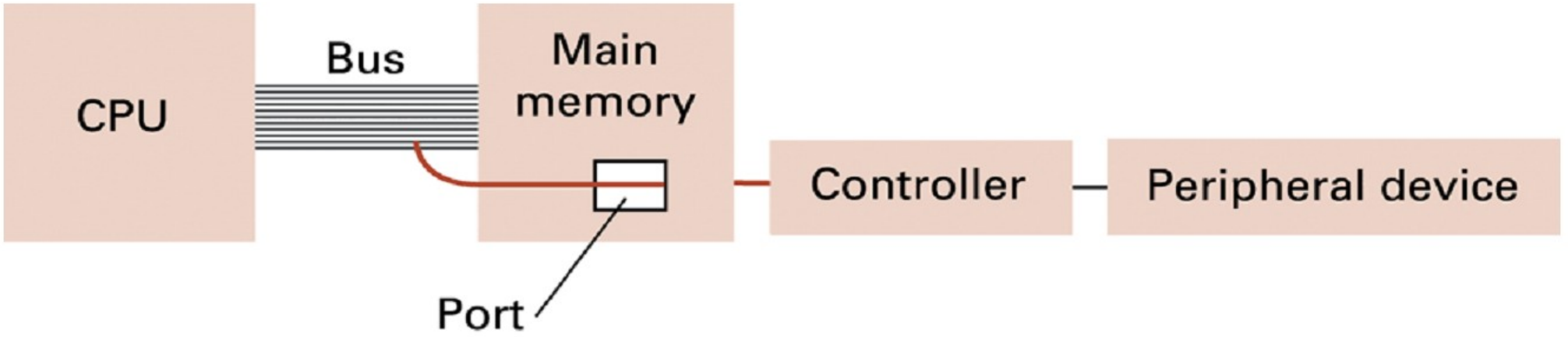


2^32 = 2 G words = 4 G bytes

Współpraca urządzeń peryferyjnych z pamięcią i procesorem



Urządzenia peryferyjne mapowane na przestrzeń pamięci

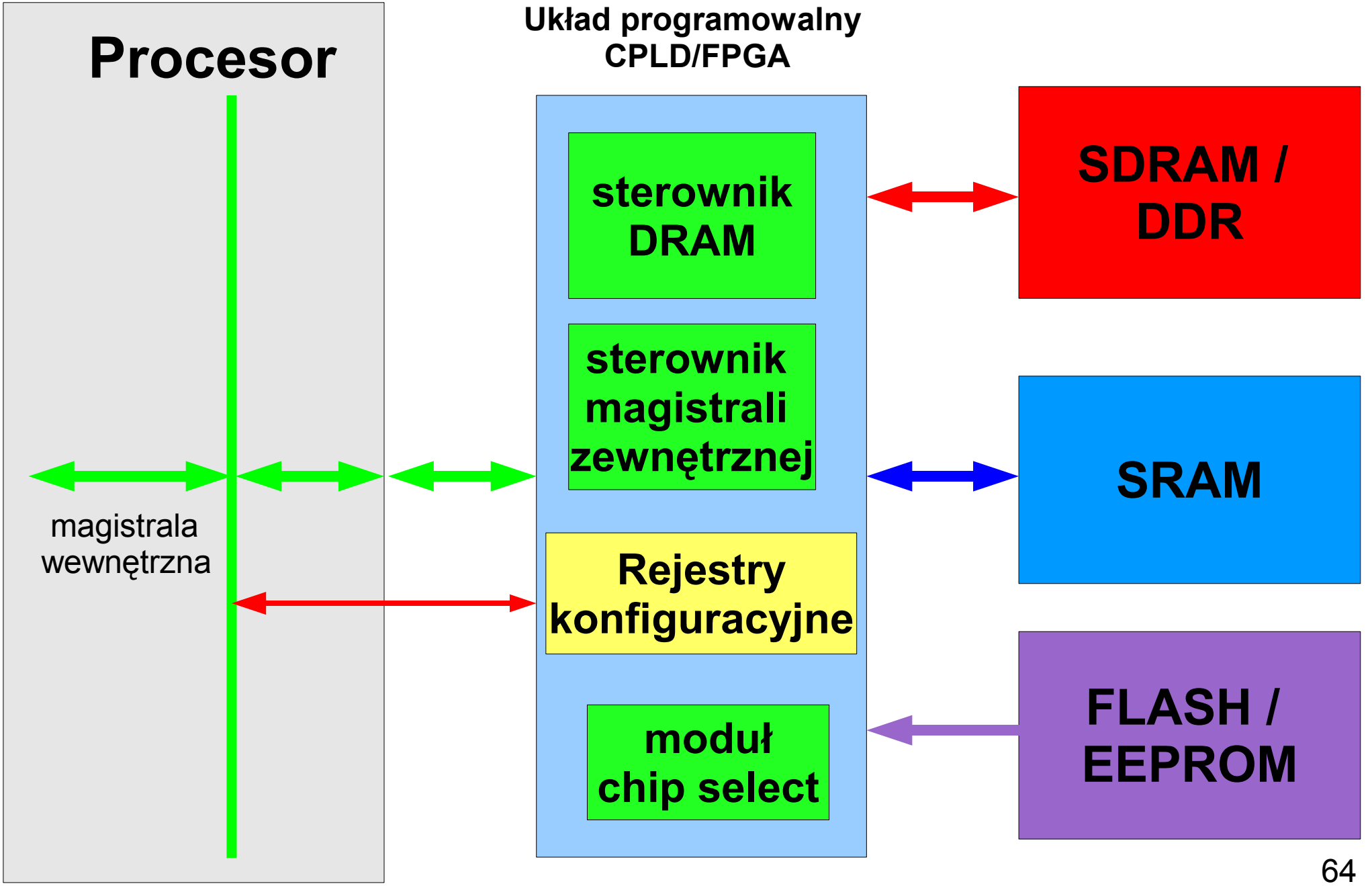


Magistrala łącząca procesor z pamięcią może się okazać wąskim gardłem systemu. Ograniczona szybkość transmisji pomiędzy procesorem, a pamięcią w porównaniu z ilością dostępnej pamięci nazywana jest wąskim gardłem von Neumanna (ang. von Neumann bottleneck).

Jak można przeciwdziałać ?

1. Pamięć cache,
2. Układ DMA.

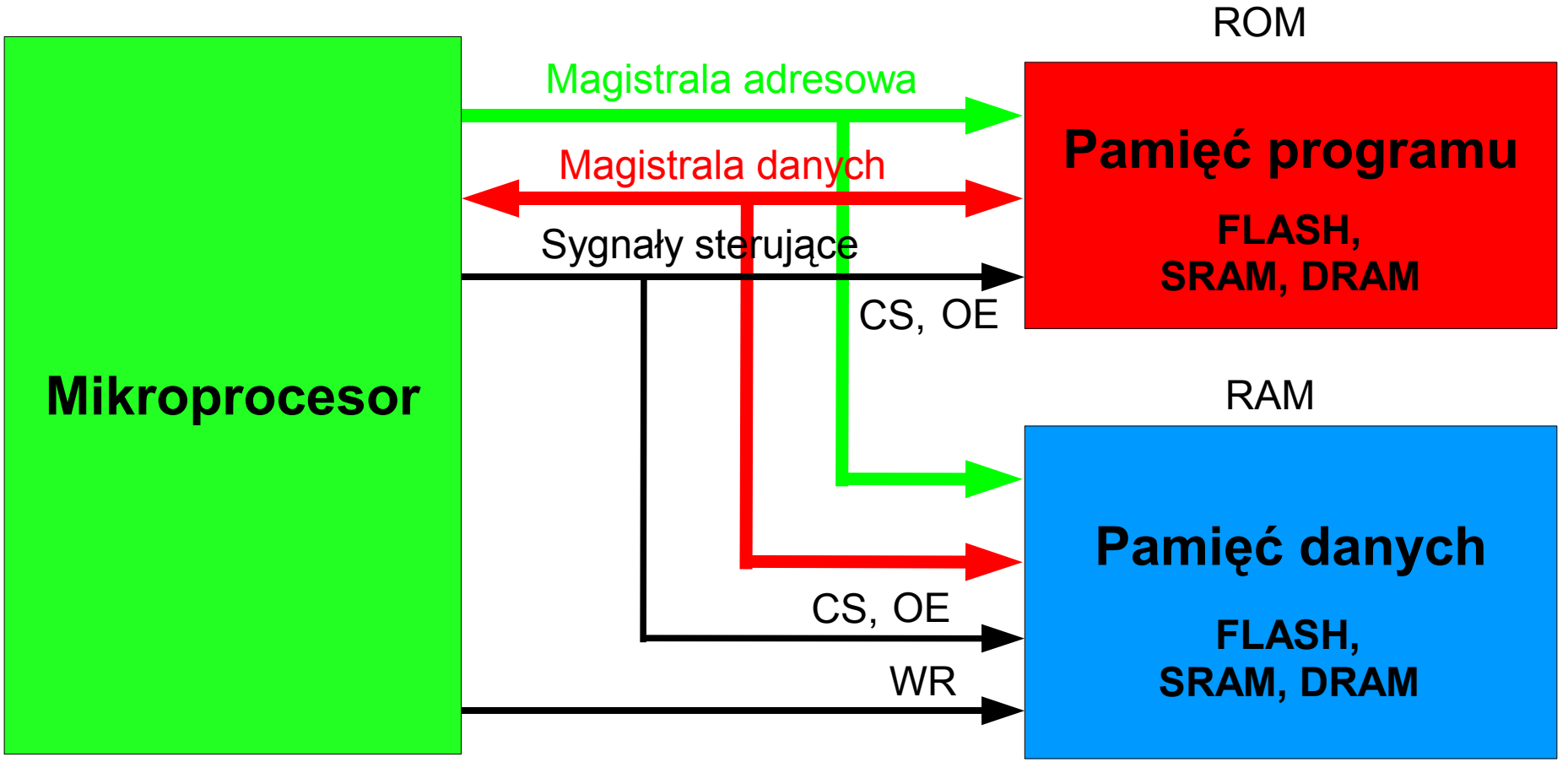
Zastosowanie układów programowalnych do budowy dekoderów adresowych



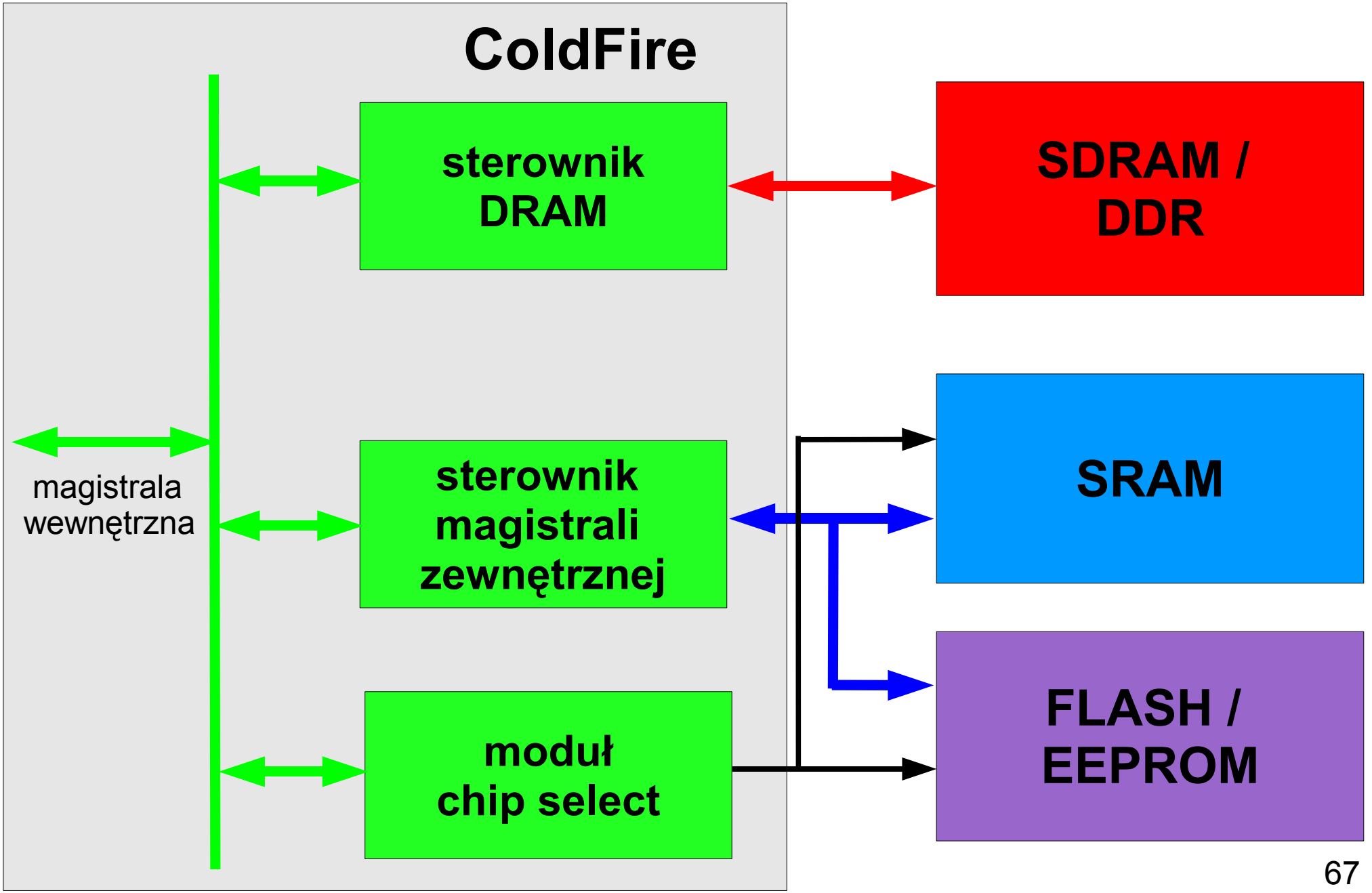
Dekoder adresowy w języku VHDL

```
Entity AddressDecoder is
port
(
      Address : in std_logic_vector(19 downto 0);
      CS_RAM1, CS_RAM2,
      CS_ROM1, CS_ROM2
      CS_PER1, CS_PER2        : out std_logic
);
end AddressDecoder;

Architecture behavior of AddressDecoder  is

begin
      CS_RAM1 <= '0' when address<0x1000 else '1';
      CS_RAM1 <= '0' when (address>=0x1000 and address<0x2000) else '1';
      CS_ROM1 <= '0' when (address>=0x2000 and address<0x3000) else '1';
      CS_ROM1 <= '0' when (address>=0x3000 and address<0x4000) else '1';
      CS_PER1  <= '0' when (address>=0x4000 and address<0x4100) else '1';
      CS_PER2  <= '0' when (address>=0x4100 and address<0x6102) else '1';
End behavior;
```

Współpraca procesora z pamięcią zewnętrzną (1)



Współpraca procesora z pamięcią zewnętrzną (2)



Wewnętrzna pamięć statyczna

Procesory z rodziny ColdFire posiadają do 128 kB wewnętrznej pamięci statycznej obsługiwanej w ciągu jednego cyklu zegarowego dołączonej do szybkiej magistrali wewnętrznej (pamięć dwuportowa).

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>31–16</td><td>BA</td><td>Base address. Defines the 0-modulo-64K base address of the SRAM module. By programming this field, the SRAM may be located on any 64-Kbyte boundary within the processor's 4-Gbyte address space.</td></tr>
<tr><td>15–12</td><td>—</td><td>Reserved, should be cleared.</td></tr>
<tr><td>11–10</td><td>PRI1, PRI2</td><td>Priority bit. PRI1 determines if DMA or CPU has priority in upper 32k bank of memory. PRI2 determines if DMA or CPU has priority in lower 32k bank of memory. If bit is set, DMA has priority. If bit is reset, CPU has priority. Priority is determined according to the following table.
<table>
<tr><th>PRI[1:2]</th><th>Upper Bank Priority</th><th>Lower Bank Priority</th></tr>
<tr><td>00</td><td>DMA Accesses</td><td>DMA Accesses</td></tr>
<tr><td>01</td><td>DMA Accesses</td><td>CPU Accesses</td></tr>
<tr><td>10</td><td>CPU Accesses</td><td>DMA Accesses</td></tr>
<tr><td>11</td><td>CPU Accesses</td><td>CPU Accesses</td></tr>
</table>
NOTE: The Motorola-recommended setting for the priority bits is 00.</td></tr>
<tr><td>9</td><td>SPV</td><td>Secondary port valid. Allows access by DMA
0 DMA access to memory is disabled.
1 DMA access to memory is enabled.
NOTE: The BDE bit in the second RAMBAR register must also be set to allow dual port access to the SRAM. For more information, see Section 8.4.2, "Memory Base Address Register (RAMBAR)."</td></tr>
</table>

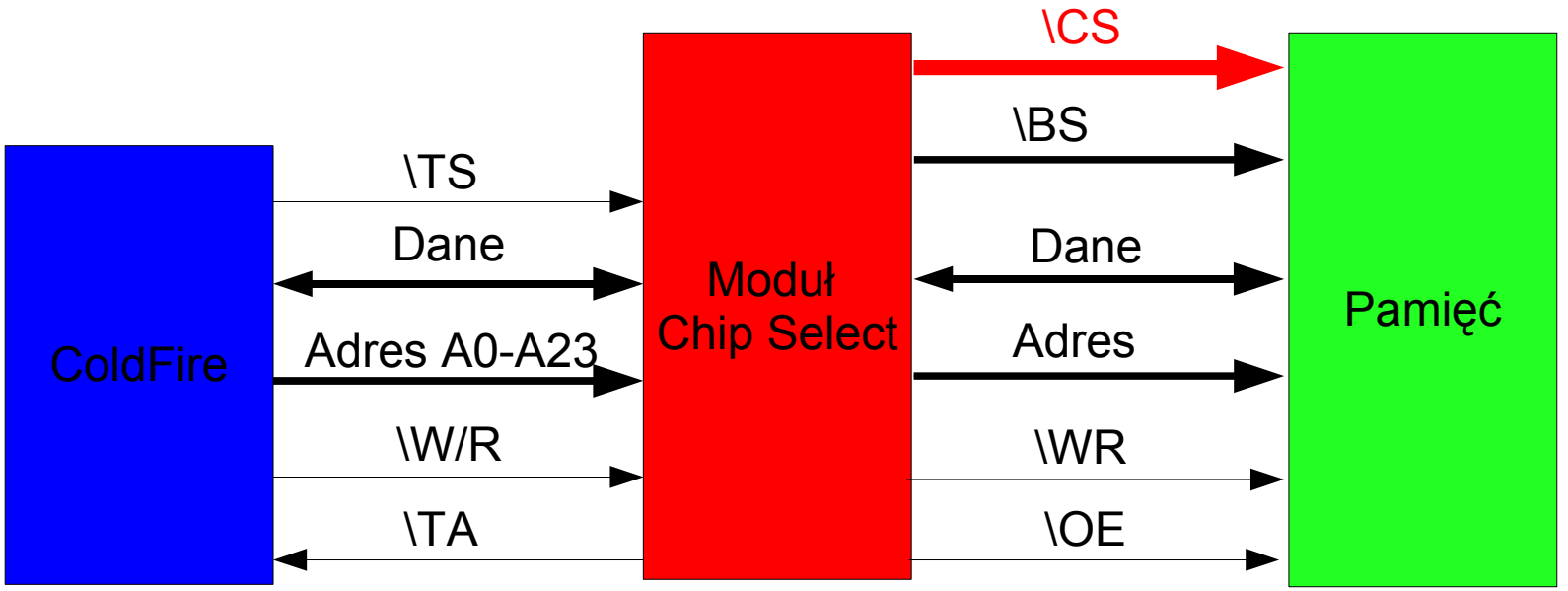
Rejestr konfigurujący RAMBAR

Bits	Name	Description
8	WP	Write protect. Allows only read accesses to the SRAM. When this bit is set, any attempted write access will generate an access error exception to the ColdFire processor core. 0 Allows read and write accesses to the SRAM module 1 Allows only read accesses to the SRAM module
7–6	—	Reserved, should be cleared.
5–1	C/I, SC, SD, UC, UD	Address space masks (ASn) These five bit fields allow certain types of accesses to be "masked," or inhibited from accessing the SRAM module. The address space mask bits are: C/I = CPU space/interrupt acknowledge cycle mask SC = Supervisor code address space mask SD = Supervisor data address space mask UC = User code address space mask UD = User data address space mask For each address space bit: 0 An access to the SRAM module can occur for this address space 1 Disable this address space from the SRAM module. If a reference using this address space is made, it is inhibited from accessing the SRAM module, and is processed like any other non-SRAM reference. These bits are useful for power management as detailed in Section 5.3.4, "Power Management."
0	V	Valid. A hardware reset clears this bit. When set, this bit enables the SRAM module; otherwise, the module is disabled. 0 Contents of RAMBAR are not valid 1 Contents of RAMBAR are valid

Przykład:
RAMBAR = 0xF000.0121

Adres bazowy = F000.0000,
rozmiar = 64 kB (2^16)
wyłączone DMA, R/W

Moduł obsługujący urządzenia dołączone do zewnętrznej magistrali (1)



\TA – Transfer Acknowledge, potwierdzenie transmisji
\TS – Transfer Strobe, ważne dane oraz adresy na magistralach
\TIP – Transfer In Progres, utrzymywany w stanie niskim do zakończenia transmisji
\TEA – Transfer Error, wejście sygnalizacji błędu zewnętrznego

Moduł obsługujący urządzenia dołączone do zewnętrznej magistrali (1)

Signal	Description
Chip Selects ($\overline{CS}$[6:0])	Each $\overline{CSn}$ can be independently programmed for an address location as well as for masking, port size, read/write burst capability, wait-state generation, and internal/external termination. Only $\overline{CS0}$ is initialized at reset and may act as an external boot chip select to allow boot ROM to be at an external address space. Port size for $\overline{CS0}$ is configured by the logic levels of D[19:18] when $\overline{RSTO}$ negates and $\overline{RCON}$ is asserted.
Output Enable ($\overline{OE}$)	Interfaces to memory or to peripheral devices and enables a read transfer. It is asserted and negated on the falling edge of the clock. $\overline{OE}$ is asserted only when one of the chip selects matches for the current address decode.
Byte Strobes $\overline{BS}$[3:0]	These signals are individually programmed through the byte-enable mode bit, CSCR*n*[BEM], described in Section 12.4.1.3. These generated signals provide byte data select signals, which are decoded from the transfer size, A1, and A0 signals in addition to the programmed port size and burstability of the memory accessed, as Table 12-2 shows.

D[19:18]	Boot Device/Data Port Size
00	Internal (32-bit)
01	External (16-bit)
10	External (8-bit)
11	External (32-bit)

Rejestry konfiguracyjne

Chip Select Address Registers (CSAR0–CSAR6)

Bits	Name	Description
15–0	BA	Base address. Defines the base address for memory dedicated to chip select $\overline{\text{CS}}$[6:0]. BA is compared to bits 31–16 on the internal address bus to determine if chip select memory is being accessed.

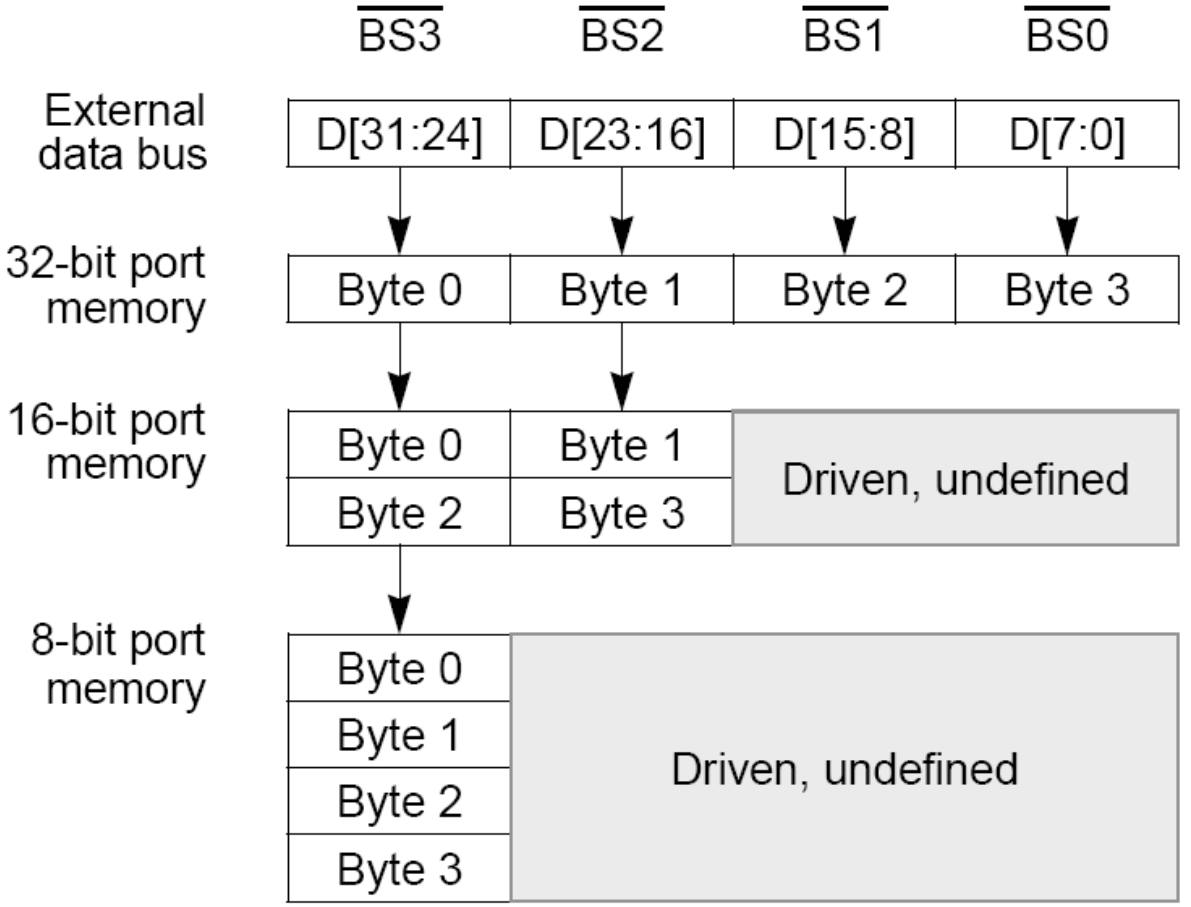
Chip Select Mask Registers (CSMR0–CSMR6)

	31 … 16	15 … 9	8	7	6	5	4	3	2	1	0
Field	BAM	—	WP	—	AM	C/I	SC	SD	UC	UD	V
Reset	Unitialized										0
R/W	R/W										
Addr	0x084 (CSMR0); 0x090 (CSMR1); 0x09C (CSMR2); 0x0A8 (CSMR3); 0x0B4 (CSMR4); 0x0C0 (CSMR5); 0x0CC (CSMR6)										

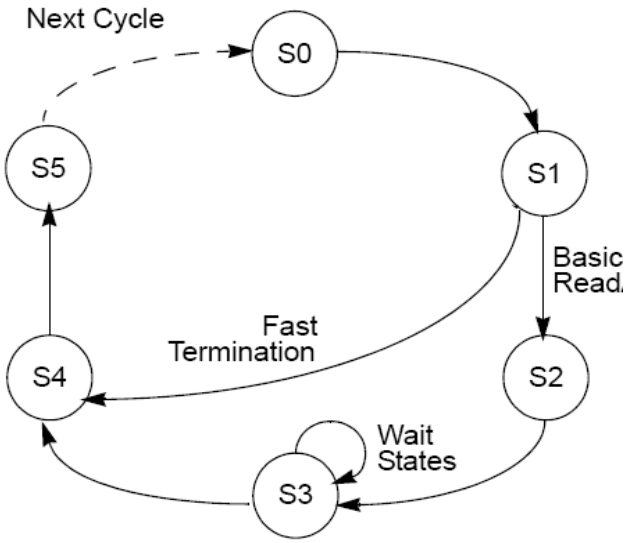
Chip Select Control Registers (CSCR0–CSCR6)

Bits	Name	Description
15–14	—	Reserved, should be cleared.
13–10	WS	Wait states. The number of wait states inserted before an internal transfer acknowledge is generated (WS = 0 inserts zero wait states, WS = 0xF inserts 15 wait states). If AA = 0, $\overline{TA}$ must be asserted by the external system regardless of the number of wait states generated. In that case, the external $\overline{TA}$ transfer acknowledge ends the cycle. An external $\overline{TA}$ supercedes the generation of an internal $\overline{TA}$.
9	—	Reserved, should be cleared.
8	AA	Auto-acknowledge enable. Determines the assertion of the internal transfer acknowledge for accesses specified by the chip select address. 0 No internal $\overline{TA}$ is asserted. Cycle is terminated externally. 1 Internal $\overline{TA}$ is asserted as specified by WS. Note that if AA = 1 for a corresponding $\overline{CS}n$ and the external system asserts an external $\overline{TA}$ before the wait-state countdown asserts the internal $\overline{TA}$, the cycle is terminated. Burst cycles increment the address bus between each internal termination.
7–6	PS	Port size. Specifies the width of the data associated with each chip select. It determines where data is driven during write cycles and where data is sampled during read cycles. See Section 12.3.1.1. 00 32-bit port size. Valid data sampled and driven on D[31:0] 01 8-bit port size. Valid data sampled and driven on D[31:24] 1x 16-bit port size. Valid data sampled and driven on D[31:16]
5	BEM	Byte enable mode. Specifies the byte enable operation. Certain SRAMs have byte enables that must be asserted during reads as well as writes. BEM can be set in the relevant CSCR to provide the appropriate mode of byte enable in support of these SRAMs. 0 $\overline{BS}$ is not asserted for read. $\overline{BS}$ is asserted for data write only. 1 $\overline{BS}$ is asserted for read and write accesses.
4	BSTR	Burst read enable. Specifies whether burst reads are used for memory associated with each $\overline{CS}n$. 0 Data exceeding the specified port size is broken into individual, port-sized non-burst reads. For example, a longword read from an 8-bit port is broken into four 8-bit reads. 1 Enables data burst reads larger than the specified port size, including longword reads from 8- and 16-bit ports, word reads from 8-bit ports, and line reads from 8-, 16-, and 32-bit ports.
3	BSTW	Burst write enable. Specifies whether burst writes are used for memory associated with each $\overline{CS}n$. 0 Break data larger than the specified port size into individual port-sized, non-burst writes. For example, a longword write to an 8-bit port takes four byte writes. 1 Enables burst write of data larger than the specified port size, including longword writes to 8 and 16-bit ports, word writes to 8-bit ports and line writes to 8-, 16-, and 32-bit ports.
2–0	—	Reserved, should be cleared.

Moduł obsługujący urządzenia dołączone do zewnętrznej magistrali (2)

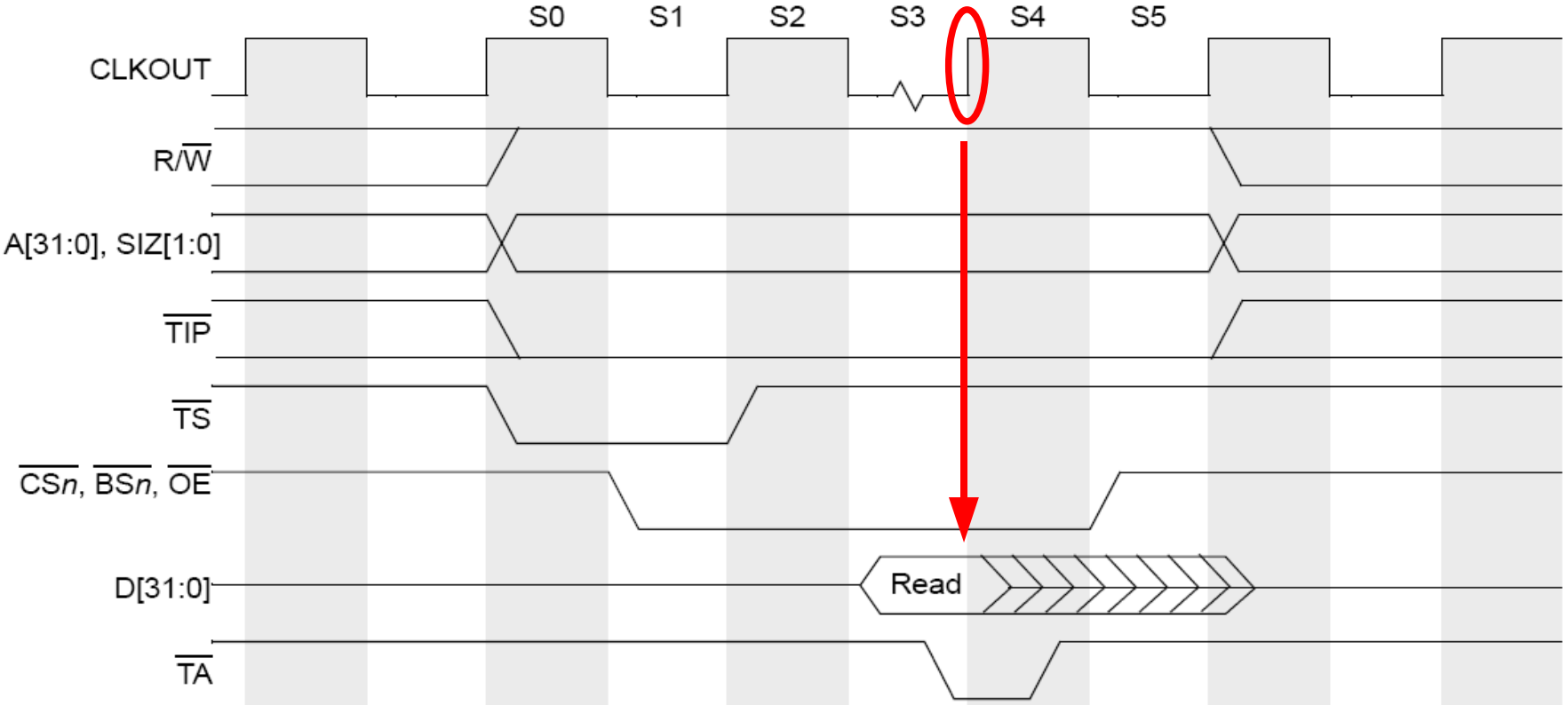


Cykl odczytu

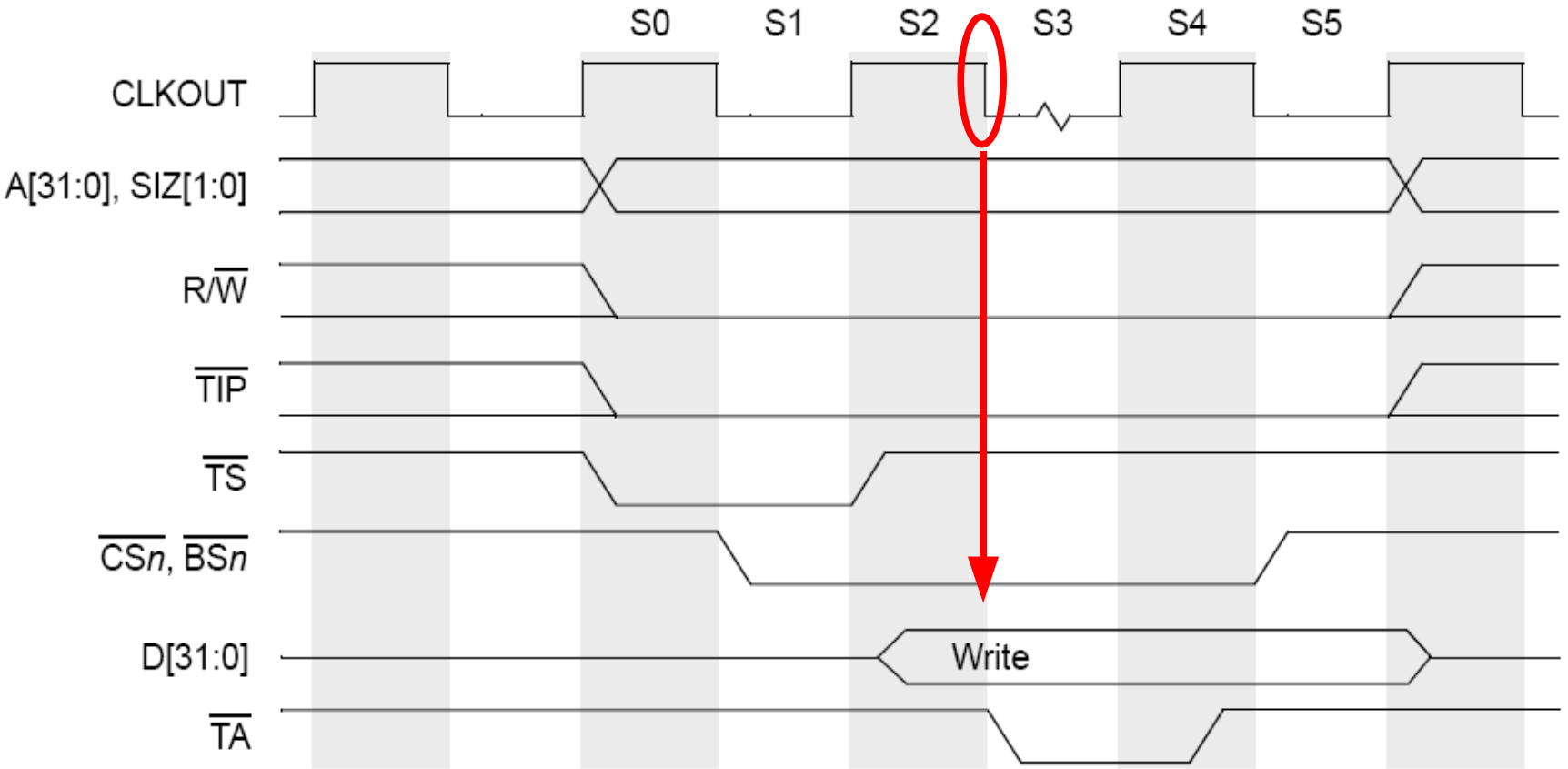


SIZ[1:0]	Transfer Size
00	Longword
01	Byte
10	Word
11	16-byte line

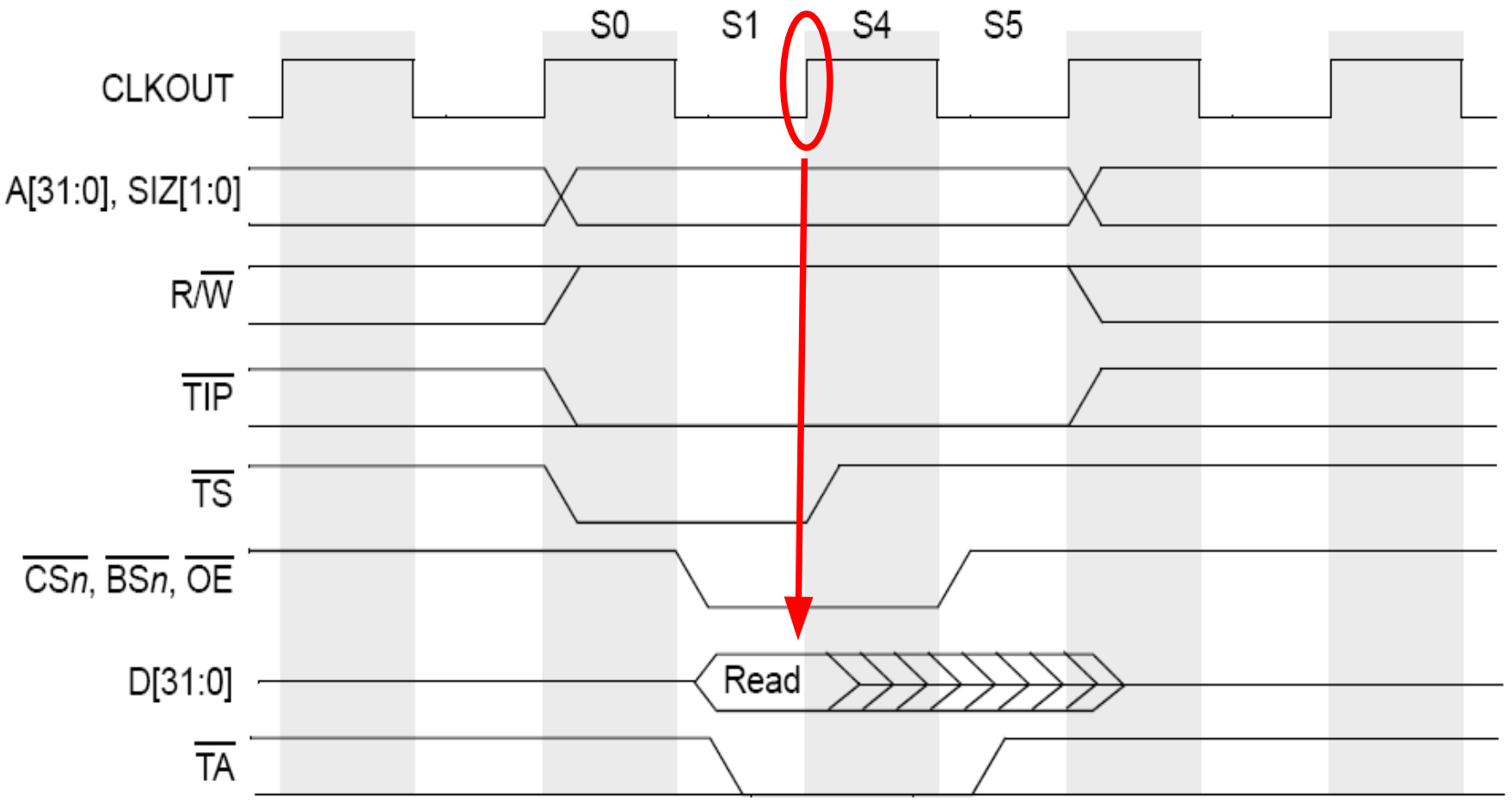
Narastające zbocze zegara



Podstawowy cykl zapisu

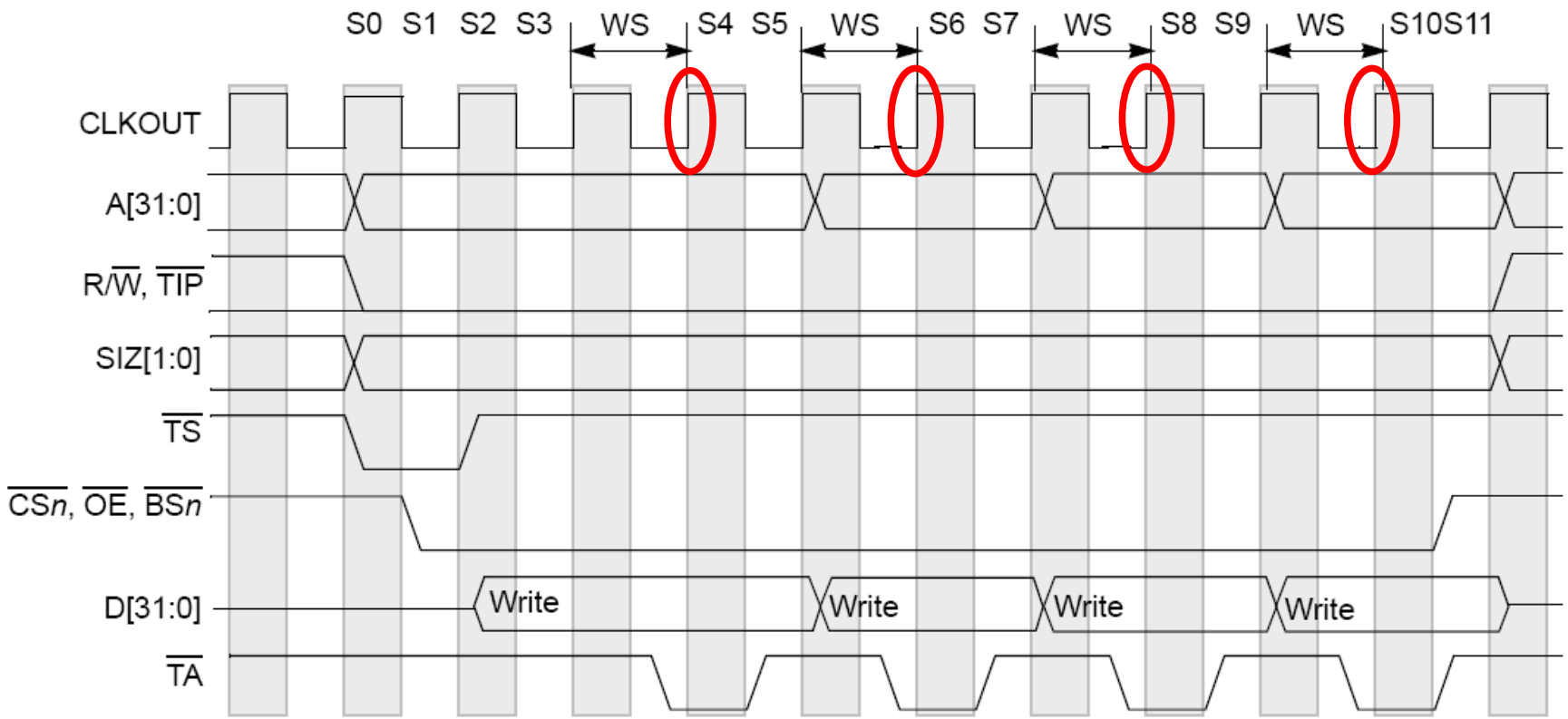


Cykl odczytu z szybką zakończeniem



Tryb z szybkim zakończeniem nie może zostać użyty podczas wewnętrznej terminacji.

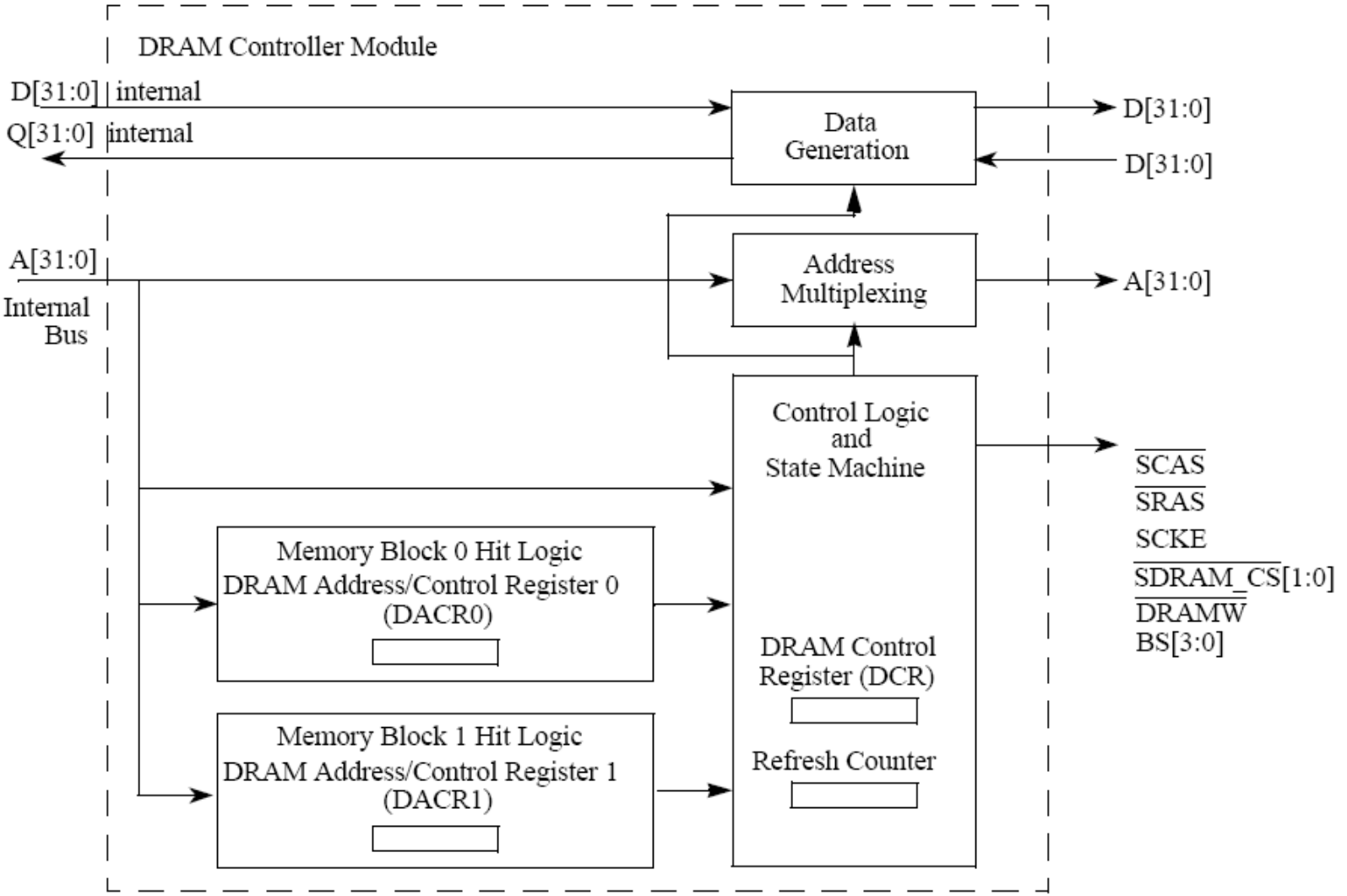
Cykl zapisu burst (3-2-2-2)



Cykle zapisu i odczytu wykorzystywane podczas transmisji DMA oraz operacji na pamięci podręcznej.

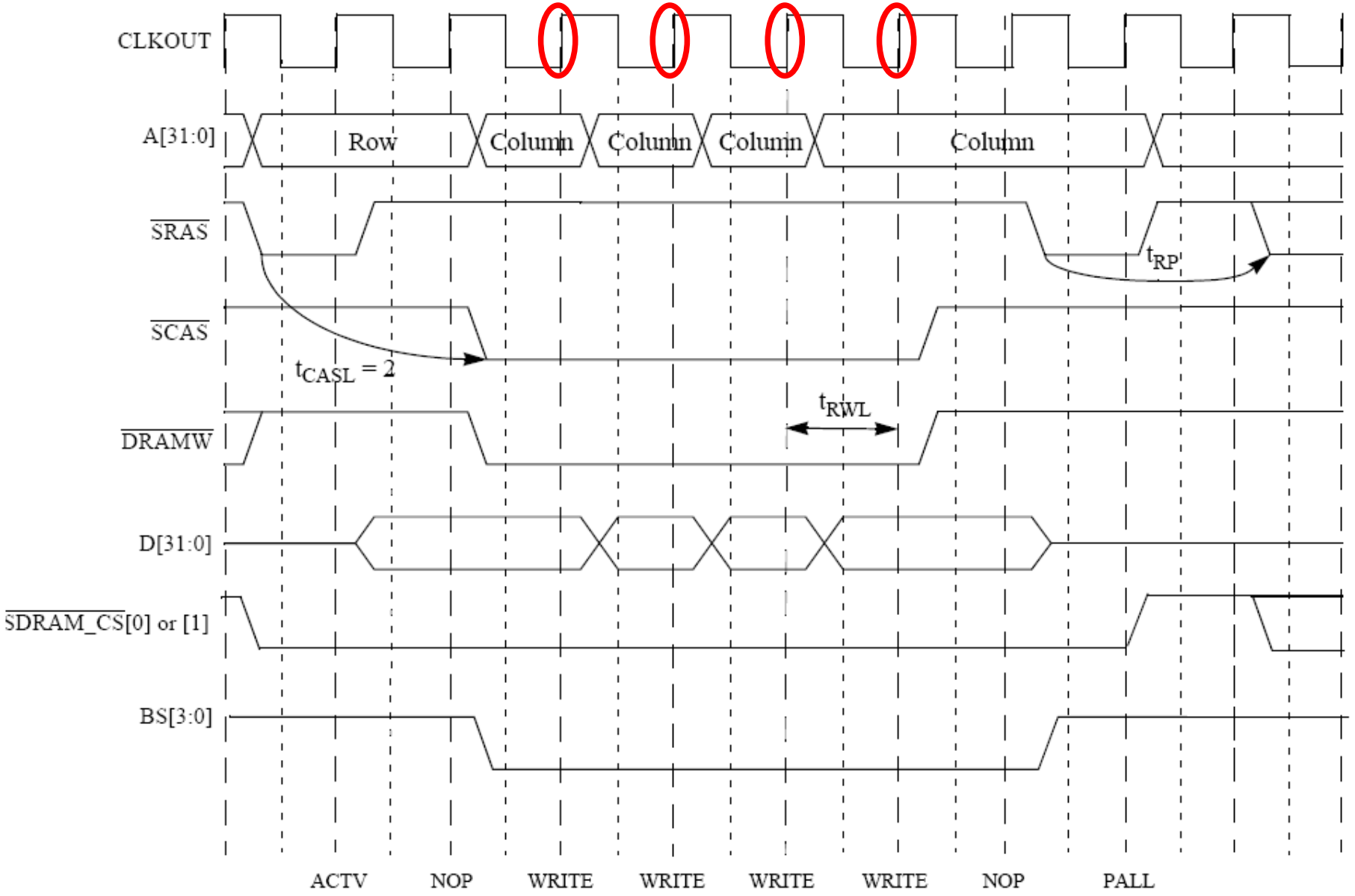
Sterownik pamięci dynamicznej

- Obsługa dwóch pamięci dynamicznych SDRAM MCF528x (MCF520x/MCF527x pamięci DDR)
- Programowalne linie SRAS, SCAS oraz czas odświeżania
- Obsługa pamięci 8, 16, 32 bitowych



Transmisja zapisu do pamięci SDRAM

Transfer typu burst



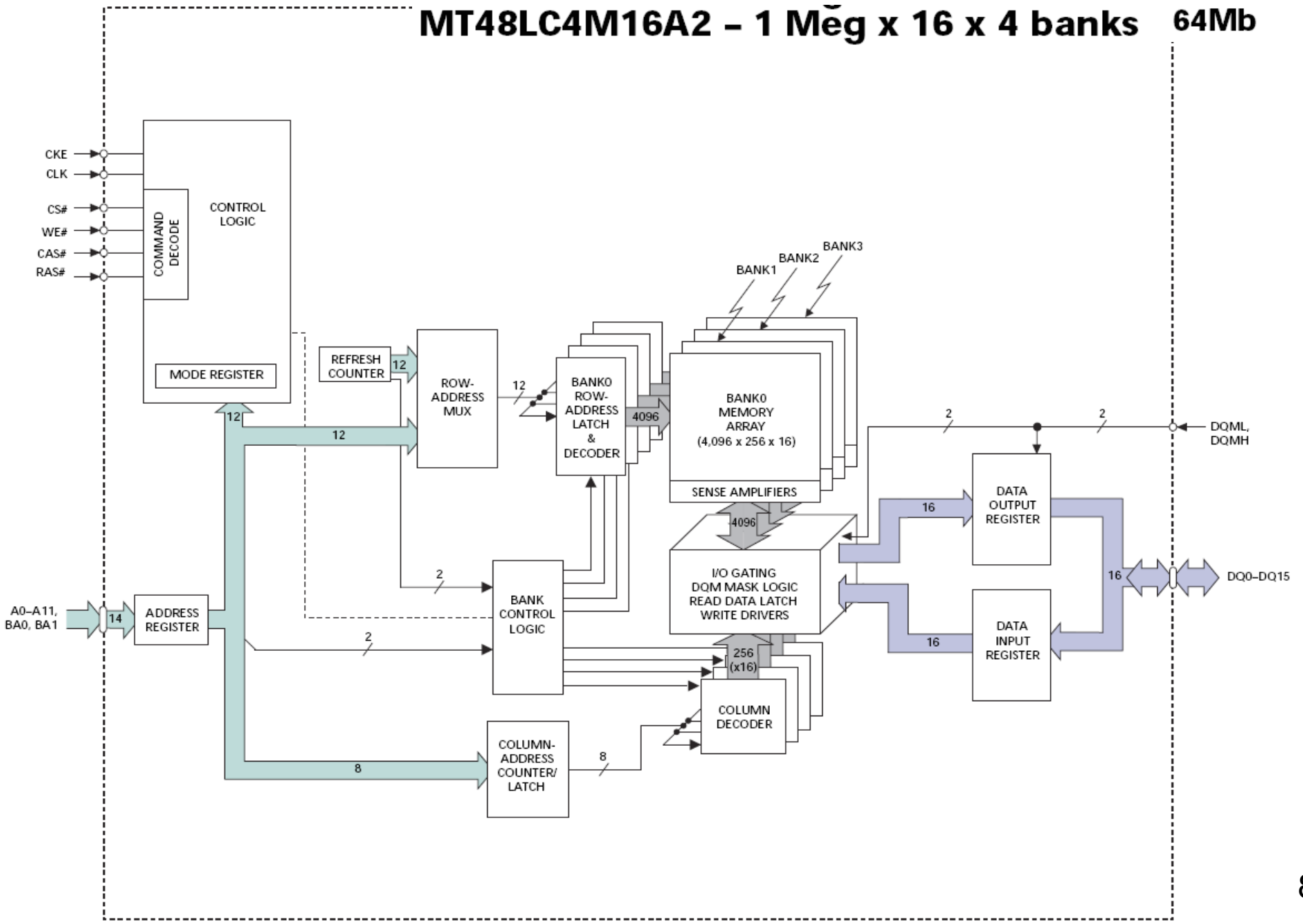
Rejestry konfiguracyjne

IPSBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x040	DRAM control register (DCR) [p. 15-5]		—	
0x044	—			
0x048	DRAM address and control register 0 (DACR0) [p. 15-6]			
0x04C	DRAM mask register block 0 (DMR0) [p. 15-8]			
0x050	DRAM address and control register 1 (DACR1) [p. 15-6]			
0x054	DRAM mask register block 1 (DMR1) [p. 15-8]			

	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	1K (A0–A9)	512 (A0–A8)	256 (A0–A7)

Parameter	Specification
Speed grade (-6)	166 MHz
12 rows, 8 columns	
Two bank-select lines to access four internal banks	
ACTV-to-read/write delay (t_{RCD})	18 ns (min.)
Period between auto-refresh and ACTV command (t_{RC})	60 ns
ACTV command to precharge command (t_{RAS})	42 ns (min.)
Precharge command to ACTV command (t_{RP})	18 ns (min.)
Last data input to PALL command (t_{RWL})	1 bus clock
Auto-refresh period for 4096 rows (t_{REF})	64 ms

64 Mbit pamięć firmy Micron



Dołączenie pamięci SDRAM Micron 64 MB

MCF5282 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23
Row	15	14	13	12	11	10	9	17	18	19	20	21	22	23
Column	2	3	4	5	6	7	8	16						
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	**BA0**	**BA1**

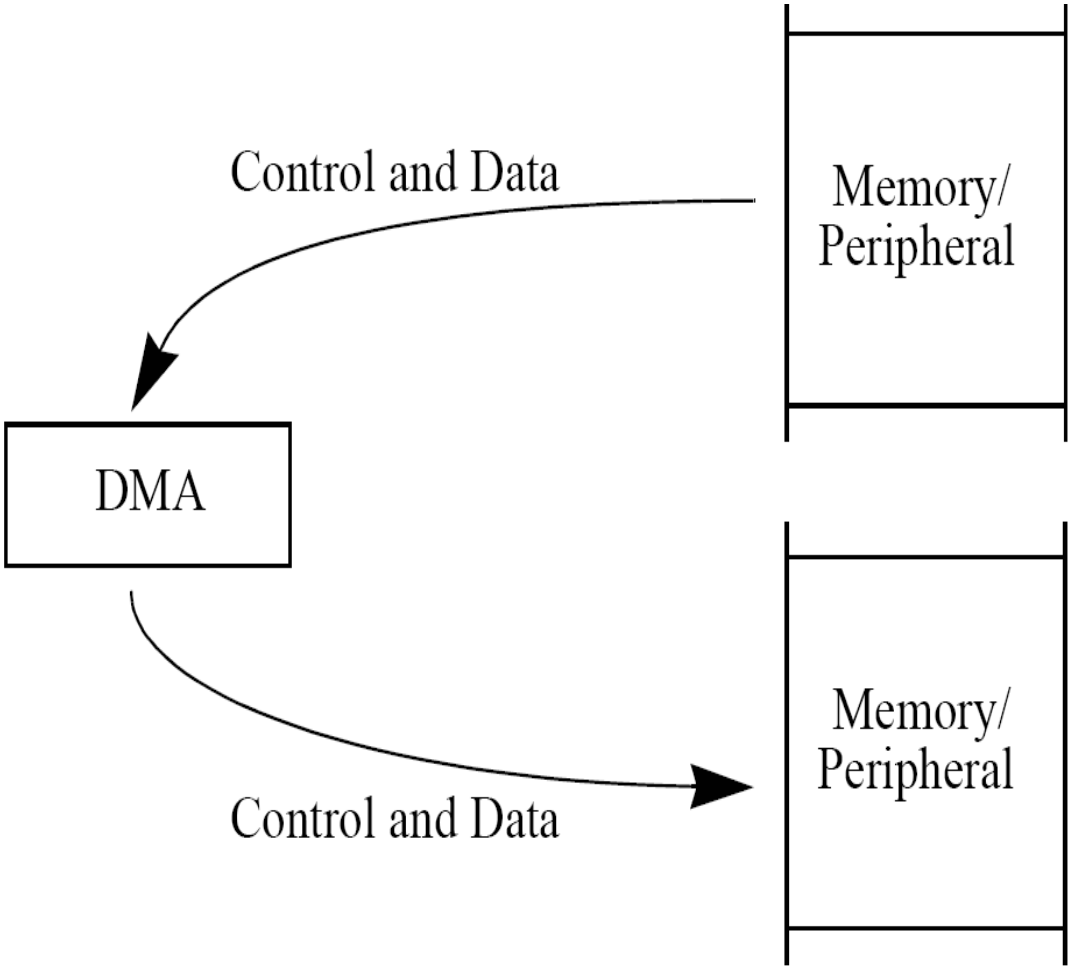
Konfiguracja pamięci SDRAM

MCF5282 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23
Row	15	14	13	12	11	10	9	17	18	19	20	21	22	23
Column	2	3	4	5	6	7	8	16						
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	**BA0**	**BA1**

Bits	Name	Setting	Description
31–18	BA	1111_1111_ 1000_10	Base address. So DACR0[31–16] = 0xFF88, placing the starting address of the SDRAM accessible memory at 0xFF88_0000.
17–16	—		Reserved. Don't care.
15	RE	0	Keeps auto-refresh disabled because registers are being set up at this time.
14	—		Reserved. Don't care.
13–12	CASL	00	Indicates a delay of data 1 cycle after $\overline{\text{SCAS}}$ is asserted
11	—		Reserved. Don't care.
10–8	CBM	011	Command bit is pin 20 and bank selects are 21 and up.
7	—		Reserved. Don't care.
6	IMRS	0	Indicates MRS command has not been initiated.
5–4	PS	00	32-bit port.
3	IP	0	Indicates precharge has not been initiated.
2–0	—		Reserved. Don't care.

Bezpośredni dostęp do pamięci DMA

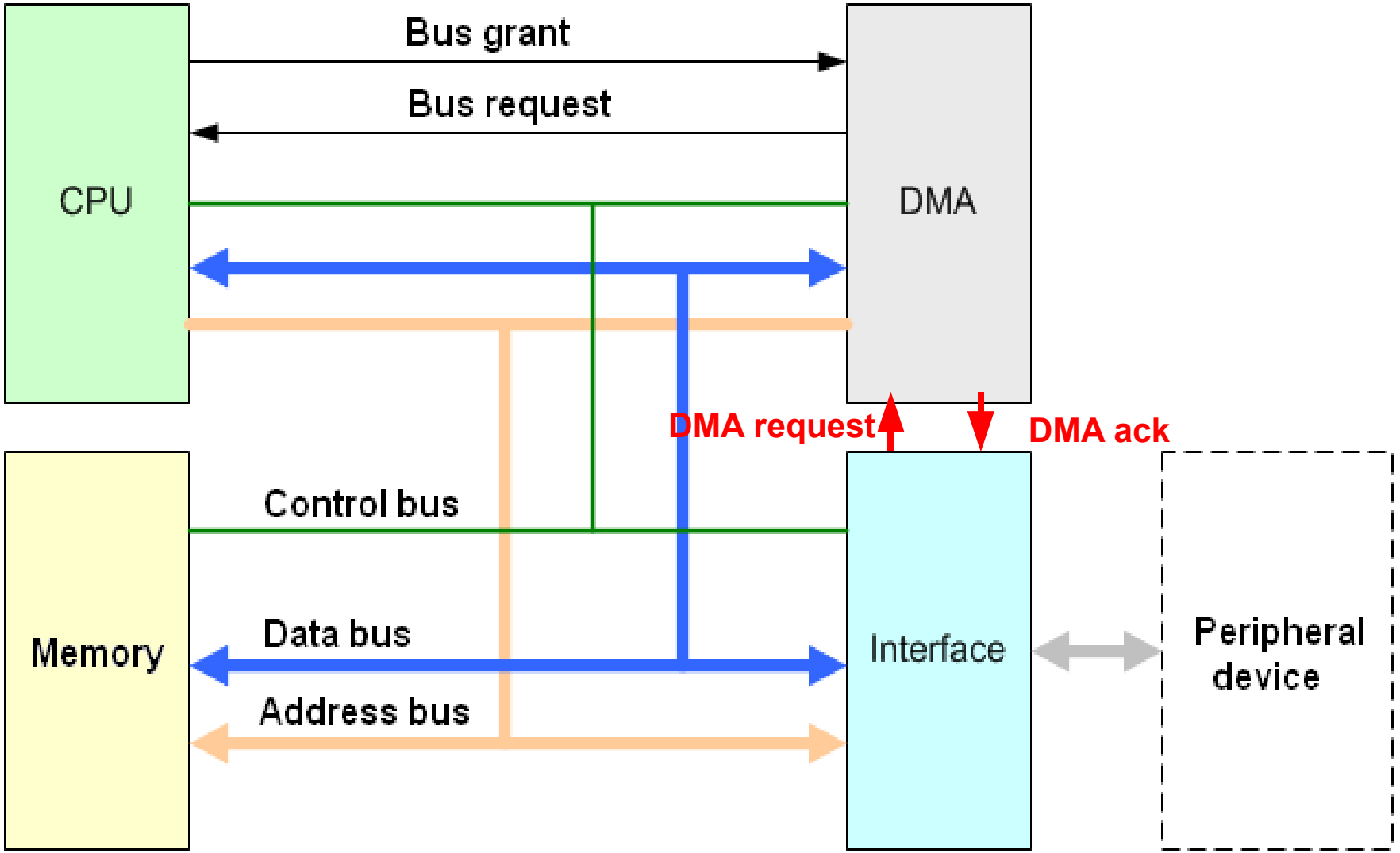
Bezpośredni dostęp do pamięci (1)



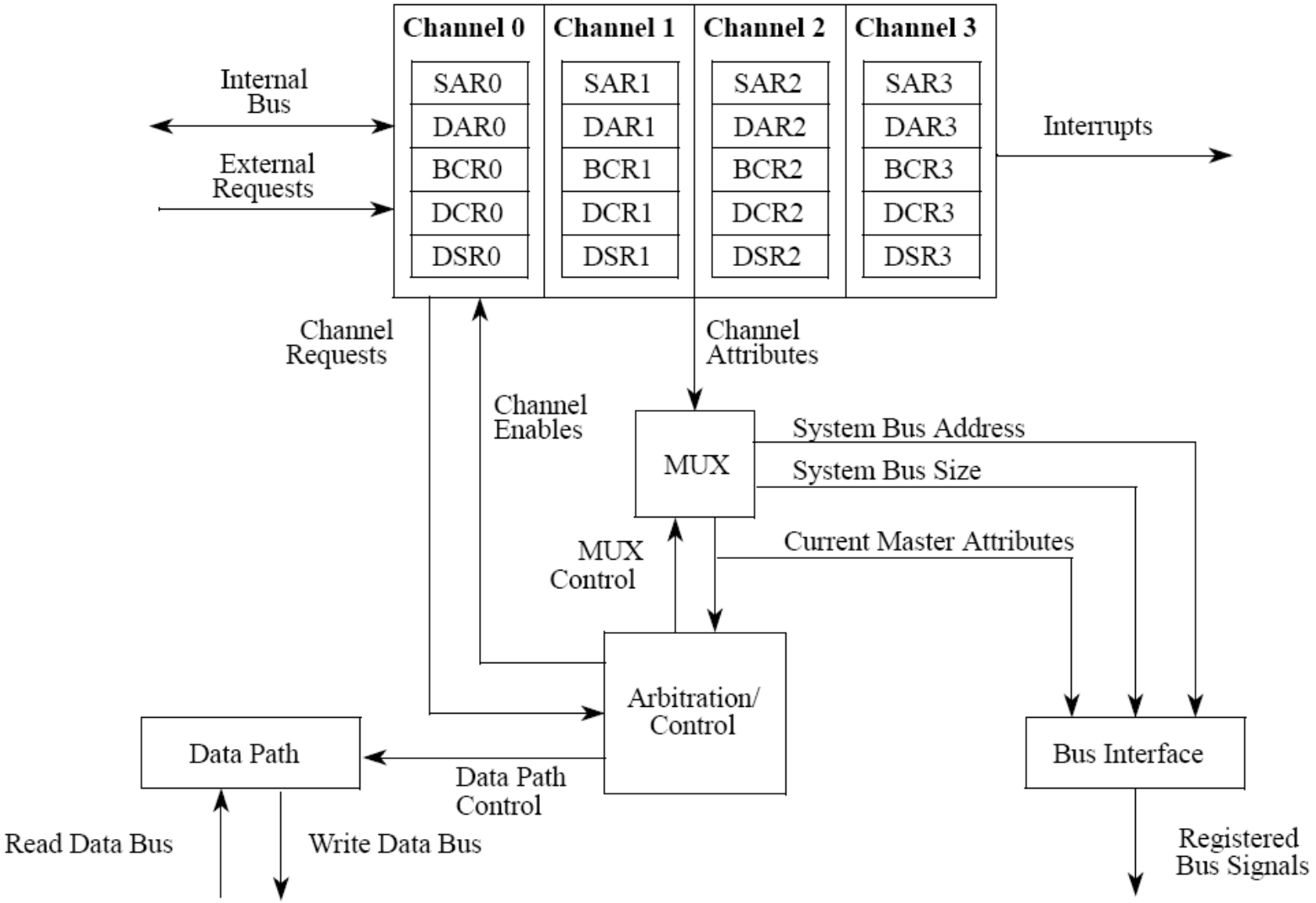
Zadanie

Napisać program w języku asembler kopiujący blok danych o wielkości 512 B z bufora interfejsu sieciowego (eth0) do pamięci danych (pod adres 0x1000). Urządzenie eth0 mapowane jest pod adresem 0xFFC0.0100.

Bezpośredni dostęp do pamięci (2)



Układ DMA procesora ColdFire



Układ DMA procesora ColdFire

Cechy modułu DMA:

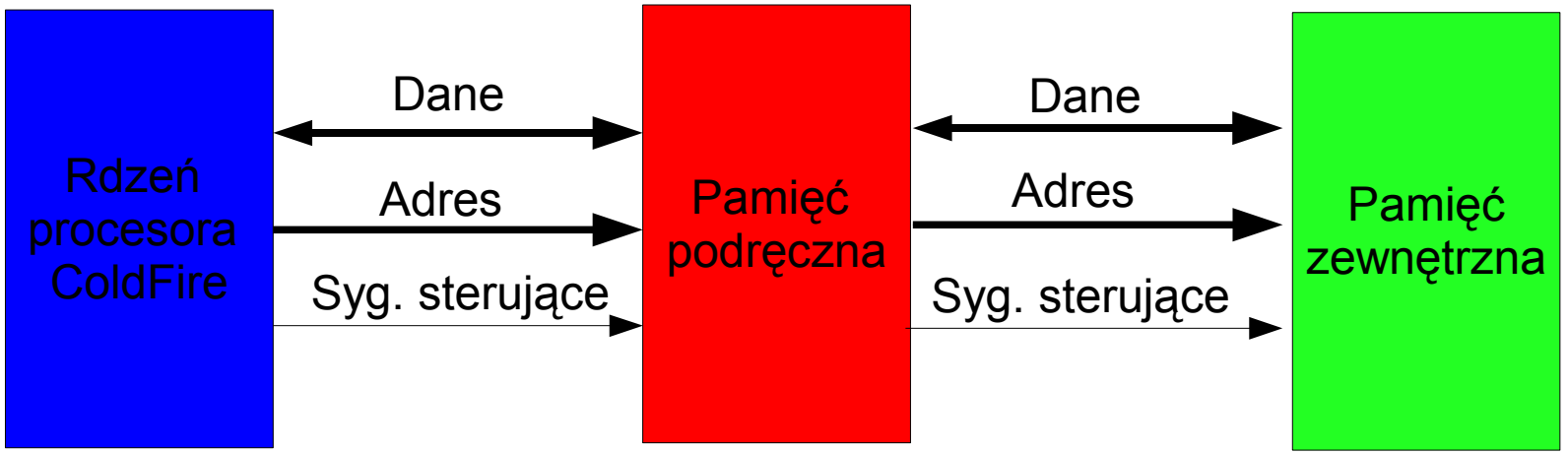
- Cztery niezależne programowalne kanały DMA
- Automatyczne wyrównywanie podczas dostępu do przestrzeni adresowej obu urządzeń,
- Transfer danych 8-, 16-, 32-, or 128-bitowych,
- Transfer jednokrotny lub ciągły,
- Transfer z urządzeń o różnych szerokościach magistral,
- Niezależne rejestry adresowe dla obu urządzeń między, którymi wykonywany jest transfer
- Zgłaszanie przerwań w przypadku nieprawidłowego odczytu

Sterowniki DMA

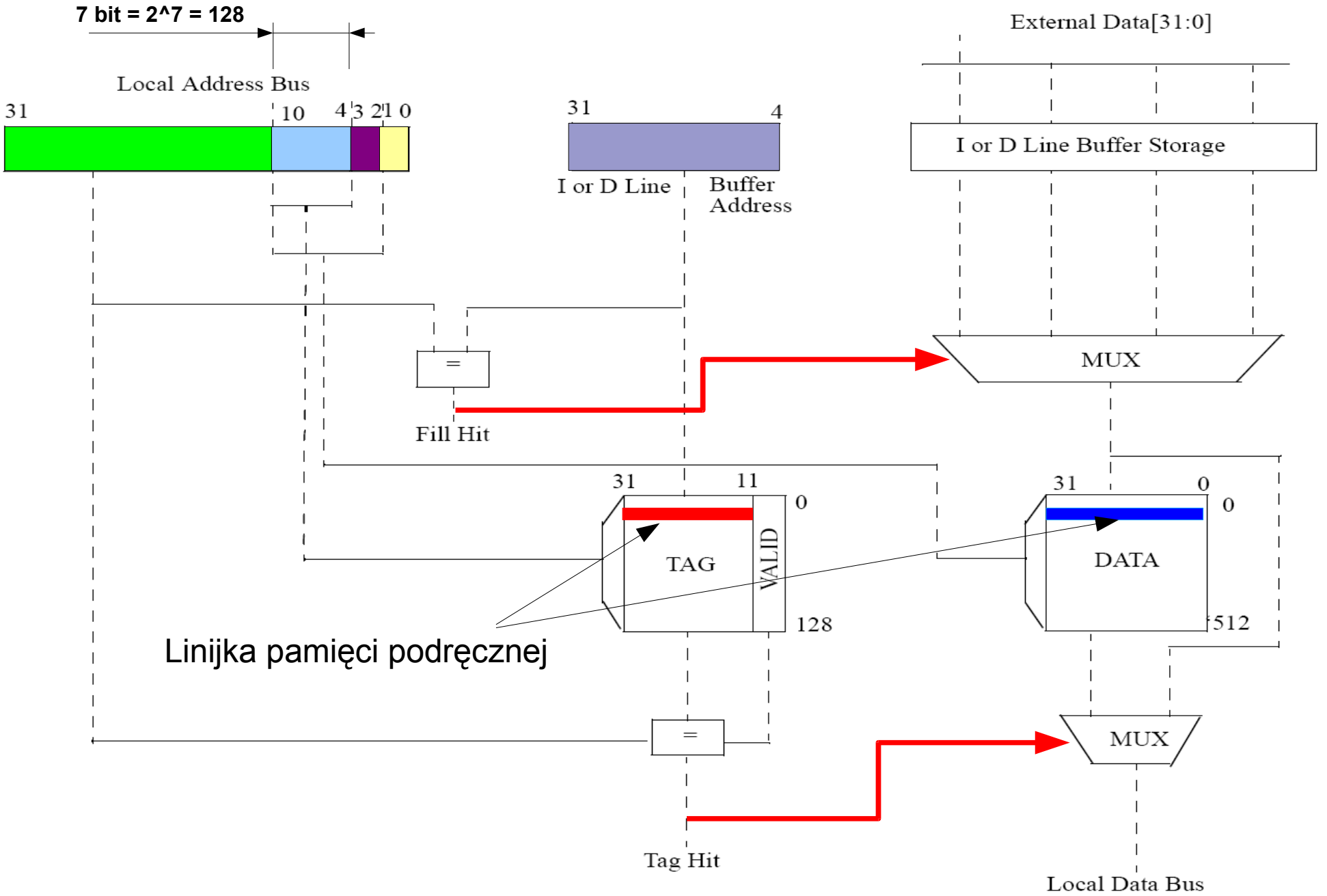
Platform	Number of DMA Channels	Data Size	Maximum Buffer Size	DMA Bus Operation	DMA Transfer Rates (Mbytes/sec)		
					8-bit	16-bit	32-bit
PC/XT	four	8-bit	64 kilobytes	flyby	0.9	–	–
PC AT (ISA)	seven (four 8-bit, three 16-bit)	8-bit, 16-bit	64 kilobytes or words	flyby	0.8	1.6	–
EISA	seven	8-bit, 16-bit, 32-bit	16 megabytes	flyby non-burst	1-2	2-4	5-8
EISA	seven	8-bit, 16-bit, 32-bit	16 megabytes	flyby burst	8.2	16.5	33.0
Micro Channel	eight	8-bit, 16-bit	16 megabytes	fetch-and-deposit	2.5	5.0	–
Macintosh II NB-DMA-8-G	eight	8-bit, 16-bit, 32-bit	16 megabytes	fetch-and-deposit to Macintosh II memory	1.4	2.0	2.5
Macintosh II NB-DMA2800	eight	8-bit, 16-bit, 32-bit	16 megabytes	fetch-and-deposit to Macintosh II memory	1.2	1.7	2.2
Macintosh II NB-DMA2800	eight	32-bit	16 megabytes	flyby to Macintosh II memory	–	–	3.1
Macintosh II NB-DMA2800	eight	32-bit	16 megabytes	flyby to fast NuBus memory	–	–	8.0
Macintosh II NB-DMA2800	eight	32-bit	16 megabytes	flyby to NuBus block-mode memory	–	–	29.1

Pamięć podręczna (Cache) (1)

- Pamięć podręczna procesorów ColdFire jest przeznaczona do przechowywania kopii niewielkiego obszaru pamięci programu i /lub danych (16 kB rozmiar linii danych),
- Pamięć dołączona do szybkiej magistrali wewnętrznej procesora,
- Odczyt/zapis w ciągu jednego cyklu zegarowego,
- Procesor MCF5282 wyposażony jest w 2 kB pamięci (512 x 32), MCF547x/8x z rodziny V4e = 32 kB (Pentium III cache L1 = 32 kB).



Pamięć podręczna (Cache) (2)



Rejestry konfiguracyjne

Address	Name	Width	Description	Reset Value	Access
MOVEC with 0x002	CACR	32	Cache Control Register	0x0000_0000	W
MOVEC with 0x004	ACR0	32	Access Control Register 0	0x0000_0000	W
MOVEC with 0x005	ACR1	32	Access Control Register 1	0x0000_0000	W

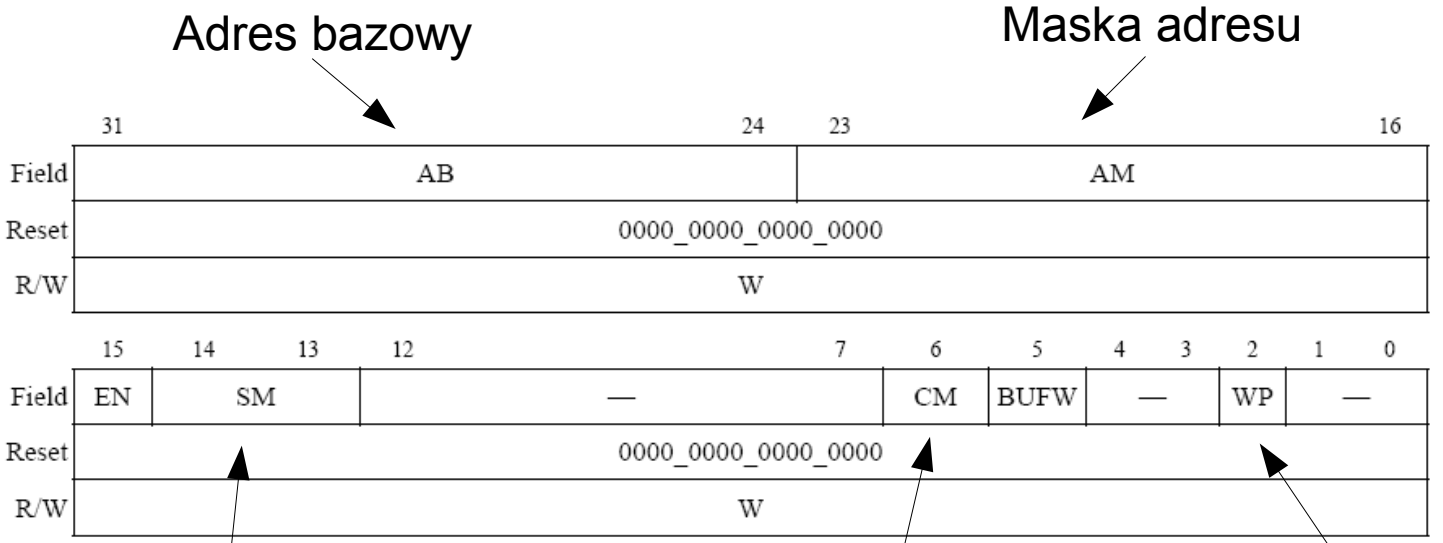


Figure 4-3. Access Control Registers (ACR0, ACR1)

Tryb pracy S/U

Pamięć aktywna

Write protect

Rejestr konfiguracyjny CACR

Bits	Name	Description
31	CENB	Cache enable. The memory array of the cache is enabled only if CENB is asserted. This bit, along with the DISI (disable instruction caching) and DISD (disable data caching) bits, control the cache configuration. 0 Cache disabled 1 Cache enabled Table 4-5 describes cache configuration.
30–29	—	Reserved, should be cleared.
28	CPDI	Disable CPUSHL invalidation. When the privileged CPUSHL instruction is executed, the cache entry defined by bits [10:4] of the address is invalidated if CPDI = 0. If CPDI = 1, no operation is performed. 0 Enable invalidation 1 Disable invalidation
27	CFRZ	Cache freeze. This field allows the user to freeze the contents of the cache. When CFRZ is asserted line fetches can be initiated and loaded into the line-fill buffer, but a valid cache entry can not be overwritten. If a given cache location is invalid, the contents of the line-fill buffer can be written into the memory array while CFRZ is asserted. 0 Normal Operation 1 Freeze valid cache lines
26–25	—	Reserved, should be cleared.
24	CINV	Cache invalidate. The cache invalidate operation is not a function of the CENB state (that is, this operation is independent of the cache being enabled or disabled). Setting this bit forces the cache to invalidate all, half, or none of the tag array entries depending on the state of the DISI, DISD, INVI, and INVD bits. The invalidation process requires several cycles of overhead plus 128 machine cycles to clear all tag array entries and 64 cycles to clear half of the tag array entries, with a single cache entry cleared per machine cycle. The state of this bit is always read as a zero. After a hardware reset, the cache must be invalidated before it is enabled. 0 No operation 1 Invalidate all cache locations Table 4-6 describes how to set the cache invalidate all bit.
23	DISI	Disable instruction caching. When set, this bit disables instruction caching. This bit, along with the CENB (cache enable) and DISD (disable data caching) bits, control the cache configuration. See the CENB definition for a detailed description. 0 Do not disable instruction caching 1 Disable instruction caching Table 4-5 describes cache configuration and Table 4-6 describes how to set the cache invalidate all bit.