5000V Family Architectural Description

ispLSI 5000V Family Introduction

The ispLSI® 5000V Family of In-System Programmable SuperWIDE™ High Density Logic Devices is based on Generic Logic Blocks (GLBs) of 32 registered macrocells and a single Global Routing Pool (GRP) structure interconnecting the GLBs.

Outputs from the GLBs drive the Global Routing Pool (GRP) between the GLBs. Enhanced switching resources are provided to allow signals in the Global Routing Pool to drive any or all the GLBs in the device. This mechanism allows fast, efficient connections across the entire device. The enhanced GRP of the ispLSI 5000V takes care of pin locking by replacing the functions of both GRP and ORP of the previous generations of ispLSI devices with a single, highly flexible scheme.

Figure 1. ispLSI 5384VA Functional Block Diagram

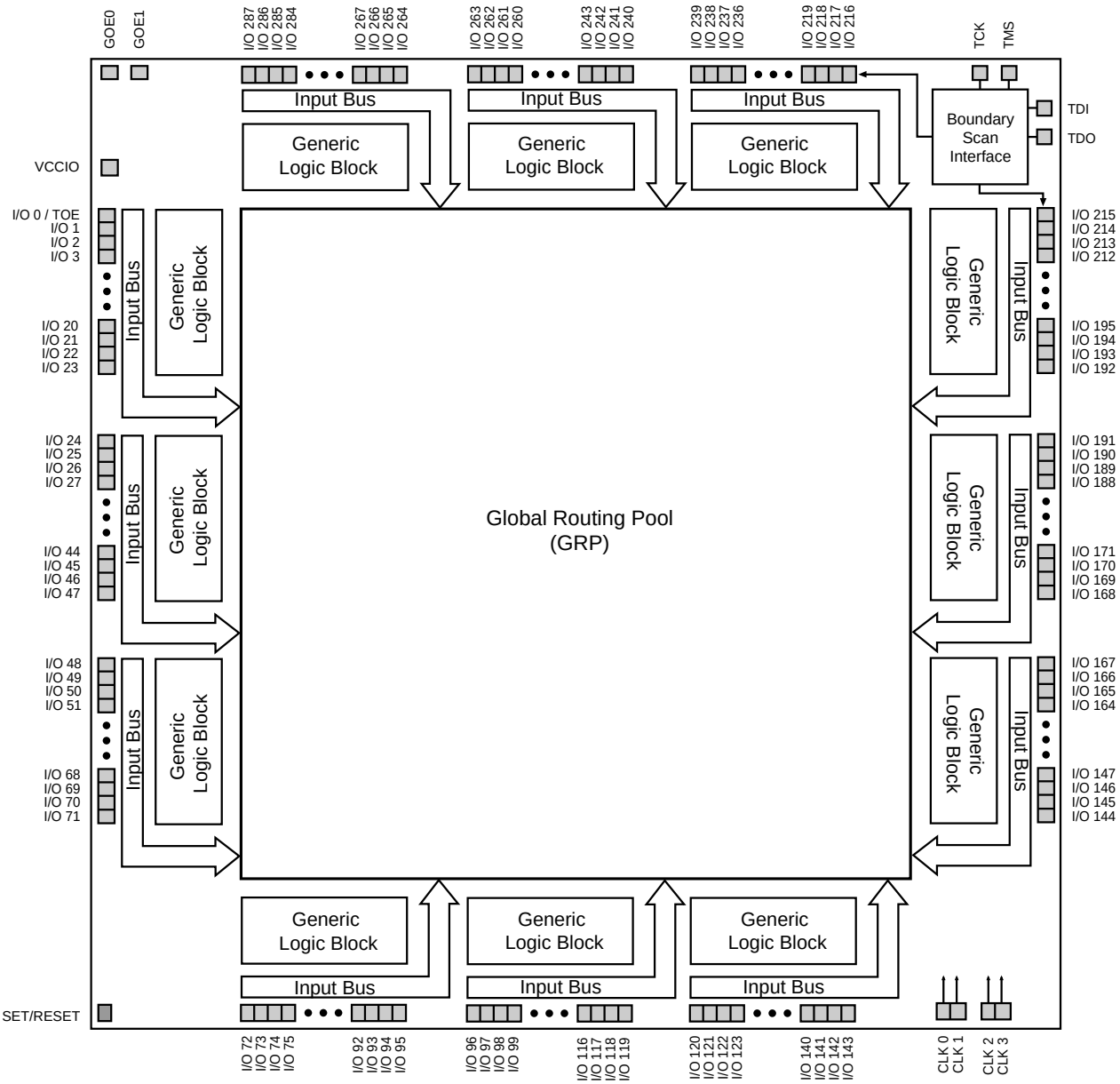
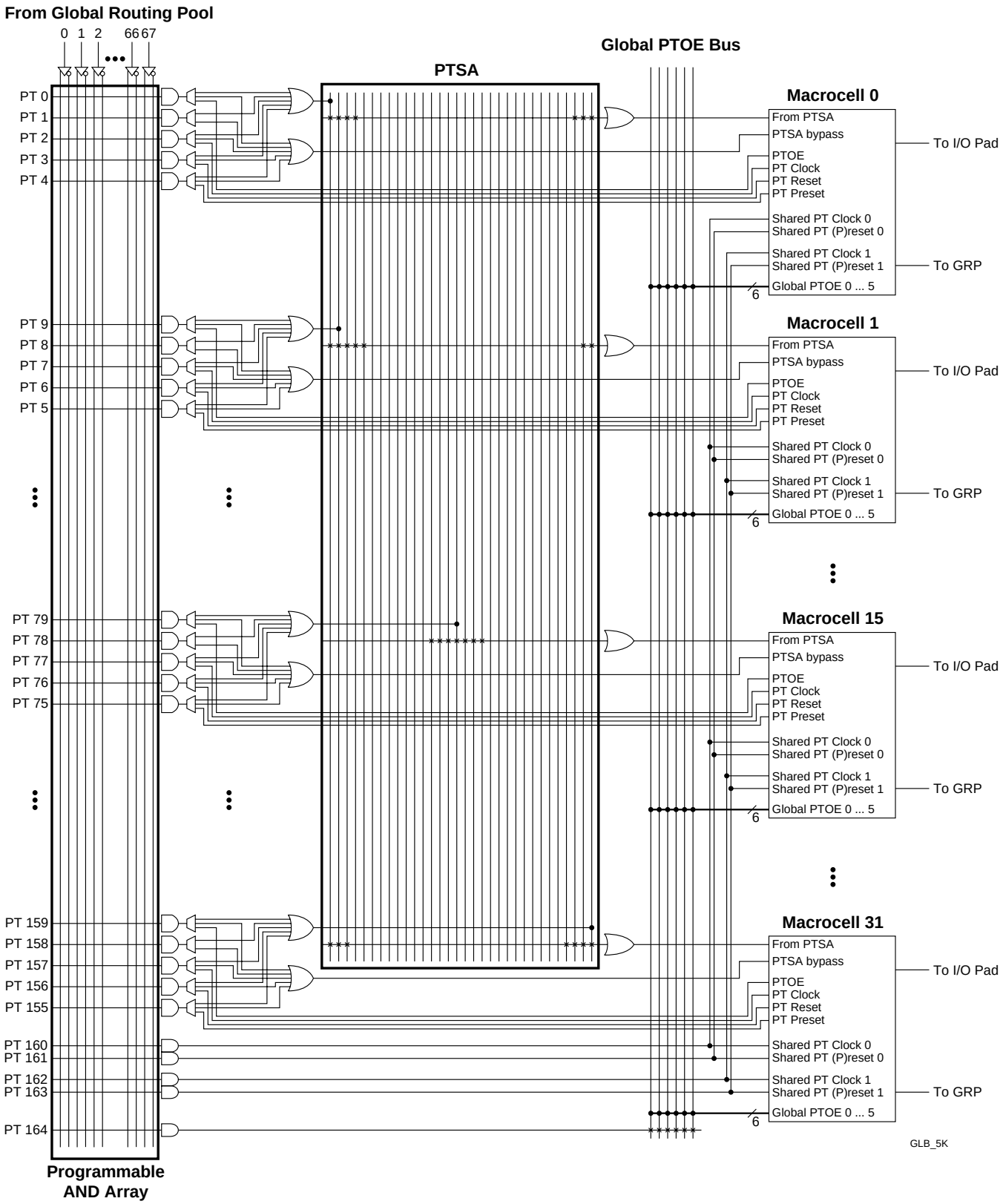


Figure 2. ispLSI 5000V GLB



Generic Logic Block

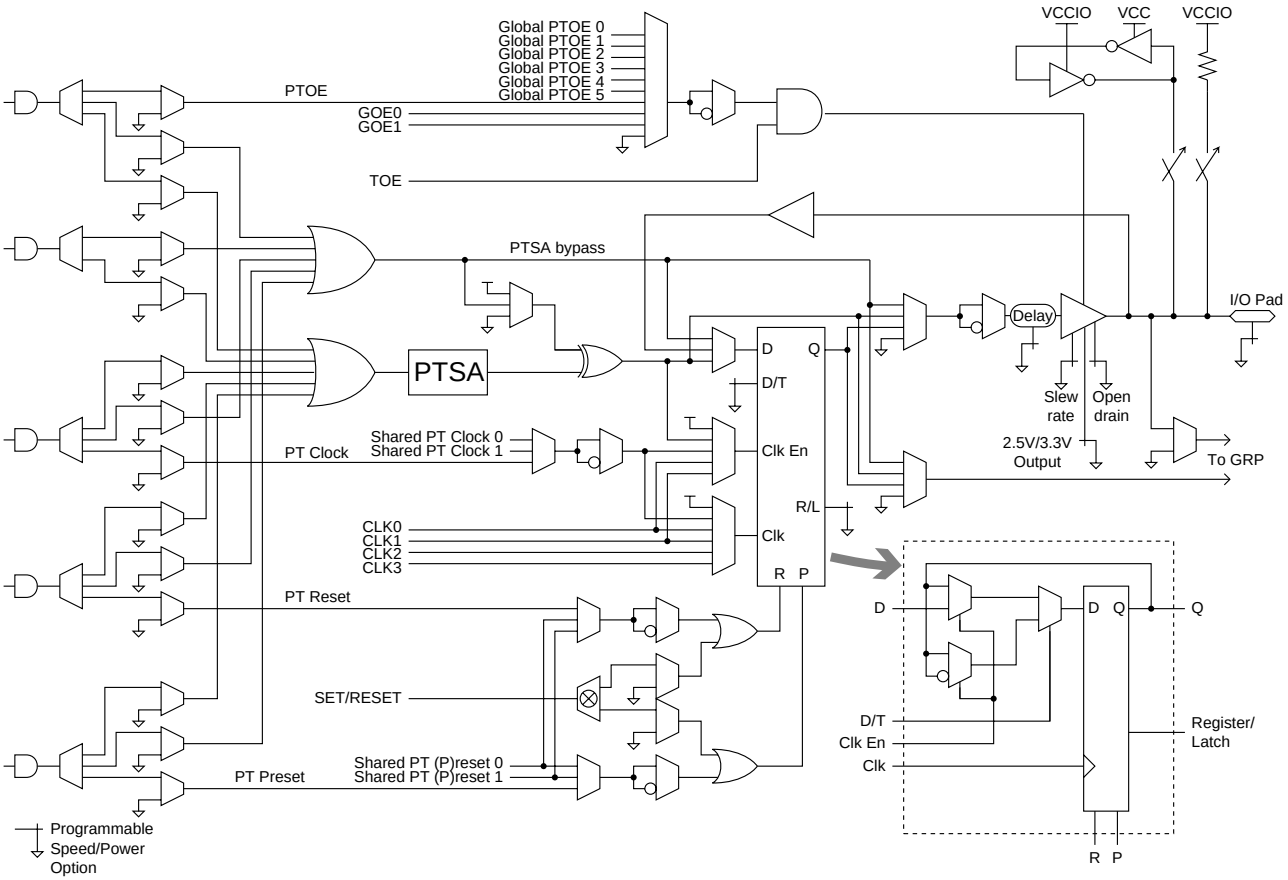
Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and 5 extra control product terms. The GLB has 68 inputs from the Global Routing Pool which are available in both true and complement form for every product term. The 160 product terms are grouped into 32 sets of five each and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 35 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of five product terms or less. The five extra product terms are used for shared GLB controls, set, reset, clock, clock enable within the GLB and for I/O output enable functions.

Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of the macrocell to construct high-speed input registers. For power management, each macrocell has a programmable High-Speed/Low-Power (HS/LP) bit. By programming this bit, DC power to each macrocell is cut by approximately 50% for an incremental delay of about 2ns. The internal timing models specify the delay increase for each speed grade device.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flipflop.

Figure 3. ispLSI 5000V Macrocell

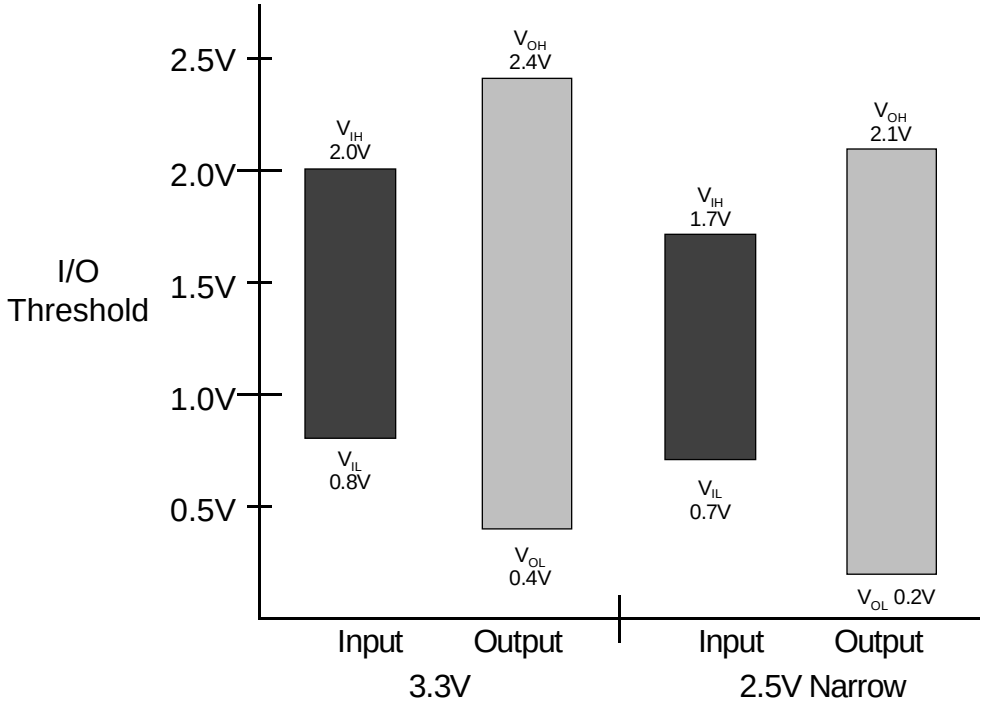


I/O Cell

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin input.

The input buffer threshold has programmable TTL/3.3V/ 2.5V compatible levels. The output driver can source 4mA and sink 8mA at 3.3V Vcc. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. Since this VCCIO pin is only a reference input, the maximum Icc for this reference VCCIO pin is limited to 45mA (for ispLSI 5384VA). The ispLSI 5000V family supports standard 3.3V and 2.5V logic levels. Figure 4 below shows the graphical representation of the logic levels. The output drivers also provide individually programmable delay, edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device. The programmable pullup and bus-hold are also configurable on each I/O pin. The combination of these extremely flexible I/O features, termed Slew-and-Skew Programmable I/O, or SASPI/O™, gives system designers the ultimate interface programmability needed by today's systems.

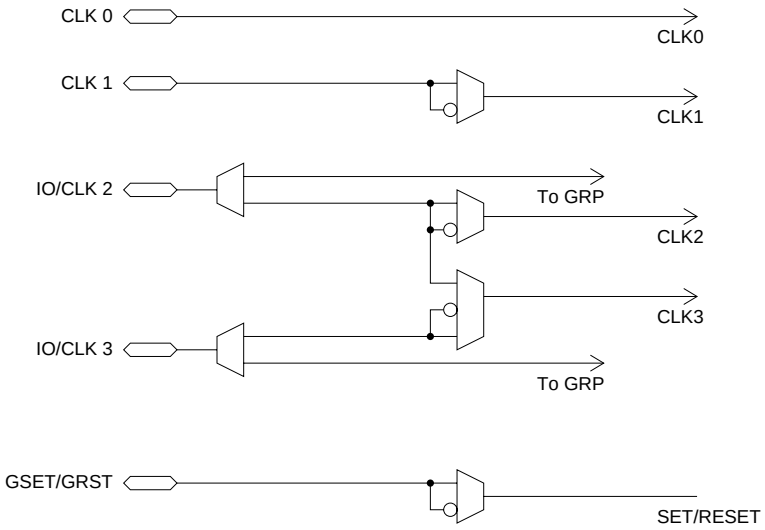
Figure 4. ispLSI 5000V I/O Logic Levels



Global Clock Distribution

The ispLSI 5000V family has four dedicated clock input pins - CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but also is available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000V Global Clock Structure



Boundary Scan and ISP

ISP™ programming of the device is performed via IEEE1149.1 compliant JTAG state machine. The programming signals are driven on the standard Test Access Port (TAP) interface. The four wire interface includes Test Data In (TDI), Test Clock (TCK), Test Mode Select (TMS), and Test Data Out (TDO). ISP program enable and disable is controlled by the private programming instruction set.

In addition to ISP programming, the JTAG state machine also provides standard boundary scan test capability. Standard boundary scan instructions supported are Sample/Preload, Extest, Bypass and High-Z instructions. The boundary scan test registers associated with each of the I/O pins control the state of the I/O pin when the device is not in normal functional mode. This feature allows users to define the state of the I/O pins during test and ISP programming modes.

Figure 6. Boundary Scan Register for I/O Pins

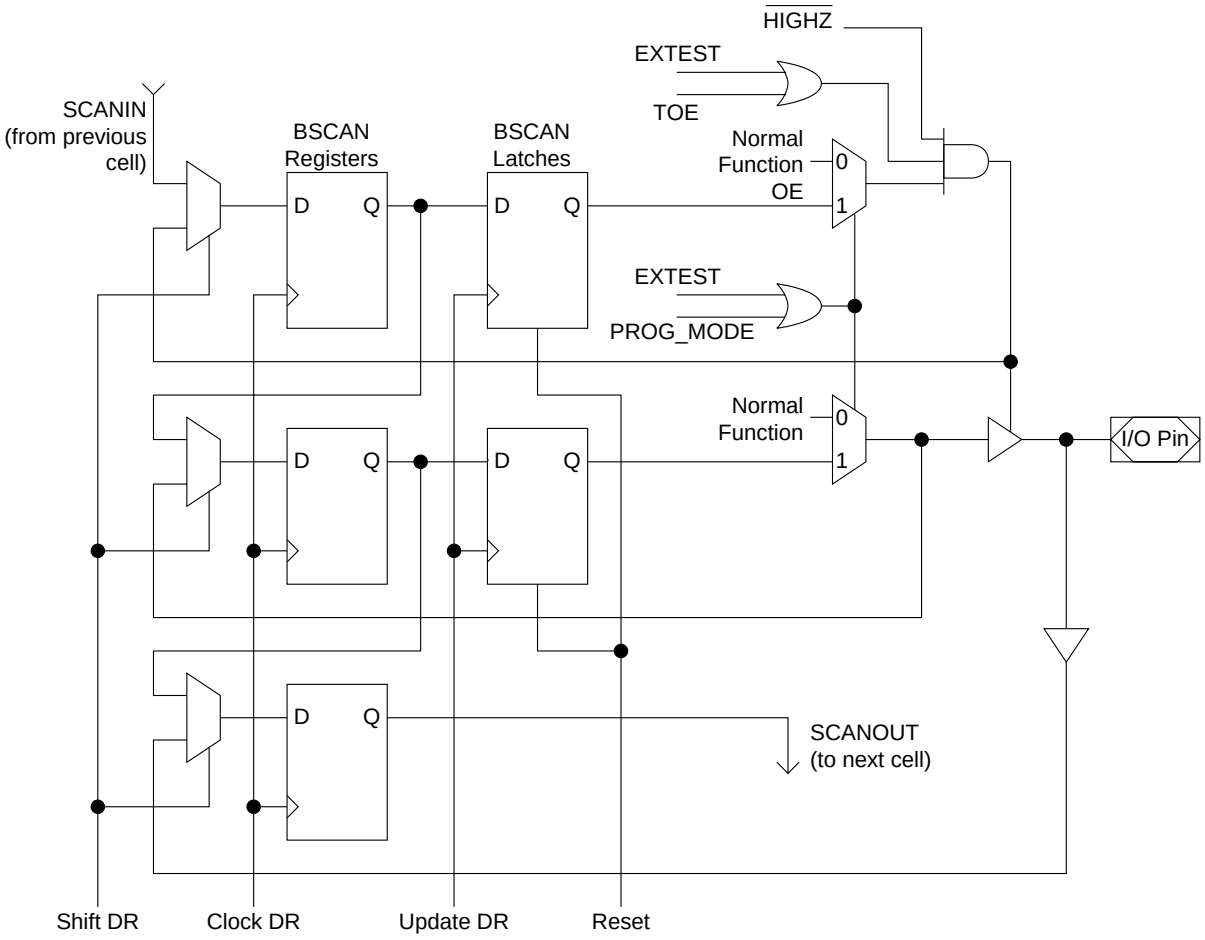
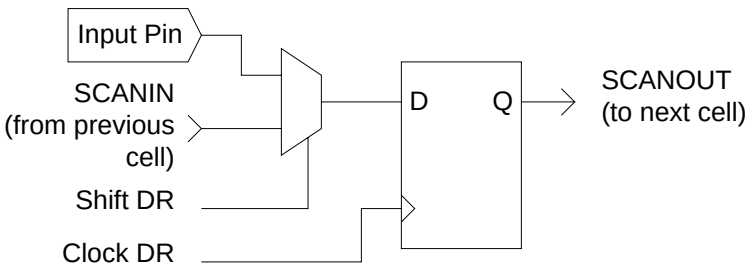


Figure 7. Boundary Scan Register for Dedicated Input Pins



Timing Model

The task of determining the timing through the ispLSI 5000V family, just as any CPLD, is relatively simple. The device timing model provided in Figure 8 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the ispDesignEXPERT™ Compiler report file, the delay path of the function can easily determined from the timing model. The software Timing Analyzer (ispTA™) reports the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 8. ispLSI 5000V Simplified Timing Model