MICROELECTRONICS

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Recommended Reading

- A.S. Sedra, K.C. Smith, “Microelectronic Circuits”, 7th Ed., Oxford University Press, 2014
- Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, Addison-Wesley 1997
- I. Sutherland, B. Sproull, D. Harris, "Logical Effort - Designing Fast CMOS Circuits", Morgan Kaufmann Publishers 1999; http://www.mkp.com/Logical_Effort
- M. Napieralska, G. Jabłoński „Podstawy mikroelektroniki” Łódź 2002, ISBN 83-89003-01-5
- http://fiona.dmcs.p.lodz.pl/micro

Syllabus

- Introduction
- The MOS Transistor
- Integrated Circuits (IC) Manufacturing Technologies
- MOS Digital Circuit Families
- Delay Calculation in CMOS Circuits – Logical Effort
- IC Design Methodologies

Microelectronics

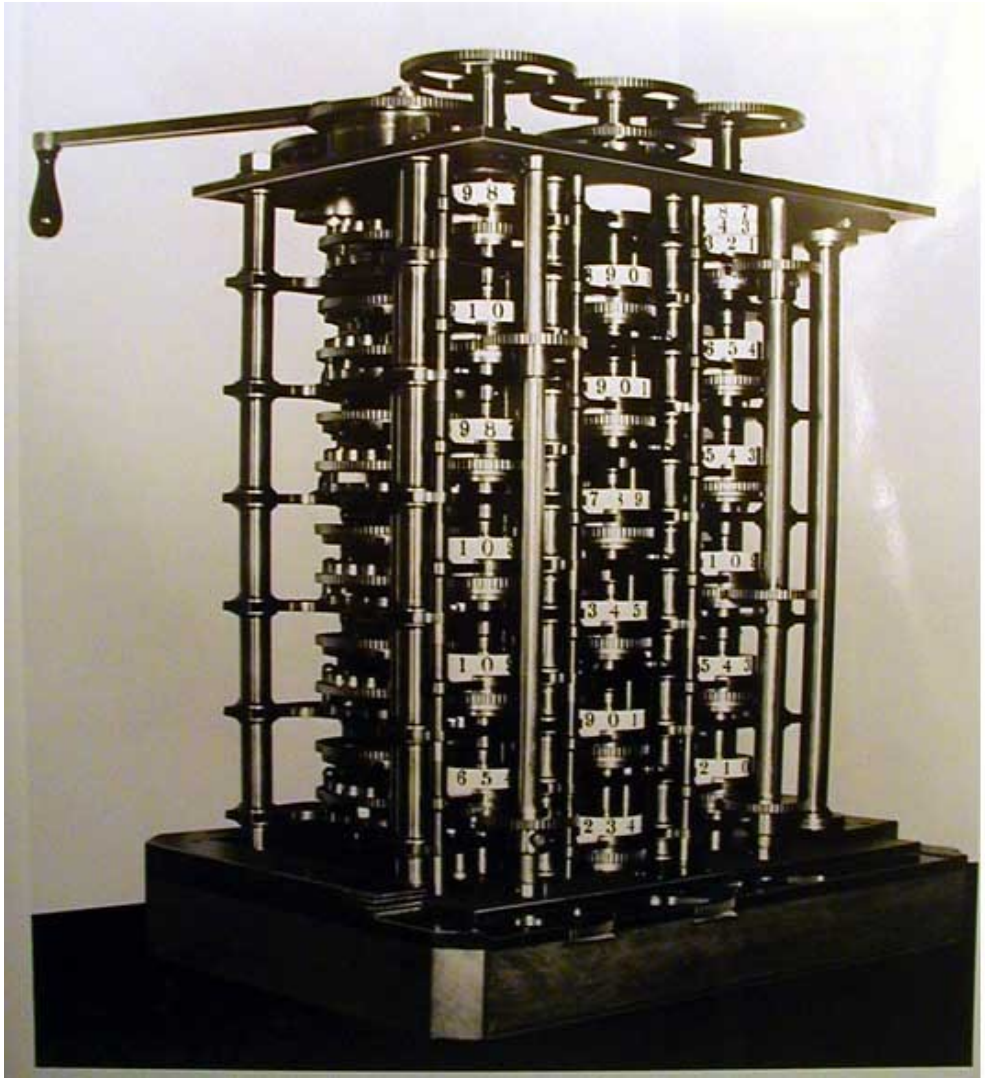
- **MICROELECTRONICS** [gr.], branch of electronics dealing with operation, construction and technology of → integrated circuits.
- **INTEGRATED CIRCUIT**, miniature electronic circuit, which part or all components are manufactured together with the interconnections in one technological cycle in or on the surface of a common substrate.

The History of Computing

Mechanical

- Abacus – 3000 BC
- Adding machine: B. Pascal – 1642
- Multiplying machine: G. Leibniz – 1694
- Difference engine: Charles Babbage 1823
- Analytical machine: Charles Babbage 1833
  - The mill (CPU), the store (memory), control, punched card reader, card puncher
  - Control from the external source (punched cards)
  - Ada (Byron) Lovelace - considered a world's first programmer

Mechanical



Elektromechanical

- Electromechanical calculator with punched cards H. Hollerith 1890.
- Electromechanical calculator Mark I 1944
  - H. Aiken: 1937-1944, USA, Harvard University + IBM
  - 750 000 components, 900 km of wires, weight 5 T
  - addition 0.3 s, multiplication 6 s

Mark II - "Computer Bug" (Grace Hopper)

Photo # NH 96566-KN First Computer "Bug", 1945

92

9/9

0800 Arctan started

1000 " stopped - arctan ✓ { 1.2700 9.037 847 025
9.037 846 795 correct

13 " (032) MP - MC ~~1.9532647000~~ ~~2.13047645 (-3)~~ 4.61592505 9(-2)

(033) PRO 2 2.13047645

correct 2.13067645

Relays 6-2 in 033 failed special speed test
In relay " " 10.00 test.
Relays changed

1100 Started Cosine Tape (Sine check)

1525 Started Mult + Adder Test.

1545  Relay #70 Panel F
(moth) in relay.

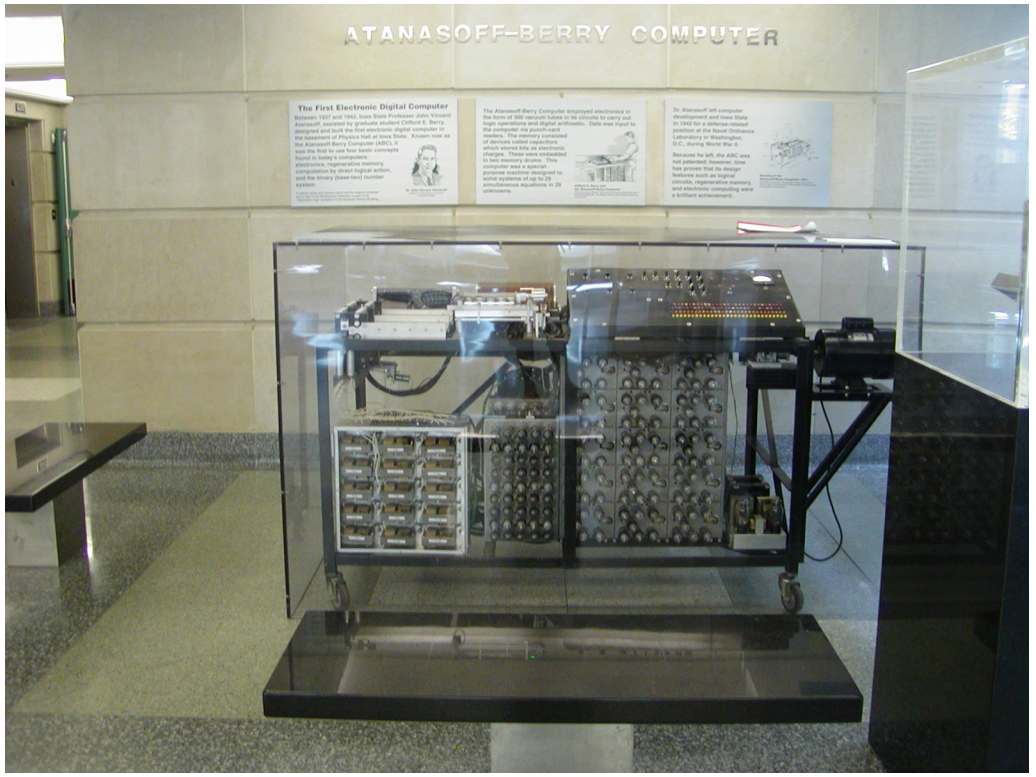
First actual case of bug being found.

~~1645~~ 1700 Arctangent started.

1700 closed down.

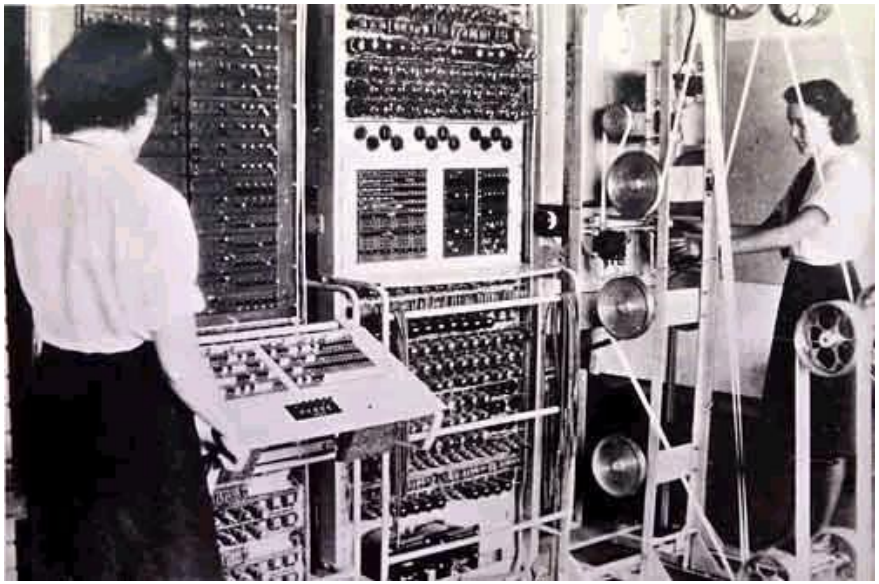
Electronic

- 1941 – John Atanasoff and Clifford Berry - ABC (calculator) – vacuum tubes



Electronic

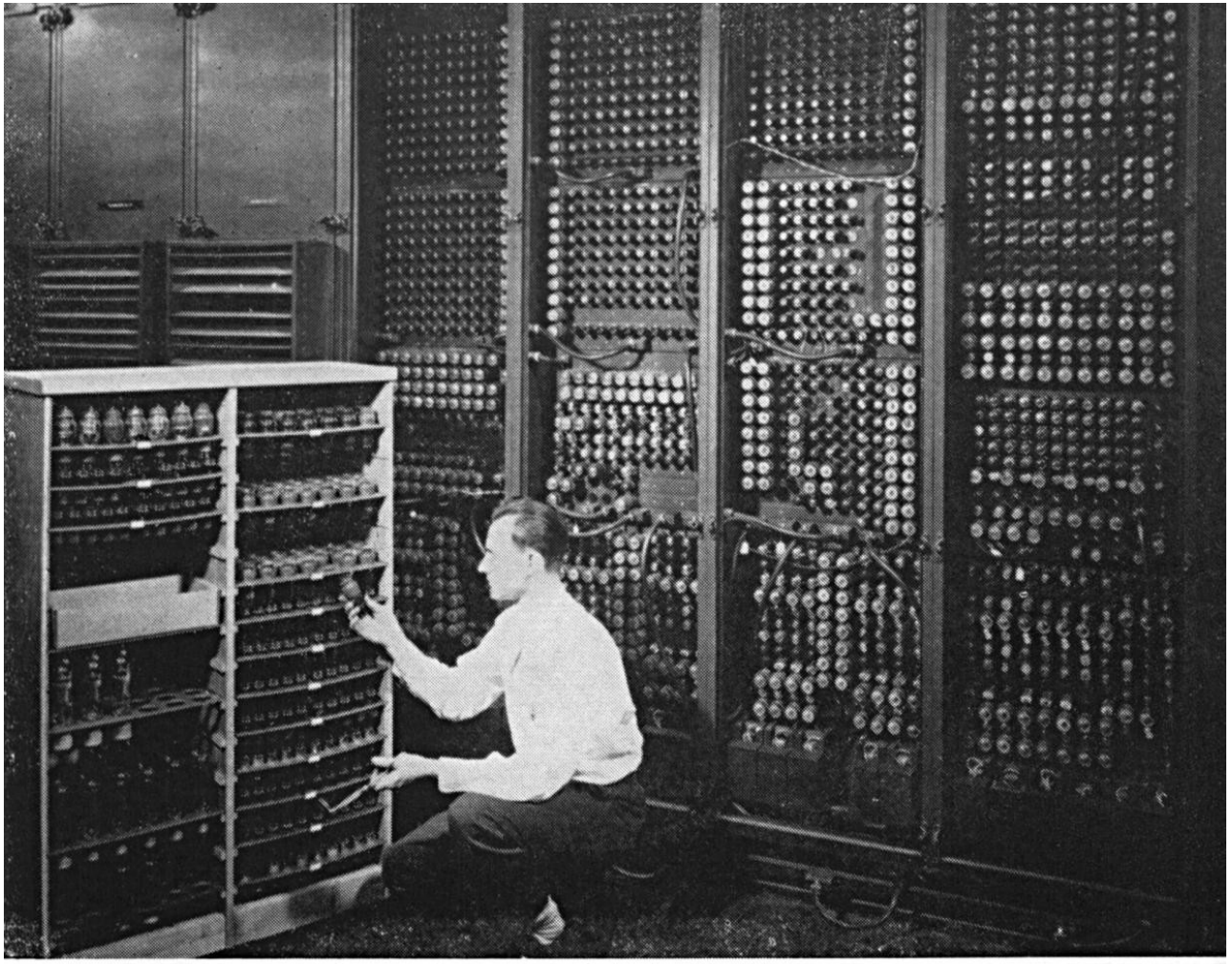
- 1943 – Colossus - code cracking calculator (1500 vacuum tubes)
  - data on perforated paper tape
- 1944 – Colossus 2 (2500 tubes)



I Generation Computers (1945-1953)

- 1943-1946 – ENIAC – the first electronic computer
  - Electronic Numerical Integrator And Computer
  - John Eckert, John Mauchly
  - 18 000 vacuum tubes, 70 000 resistors, 1500 relais, weight 30 T,
  - Power consumption 174 kW, cost 750 000 $
  - Addition: 0.2 ms
  - Numbers encoded in decimal, every digit stored in 10-position counter (36 tubes), 10 digits stored in an accumulator.
    - The whole machine: 20 accumulators.
  - The control of the machine operation: setting 10-position electric switches

ENIAC

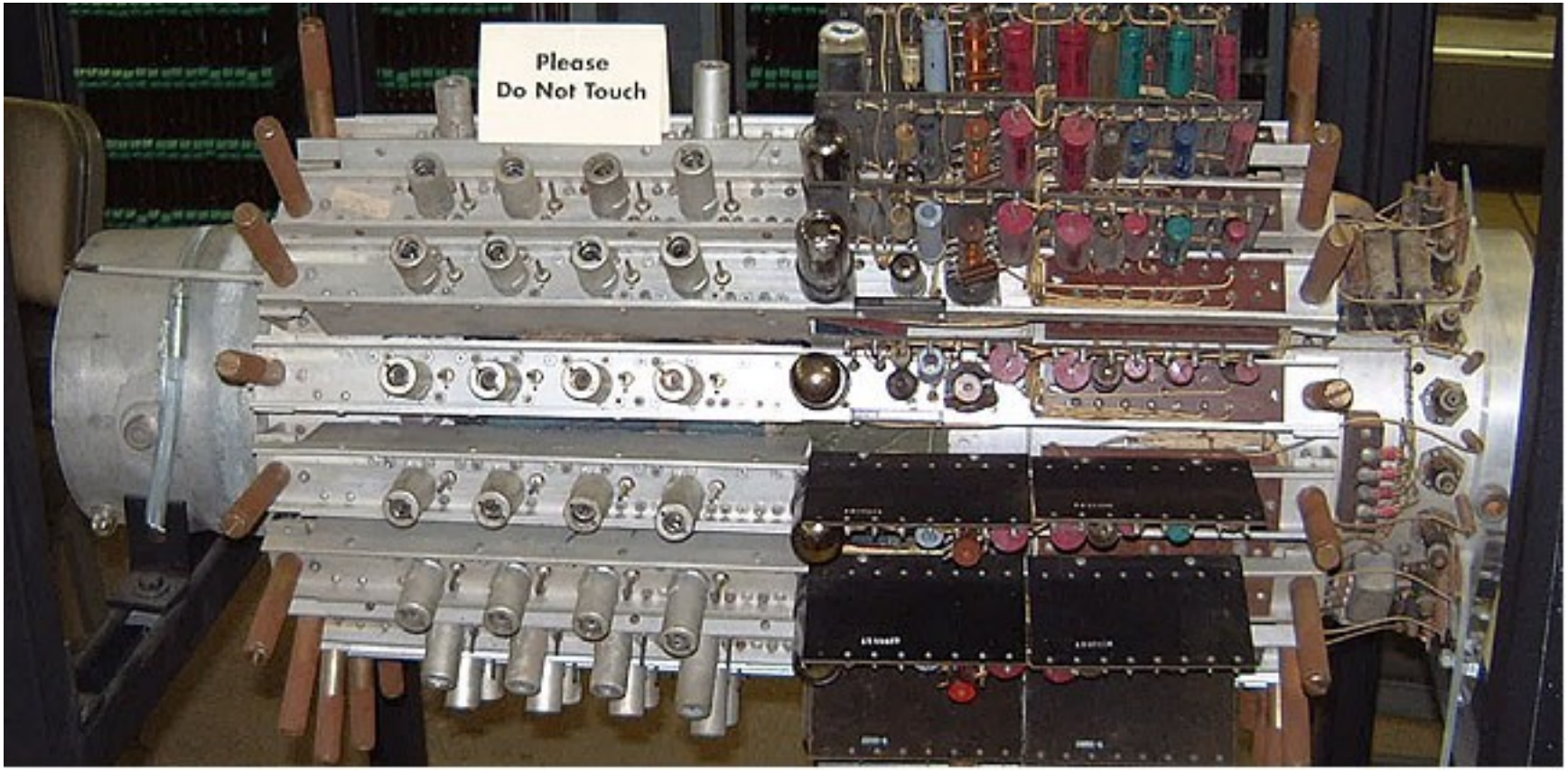


Replacing a bad tube meant checking among ENIAC's 19,000 possibilities.

I Generation Computers

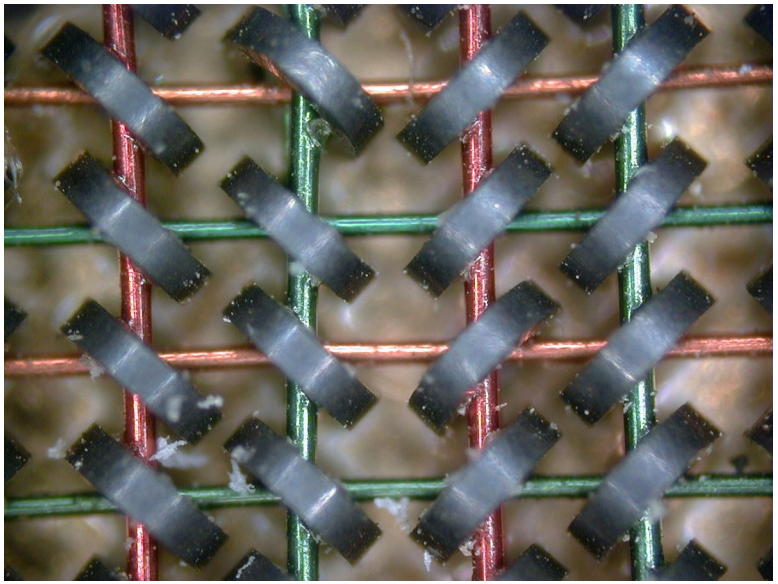
- 1944 – 1949 EDVAC John von Neumann et al
- Electronic Discrete Variable Automatic Computer
  - stored program machine;
  - basic components:
    - arithmetical and logical unit, memory, input, output, control
    - binary system
    - memory - mercury delay line
- 1951 – UNIVAC I - first successfull commercial computer

Mercury Memory



II Generation Computers (1954-1964)

- Technology:
  - digital circuits: transistors
  - memories: drum memory (initially), ferrite memory



III Generation Computers (1965-1971)

- Technology:
  - Digital circuits: low and medium scale of integration integrated circuits
  - Memories: ferrite memory (initially), integrated circuits

III Generation Computers

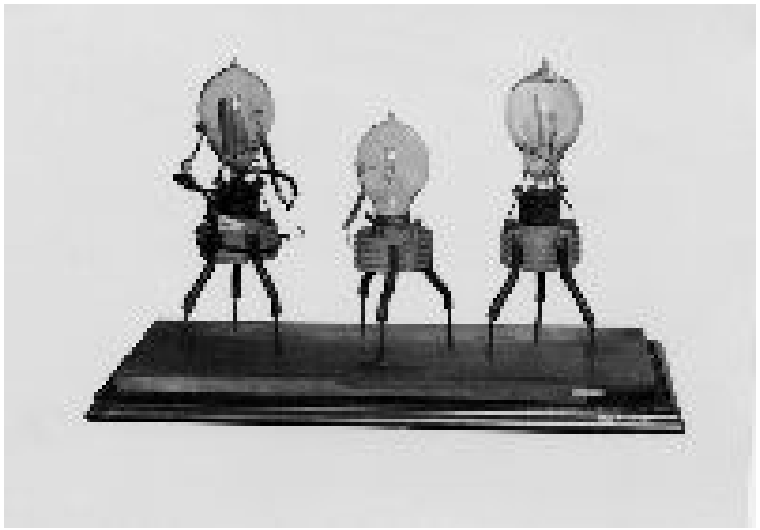
- Interesting dates:
  - 1965 – IBM 360
  - 1971 – IBM 370 - 70 % of computer market
  - 1968 – PDP-8 - 12-bit minicomputer with a bus architecture
  - 1970 – PDP 11 - 16-bit minicomputer with a bus architecture
  - 1972 – Illiac IV - matrix computer with 64 processing units

IV Generation Computers (1971 - now)

- Technology:
  - Digital circuits: very-large scale of integration digital circuits
  - Memories: VLSI circuits

History of Electronics

1904

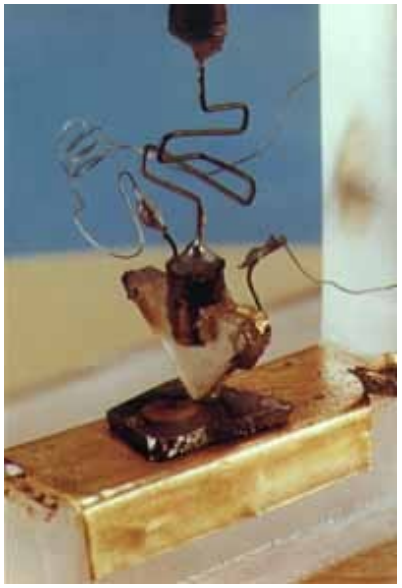


Ambrose Fleming at Marconi Company patents the two-electrode radio rectifier, which he called the thermionic valve; it is also known as the vacuum diode, kenotron, thermionic tube, and Fleming valve.

1906

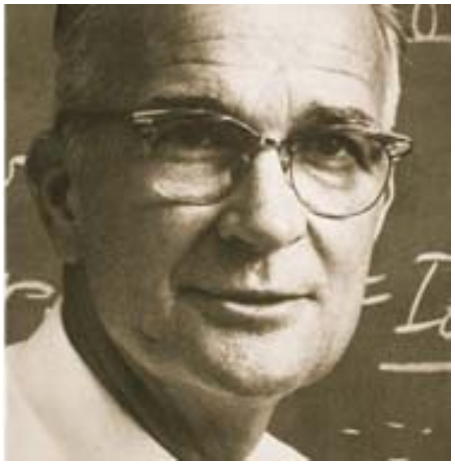
Lee De Forest devises a three-electrode tube, or triode; the device is capable of detecting and amplifying radio signals. It was also known as an 'Audion valve‘.

1947



On December 23, 1947 William Shockley, Walter Brattain and John Bardeen at Bell Labs demonstrate their new invention of the point-contact transistor amplifier. The name transistor is short for "transfer resistance".

1955



William Shockley, co-inventor of the transistor seven years earlier, founds Shockley Semiconductor Laboratories in Santa Clara Valley. He recruits 12 young scientists dedicated to the use of germanium and silicon for transistors -- his “Ph.D. production line.” Shockley wins the Nobel Prize for Physics in 1956, but his management style and disenchantment with pure research causes the eight young scientists to leave company.

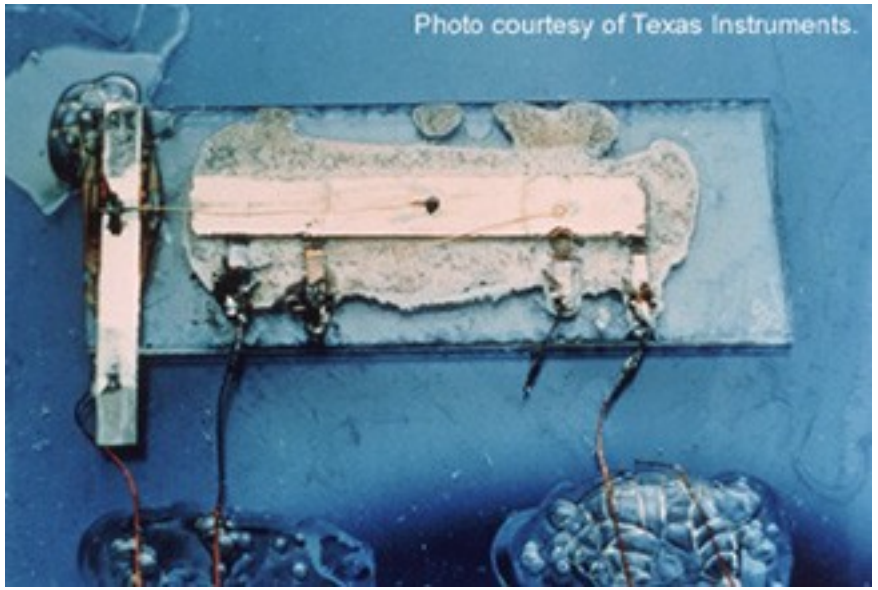
1957

Gordon E. Moore, C. Sheldon Roberts, Eugene Kleiner, Robert N. Noyce, Victor H. Grinich, Julius Blank, Jean A. Hoerni and Jay T. Last - the “Traitorous Eight” from Shockley Semiconductor - use $3500 of their own money to develop a method of mass-producing silicon transistors using a double diffusion technique and a chemical-etching system.

The silicon and germanium mesa allows manufacturers to produce multiple transistors on a single wafer.

Fairchild Camera and Instrument Corporation invests $1.5 million in return for an option to buy the company within eight years. On October 1, 1957, Fairchild Semiconductor is born. The new company is profitable in six months with the help of its first sale: an order from IBM™ for 100 transistors at $150 a piece.

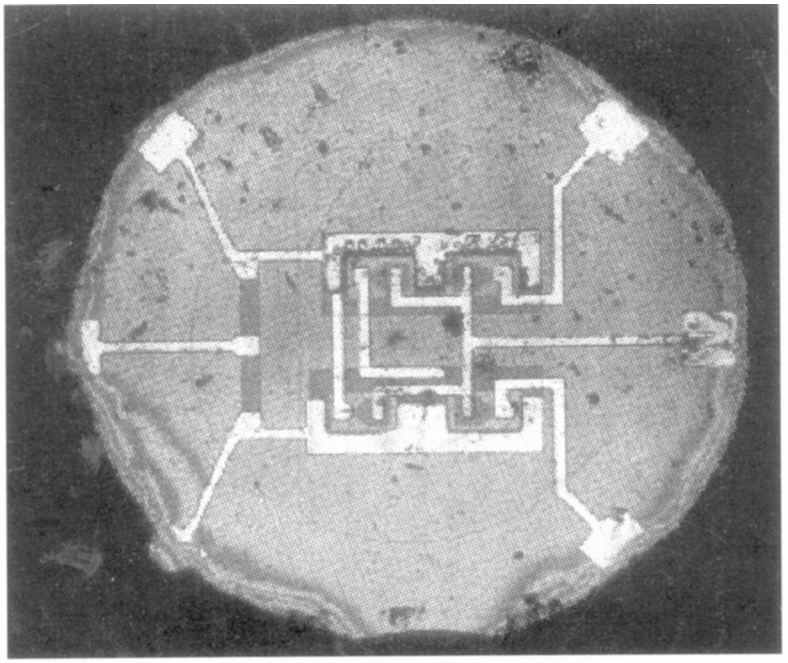
1958



At Texas Instruments, Jack Kilby builds the first integrated circuit – an oscillator consisting of one transistor, two resistors and one capacitor – all of them made of germanium.

On September 12, 1958, Texas Instruments executives gathered around Kilby's oscillator, a complete circuit on a chip less than half an inch long. Kilby pushed the switch, and a bright green thread of light snaked across the screen. The integrated circuit worked, and a new era in microelectronics was born.

1959

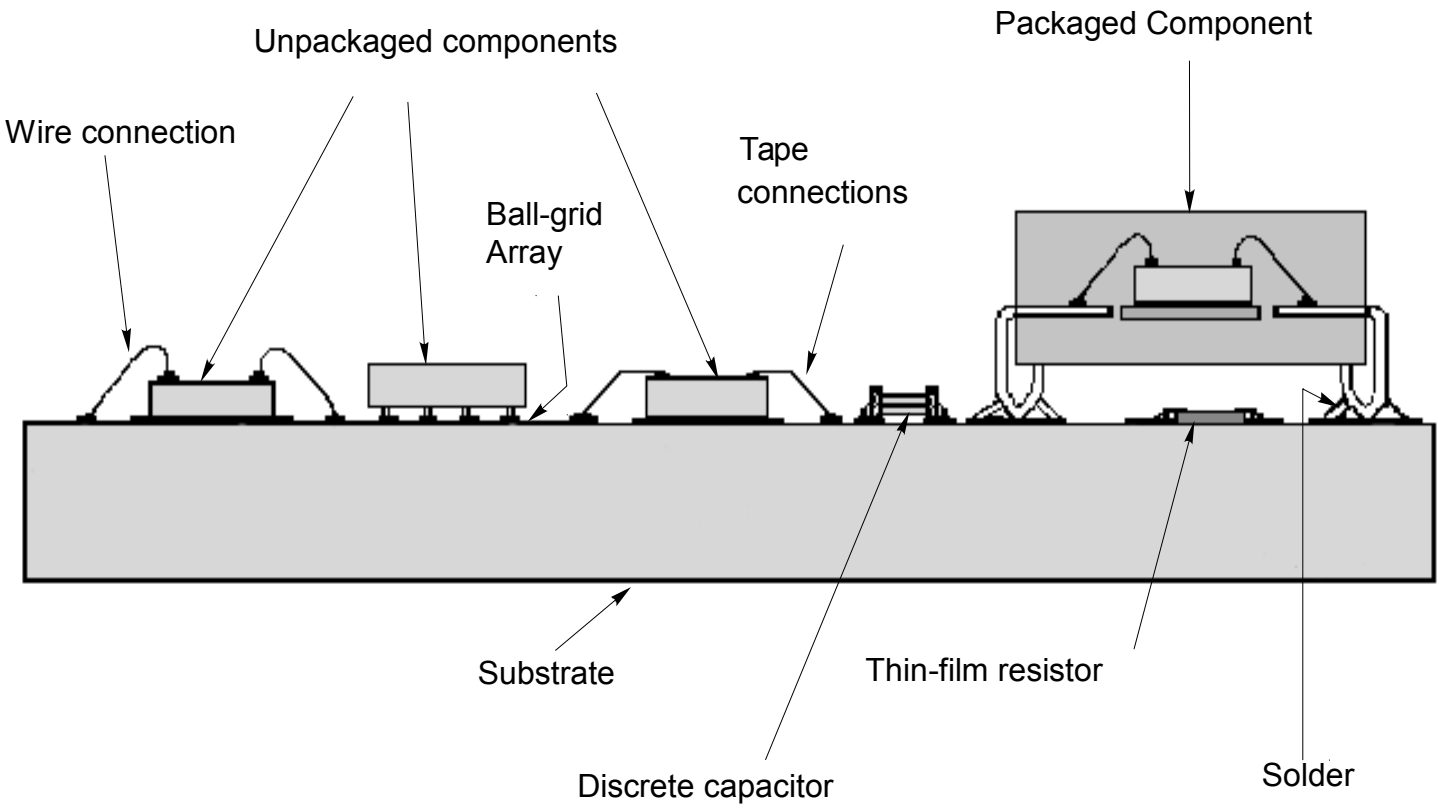


Jean Hoerni at Fairchild Semiconductors invents a planar transistor, where a collector, base and emitter are all on one plane. Using this device, Robert Noyce develops the monolithic integrated circuit -- a flip-flop consisting of six devices on a fingernail-size wafer of silicon. Today, nearly fifty years later, the planar process is the primary method for producing transistors.

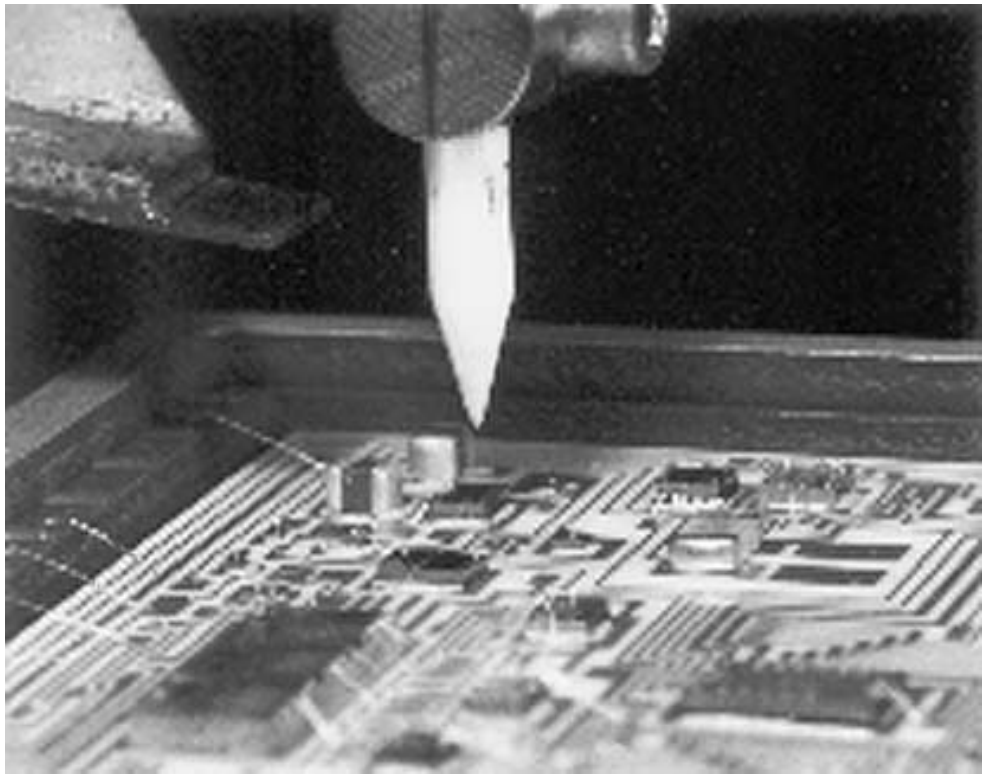
Types of Integrated Circuits

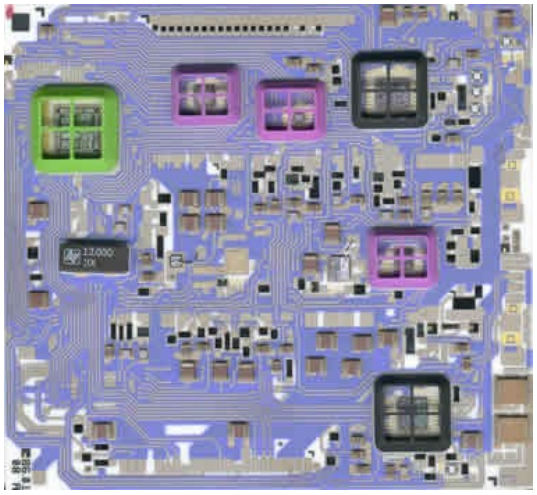
- Hybrid
  - Thick-film
  - Thin-film
- Monolithic

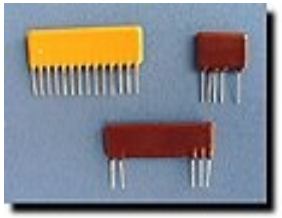
Thick-Film Circuits



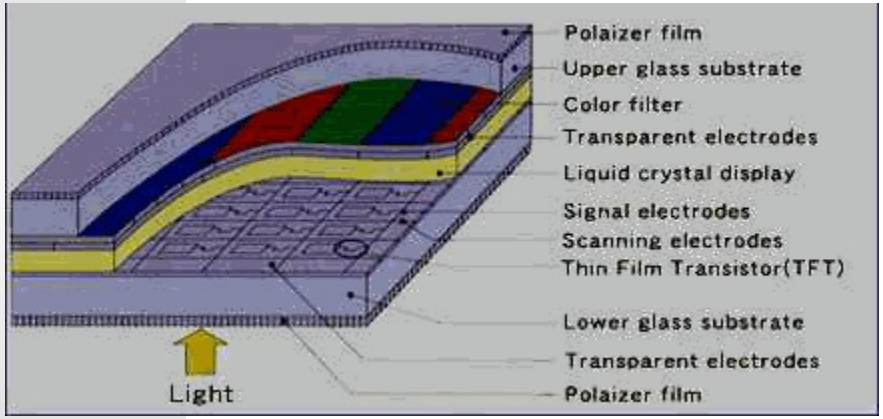
Thick-Film Circuits



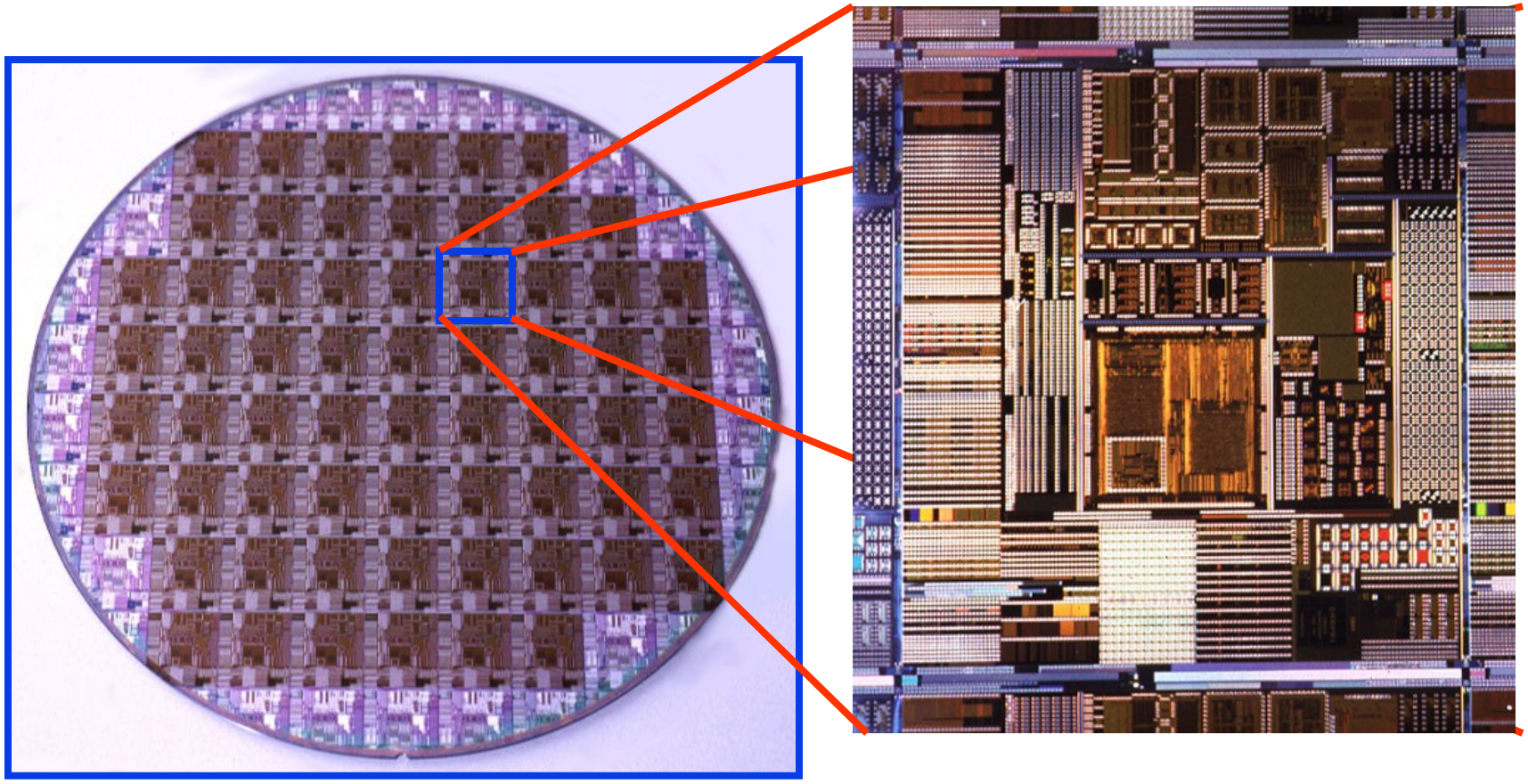




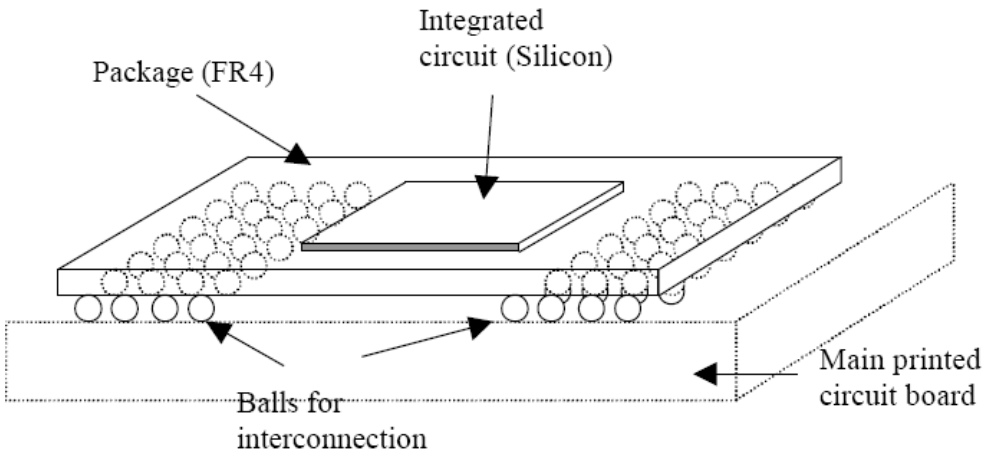
Thin-Film Circuits

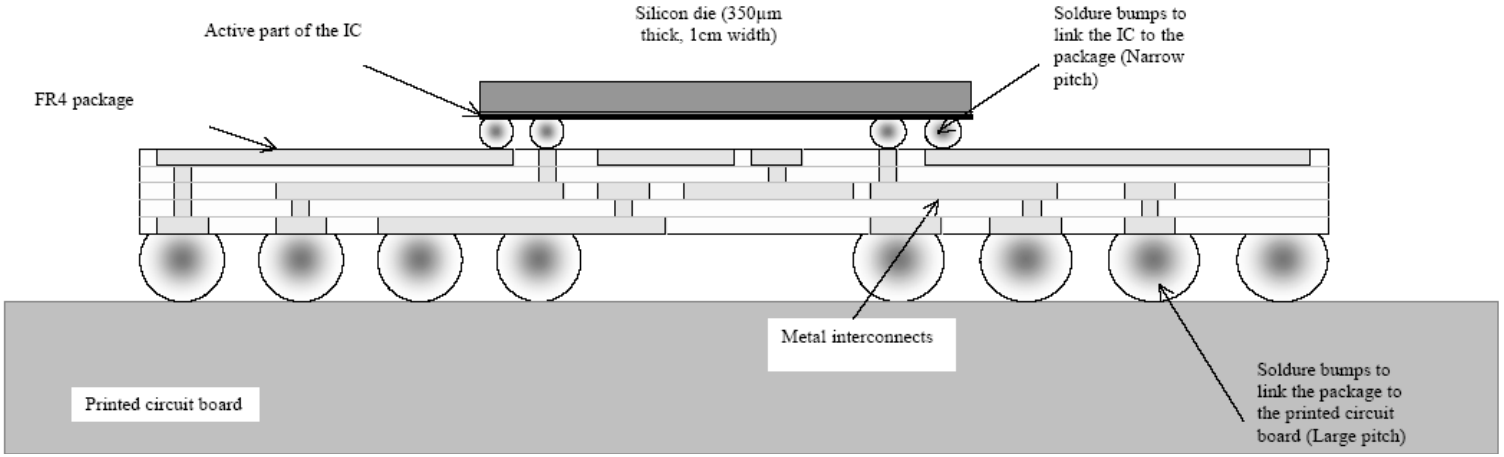


Monolithic Circuits



Monolithic Circuits





Advantages of Integrated Circuits

- Low cost
- Low size
- High quality and reliability
- Same temperature characteristics of all the components

IC Development

- The 60's: First ICs
- The 70's: Microprocessors
- The 80's: ASICs (Application Specific Integrated Circuits)
- The 90's: Micro Electro-Mechanical Systems (MEMS)
- The 2000's: System on Chip

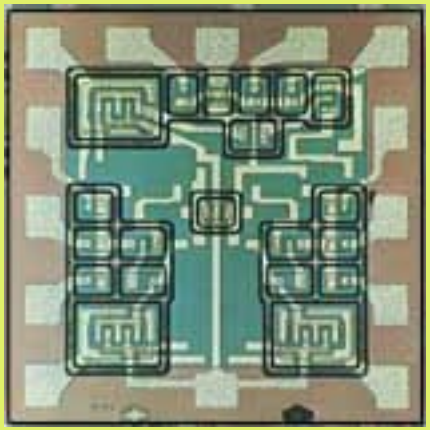
The 60's – First ICs

1958 First IC (J. Kilby - T.I.)

1960 First comercial IC - logic RTL circuits MICROLOGIC - (Fairchild)

1964 TTL circuits (series 54 i 74 - Texas Instruments)

1965 First Operational Amplifier µA 702 - (Fairchild)

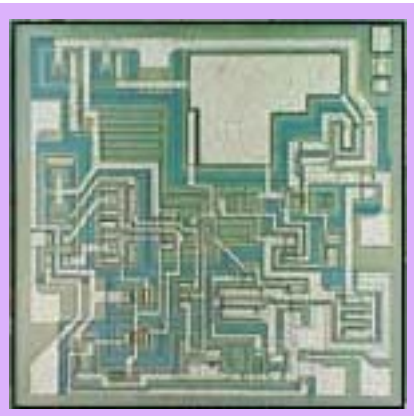


1967 OPAMP with high input impedance µA 709, first comparator µA 710

1967 First ROM memory 64 bits - (MOS technology, Fairchild)

1968 µA 741

1968 OPAMP with input JFET transistors



1968 CMOS technology (RCA), calculators, watches, …

1968 ROM memory 1024 bits (PHILCO)

The 70's - Microprocessor Development

1971 INTEL first commercial 4 bit microprocessor 4004, with 45 instructions. PMOS Technology, 2300 transistors

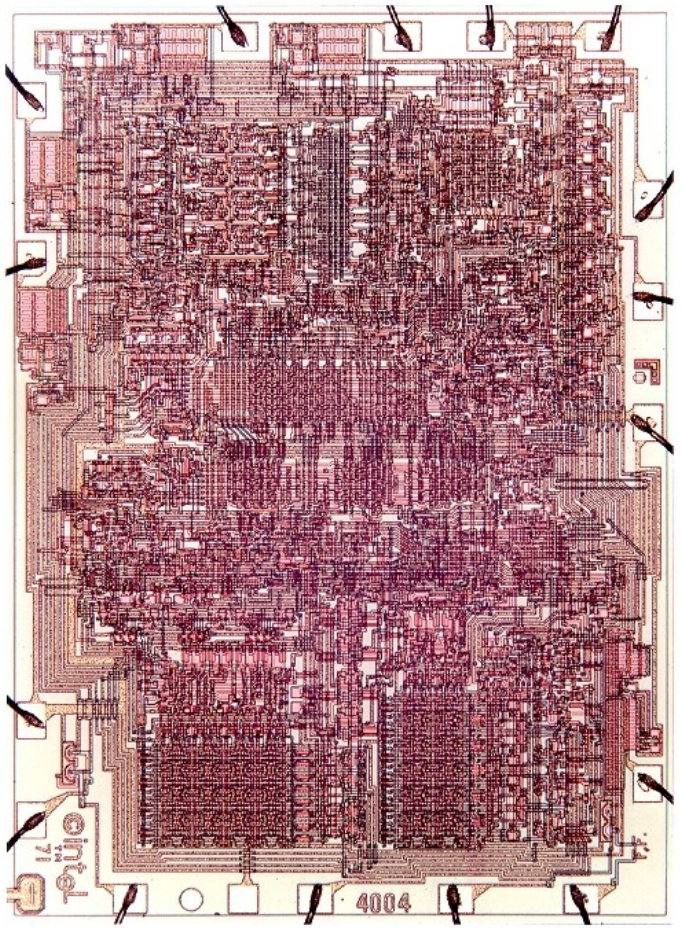
1972 First 8 bit microprocessor 8008 (INTEL).

1973 INTEL 8080, NMOS technology, improved by Zilog - Z80

1974 First CMOS microprocessor- 1802 (RCA).

1974 MOTOROLA 6800 - single 5V supply voltage.

1976 First microcontroller 8048 (INTEL).



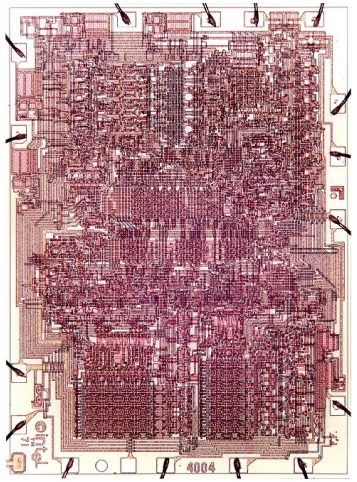
Intel 4004

2,300 transistors

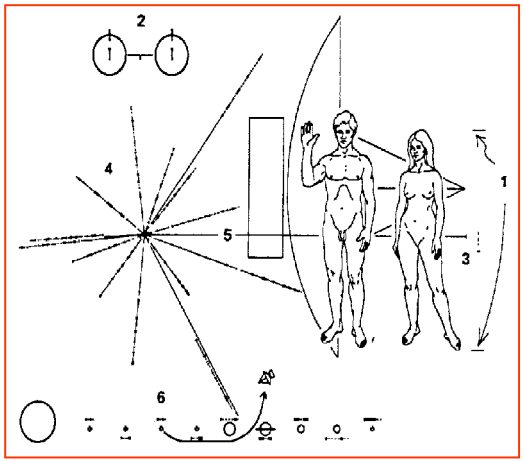
10-micron technology
46 instructions
40,000 instructions per second
4-bit data/address bus.
4-bit accumulator with separate carry and test bits,

Sixteen 4-bit 'scratch-pad' registers (which can be used as eight 8-bit registers),

A 12-bit PC (program counter), and three more 12-bit registers comprising an address stack

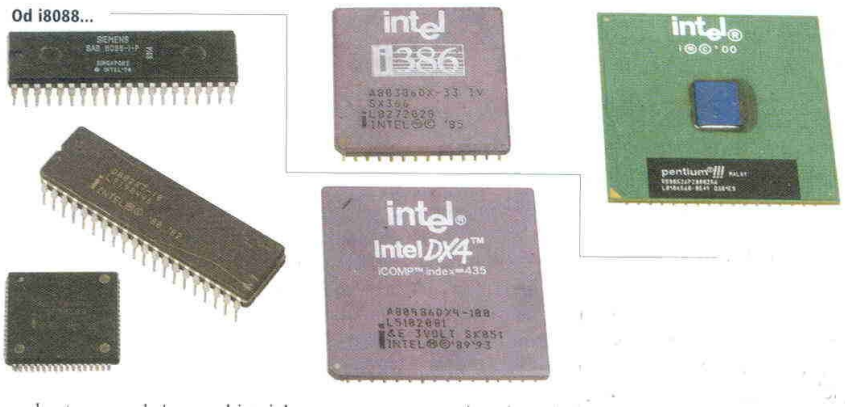


In 1972 on board of Pioneer 10, until 1998 the most distant human-made object (currently Voyager 1)



INTEL Processors

1978 INTEL 8086
1982 INTEL 80286
1989 INTEL 80486
1993 INTEL Pentium
1999 INTEL Pentium III
2000 INTEL Pentium 4
2004 INTEL Itanium 2
2006 INTEL Core Duo Processor
2007 INTEL Core 2 Quad Processor



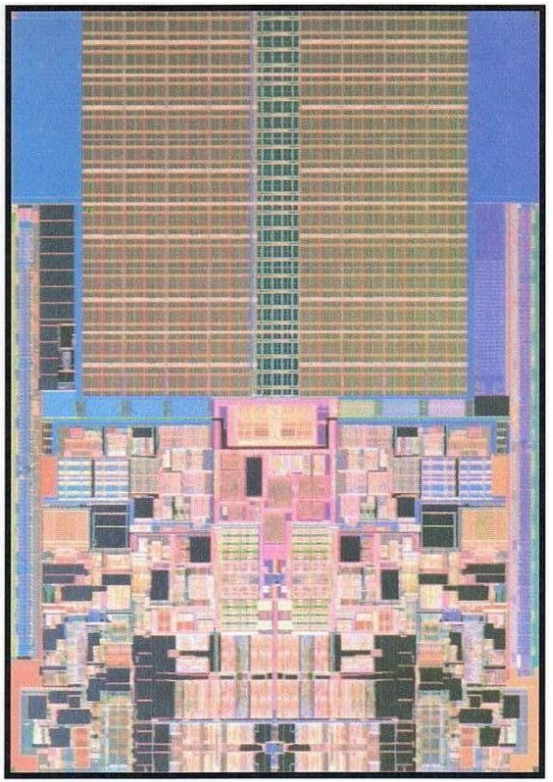
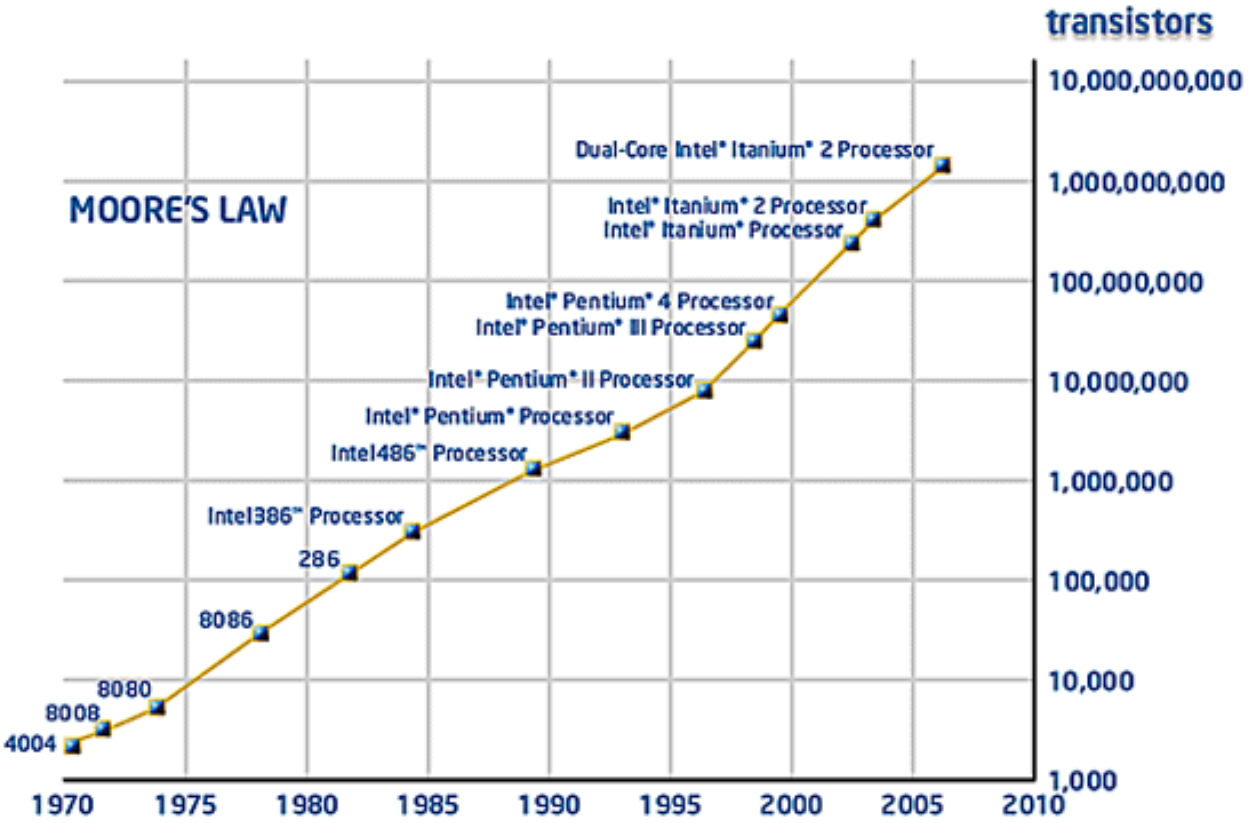


Photo of a die of dual-core Intel Penryn processor (45 nm) introduced in second half of 2007

Number of Transistors in Different Processors

Year of introduction	Processor	Number of transistors
1971	4004	2,300
1972	8008	2,500
1974	8080	4,500
1978	8086	29,000
1982	Intel286	134,000
1985	Intel386™ processor	275,000
1989	Intel486™ processor	1,200,000
1993	Intel® Pentium® processor	3,100,000
1997	Intel® Pentium® II processor	7,500,000
1999	Intel® Pentium® III processor	9,500,000
2000	Intel® Pentium® 4 processor	42,000,000
2001	Intel® Itanium® processor	25,000,000
2002	Intel® Itanium® 2 processor	220,000,000
2004	Intel® Itanium® 2 processor (9MB cache)	592,000,000
2006	Dual-Core Intel Itanium 2	1,720,000,000
2010	Quad-Core Intel Itanium	2,046,000,000

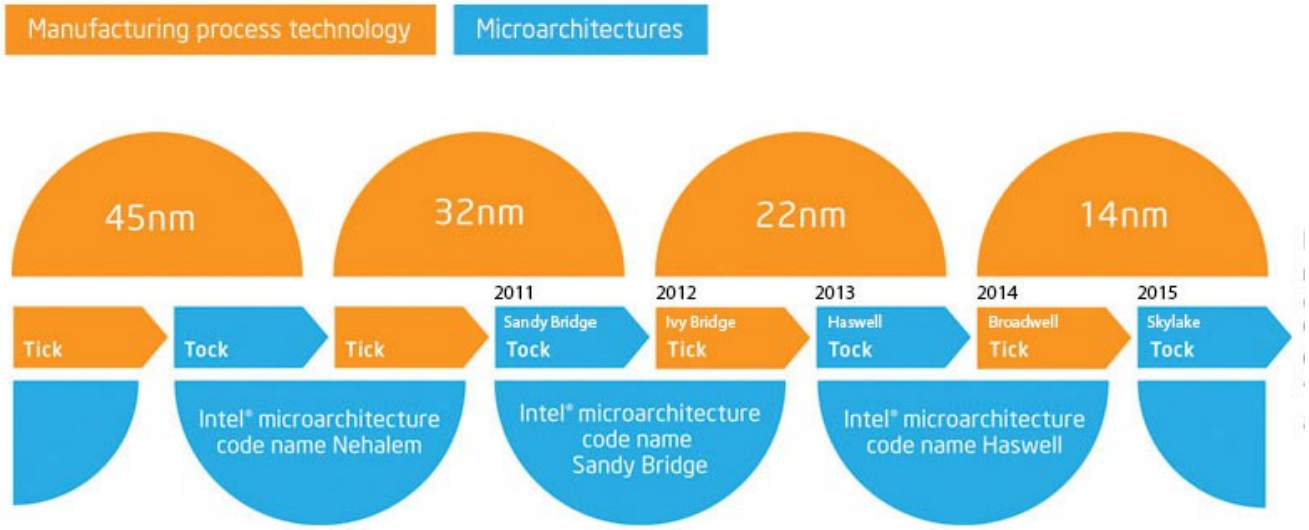
Moore's Law



Moore's Law (1965) – number of transistors in an integrated circuit doubles every 18 months

http://www.intel.com/technology/mooreslaw/index.htm

Intel Tick-Tock Strategy



2010 — Westmere 32nm

- ULV processors
- Turbo
- Integrated Gfx on Package
- Power Control Unit
- Power Gates
- Increased Parallelism & Hyper-Threading

2011 — Sandy Bridge 32nm

- Integrated On-die Gfx
- More Aggressive Turbo
- Core/Gfx Power Balancing
- Platform Power Limits
- More efficient OoO Engine

2012 — Ivy Bridge 22nm

- 22nm Tri-gate Transistor
- Improved Perf at Low V
- Configurable TDP
- Increased 3D Gfx Perf
- DirectX11 Support

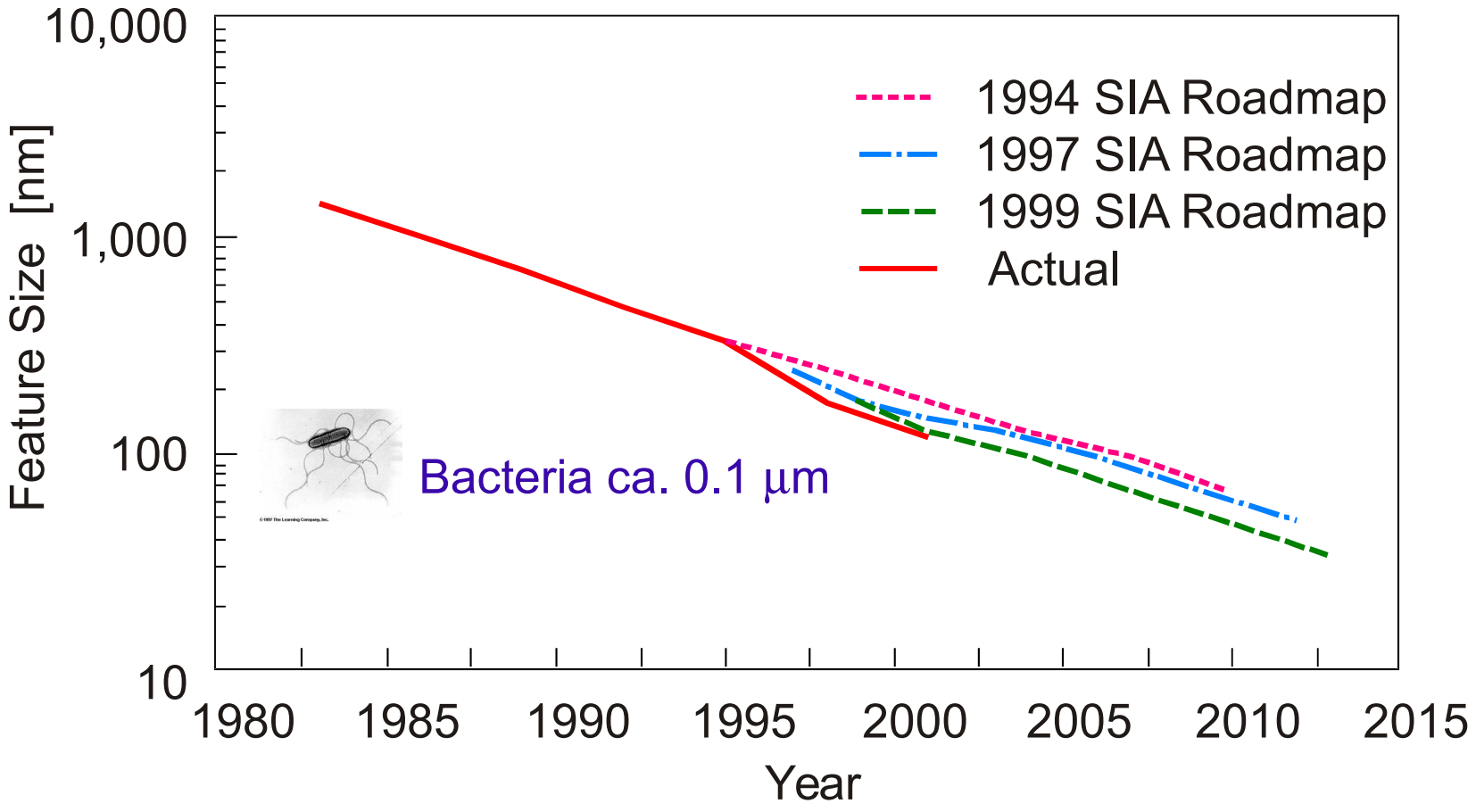
2013 — Haswell 22nm

- ULT Process Optimization
- 2X Battery life
- 20X Idle power reduction
- Chipset MCP Integration
- Low Latency Idle States
- New FIVR
- Increased Dynamic Operating Range

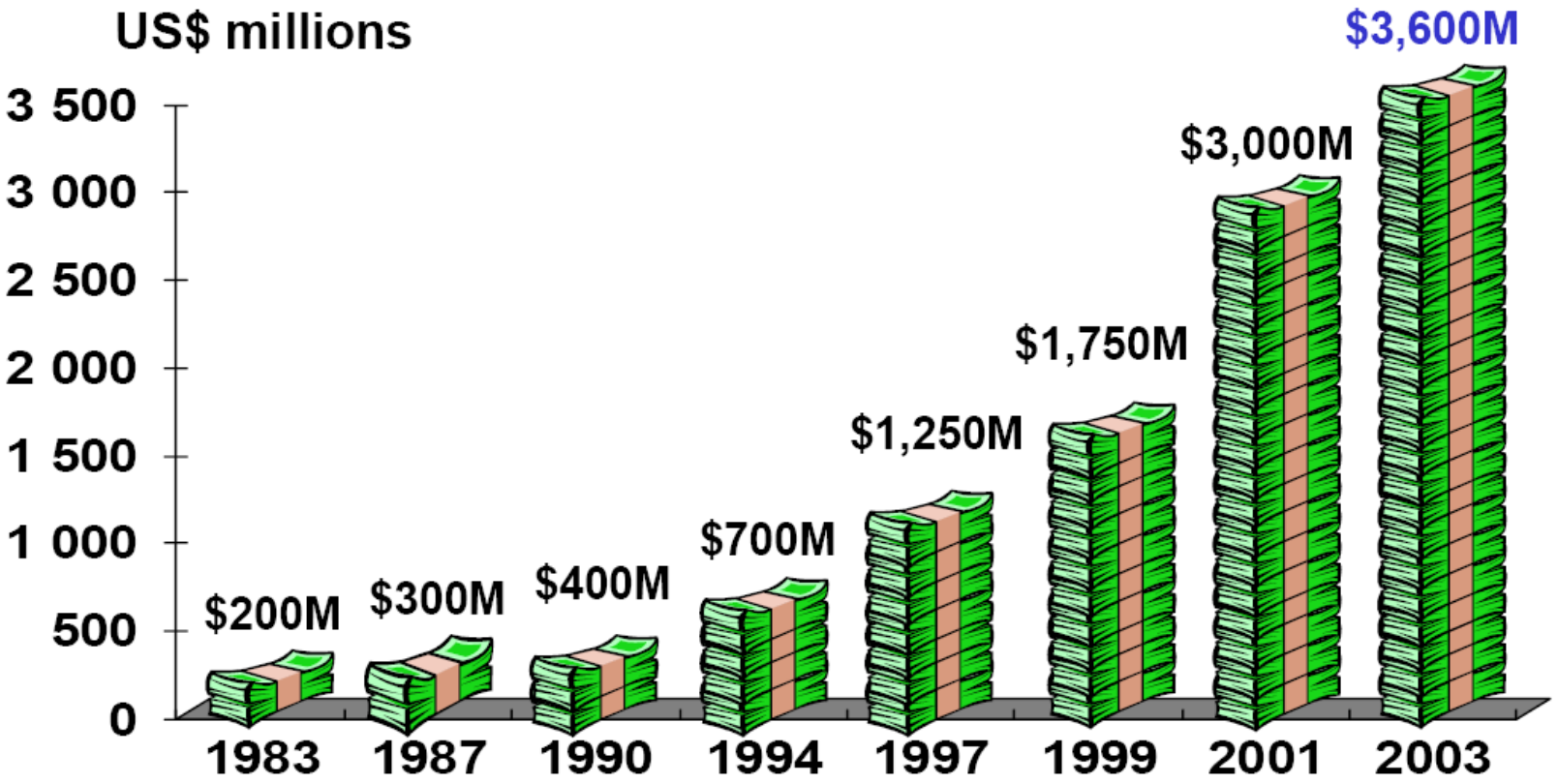
2014 — Broadwell-Y 14nm

NEW

VLSI Feature Size



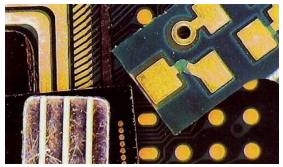
Rising Fab Costs



wafer	4"/5"	5"/6"	6"	6"/8"	8"	8"	12"	12"
process	1.2-um	1.0-um	0.8-um	0.5-um	0.35-um	0.25-um	0.13-um	0.09-um

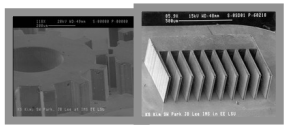
Source: Dataquest, UMC

Miniaturization

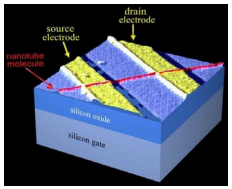


PCB

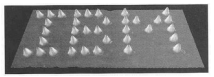
Diced chip



MEMS devices



Nanotube FET



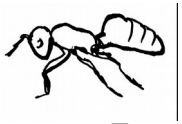
Nano manipulation

TR on IC

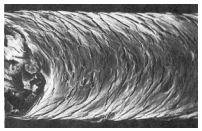
m cm mm µm nm Å

Human: ~ 2 m

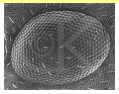
Grain of sand: ~ 1 mm



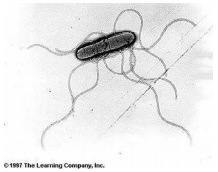
Ant: ~ 5mm



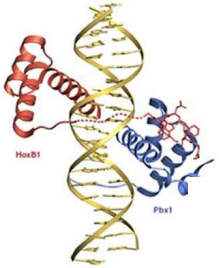
Hair: ~ 100 µm



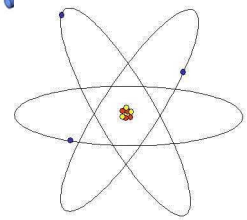
Ant eye segment: ~ 5 µm



Bacteria: ~ 0.1 µm

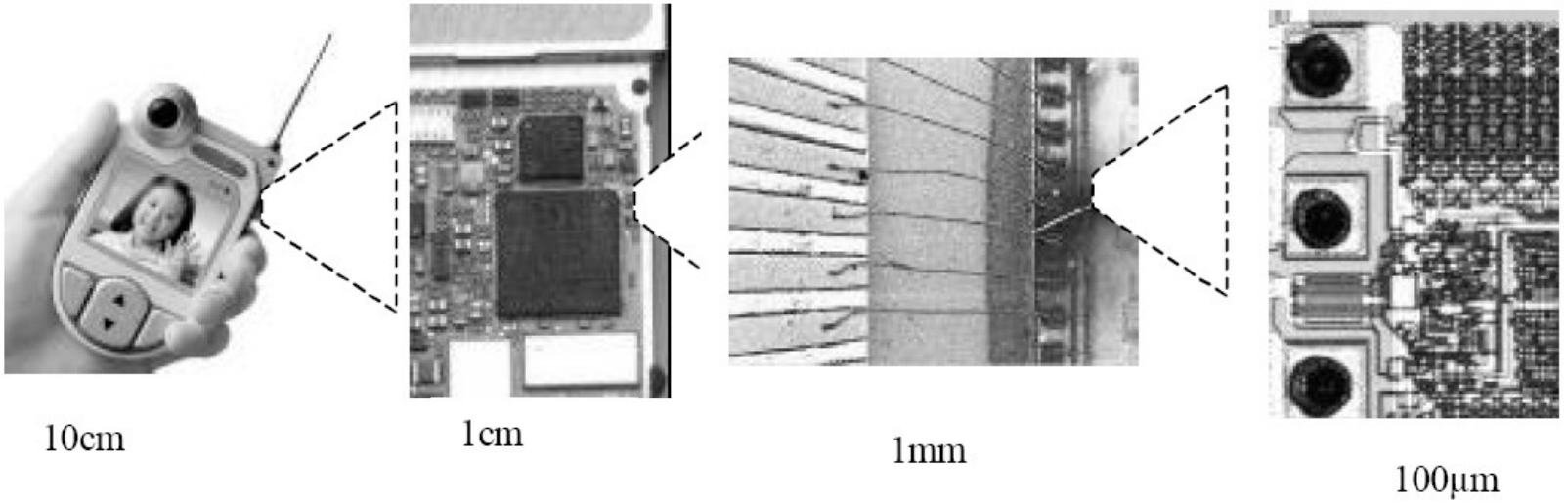


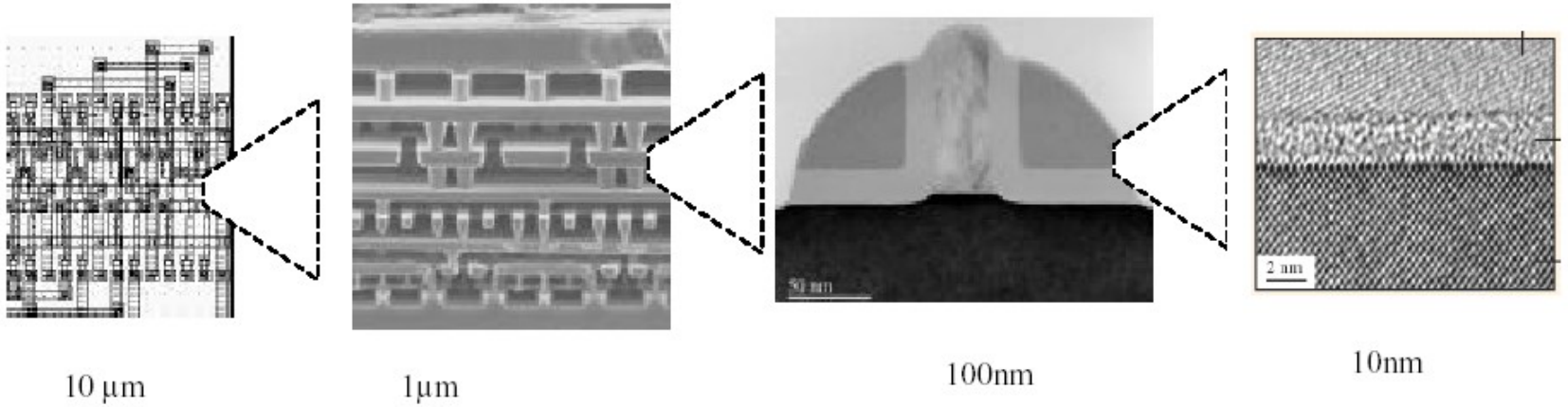
DNA: ~ nm



Atom: ~ Å

Miniaturization





Microelectronics Technology Parameters

- Basic parameters
  - Logic gate delay
  - Power dissipation
- Synthetic parameter
  - Power-delay product

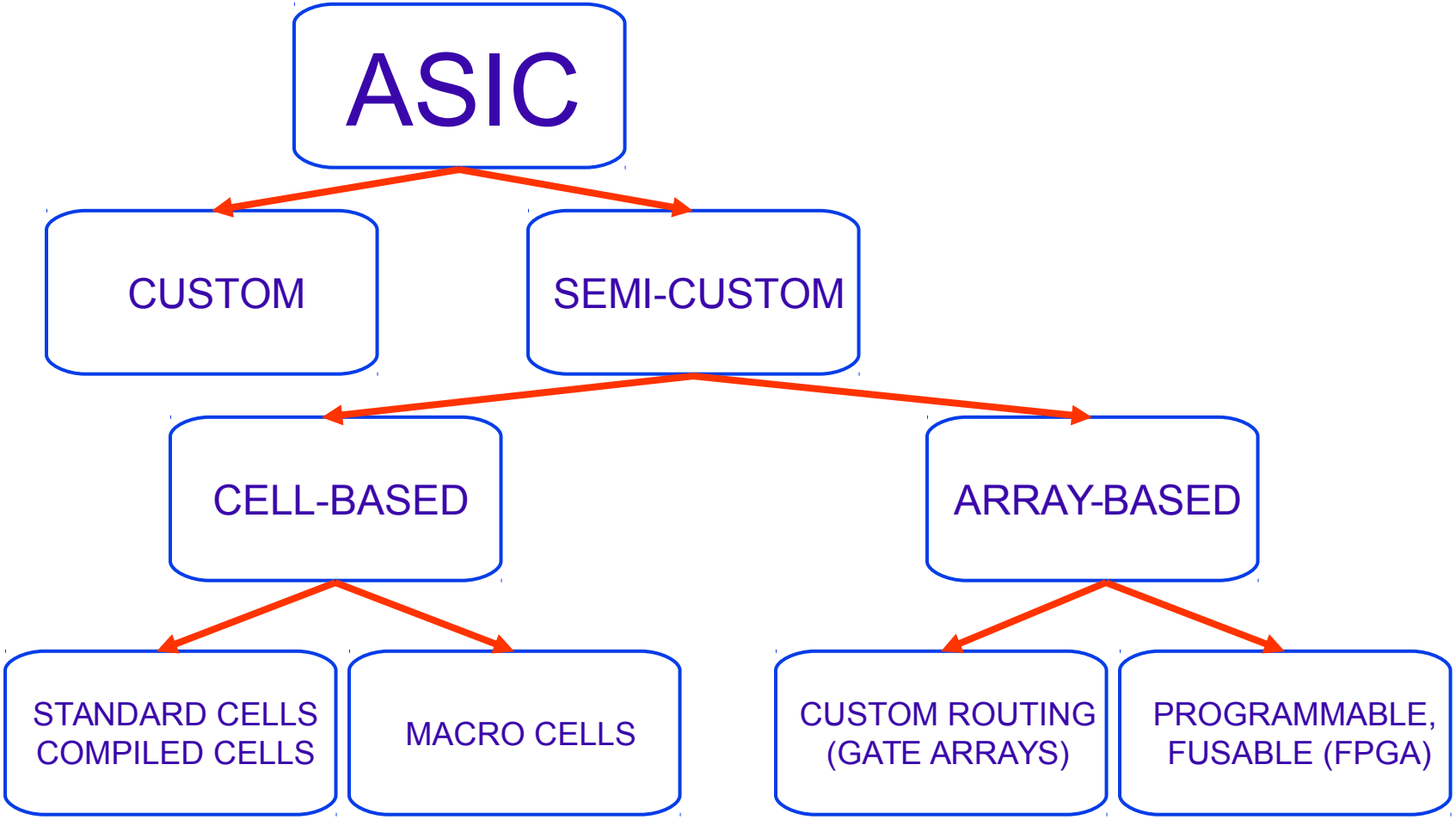
Monolithic Circuits

- Standard
- Application Specific Integrated Circuits (ASIC)
- Application Specific Standard Product (ASSP)

Standard ICs

- Advantages of Standard ICs
  - Low cost
  - “Off-the-shelf” availability
  - Known reliability
  - Many suppliers (usually)
- Disadvantages of Standard ICs
  - Not optimized for a specific system
  - Hard to create a unique product
  - High area consumption

The 80's – The ASIC Circuits

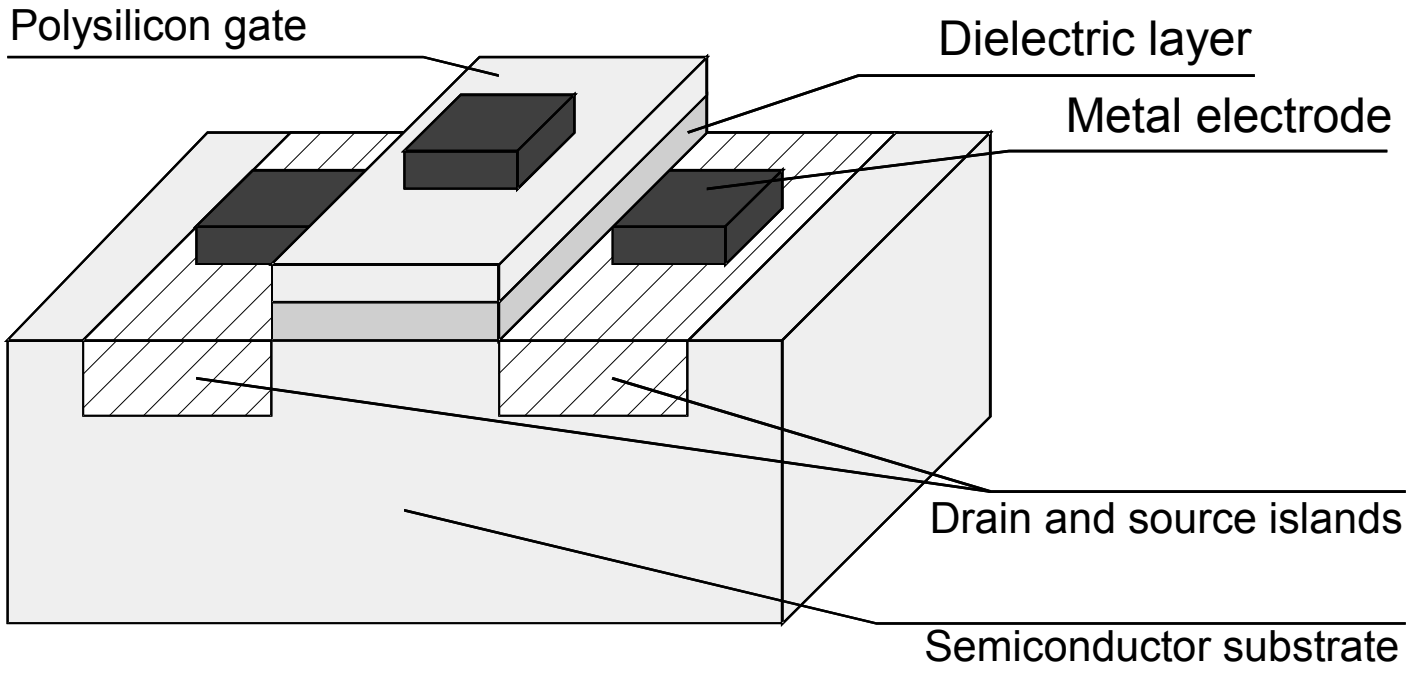


Classification of ASICs

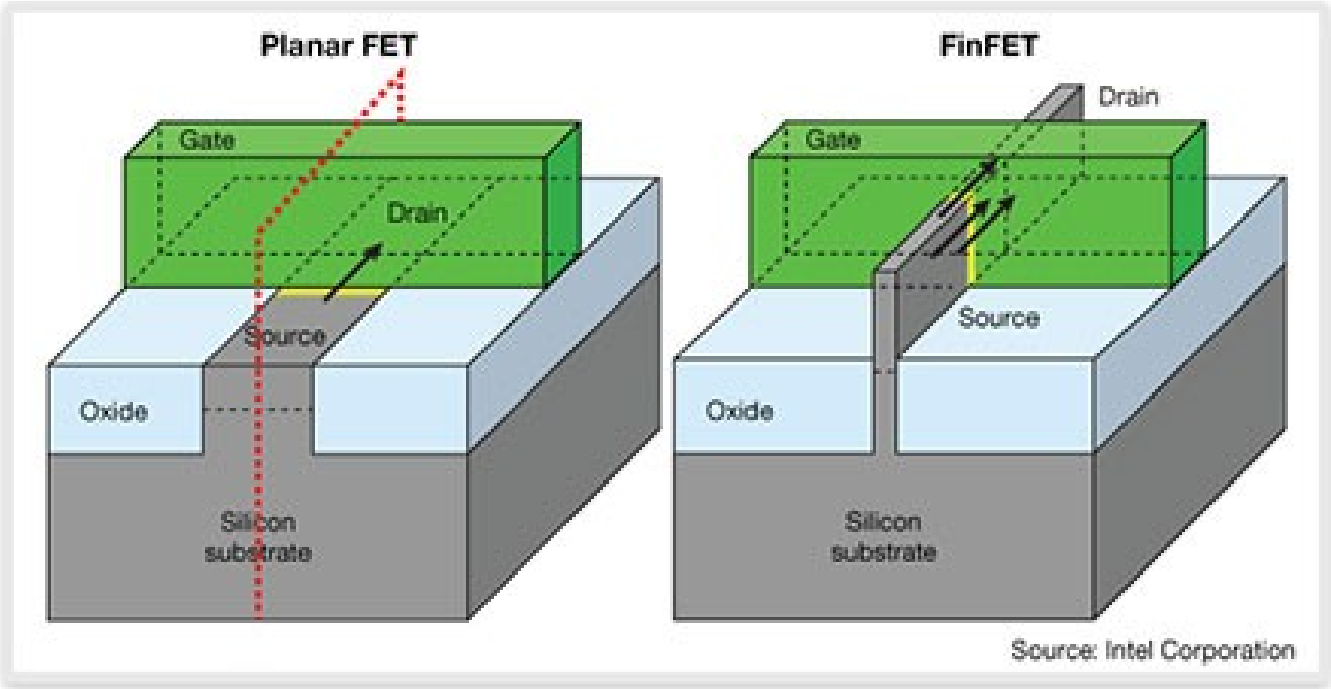
- Semicustom
  - Interconnection masks customized
- Custom
  - All masks customized
    - Standard Cell
    - Full Custom
- Programmable (Field Programmable Logic Devices)
    - Writable (Laser, Fuse, Antifuse, OTP EPROM)
    - Writable/erasable (EPROM, EEPROM, Flash memory, Ferroelectric)
  - Volatile (SRAM, FPGA)

“Field Engineer”

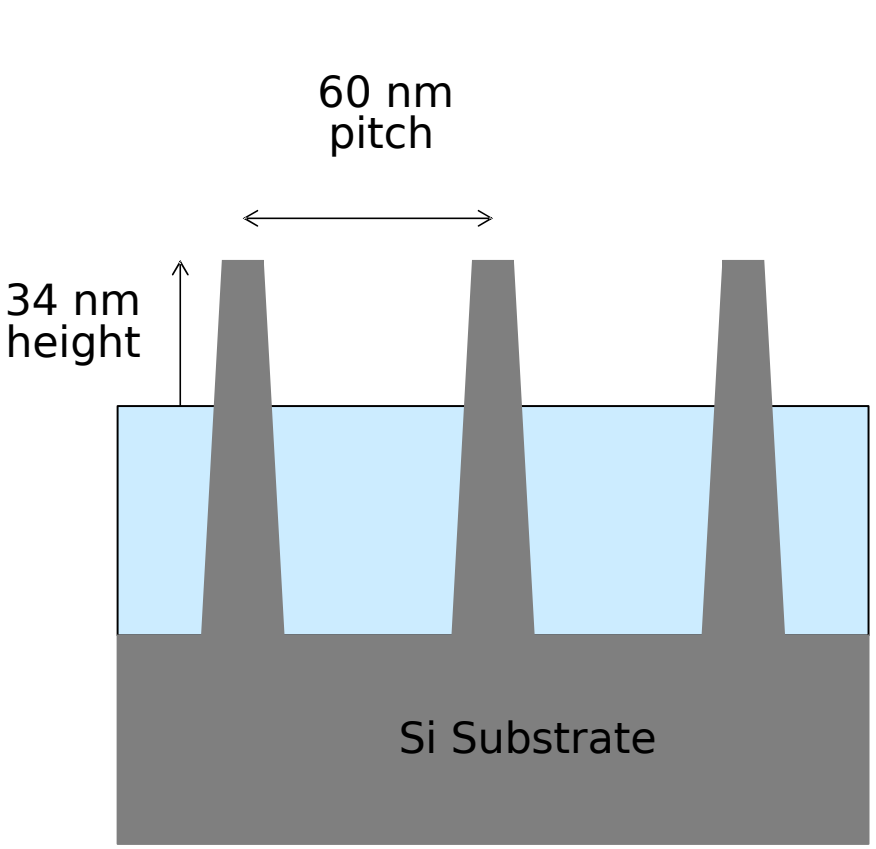
The MOS transistor



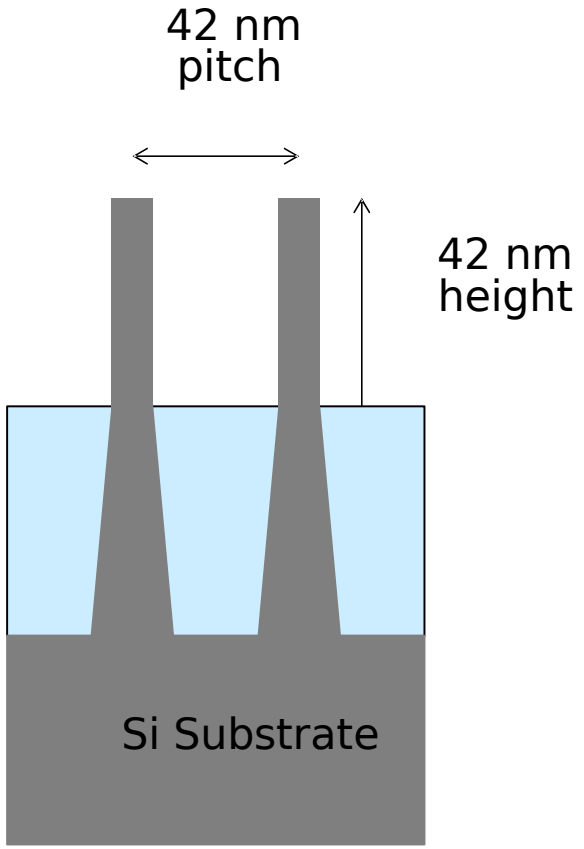
Planar FET and FinFet



Transistor Fin Improvement

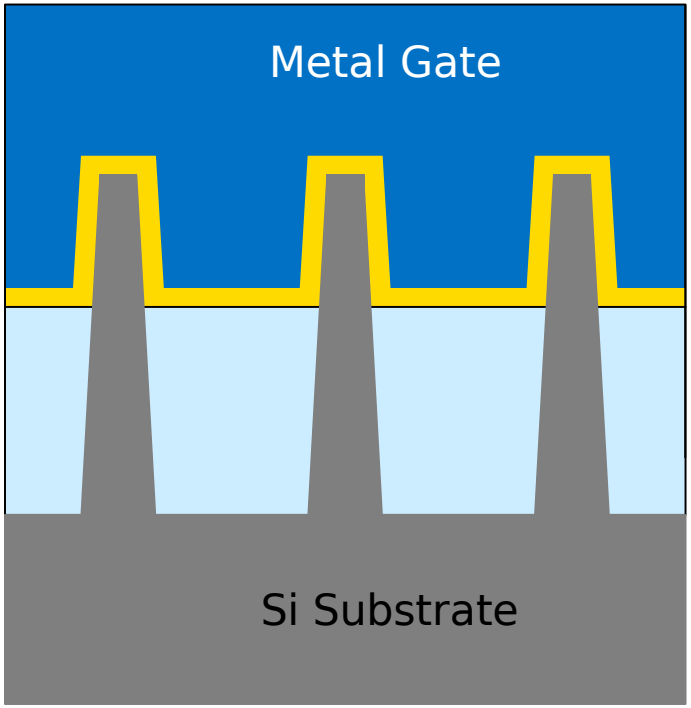


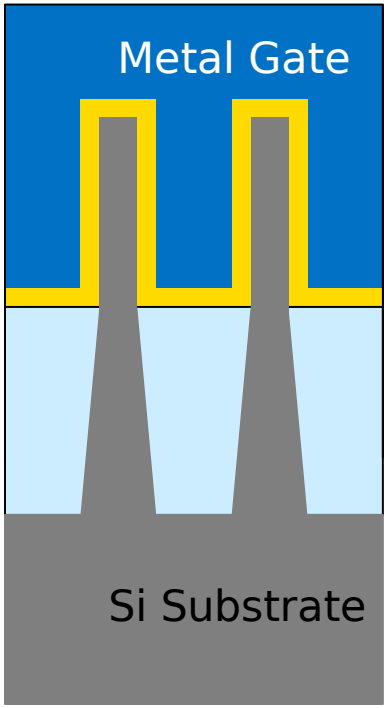
22 nm Process



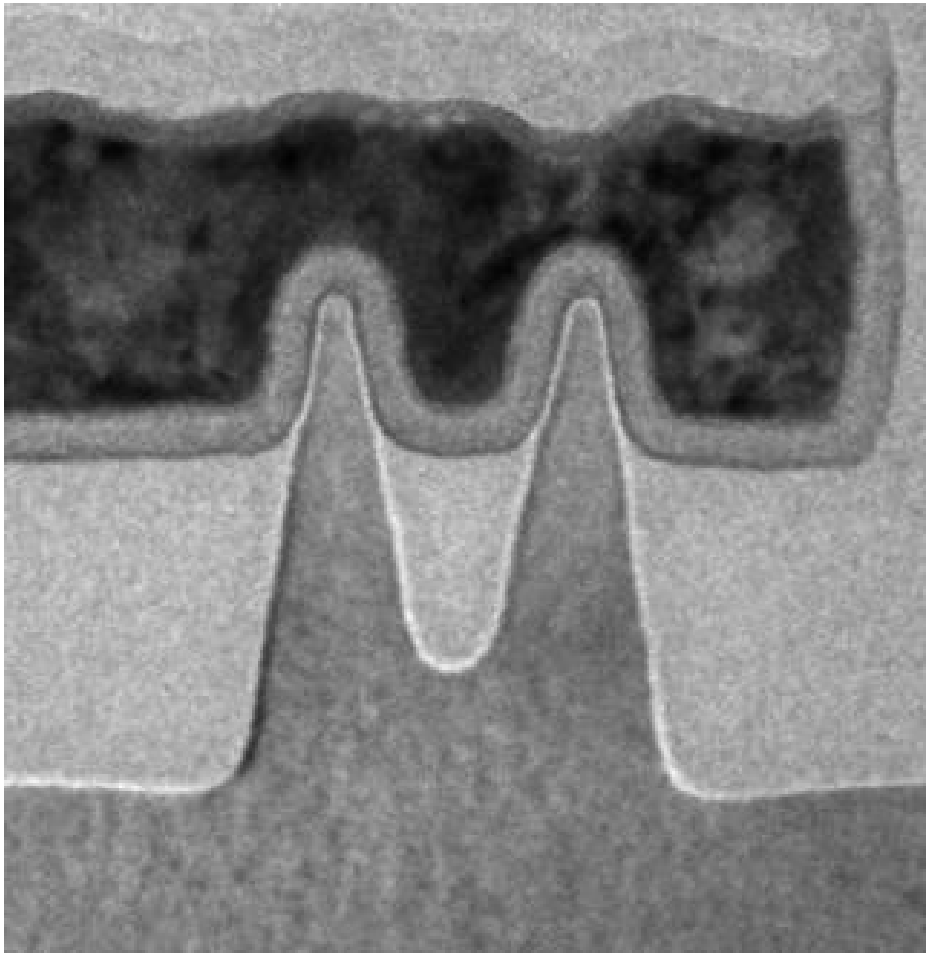
14 nm Process

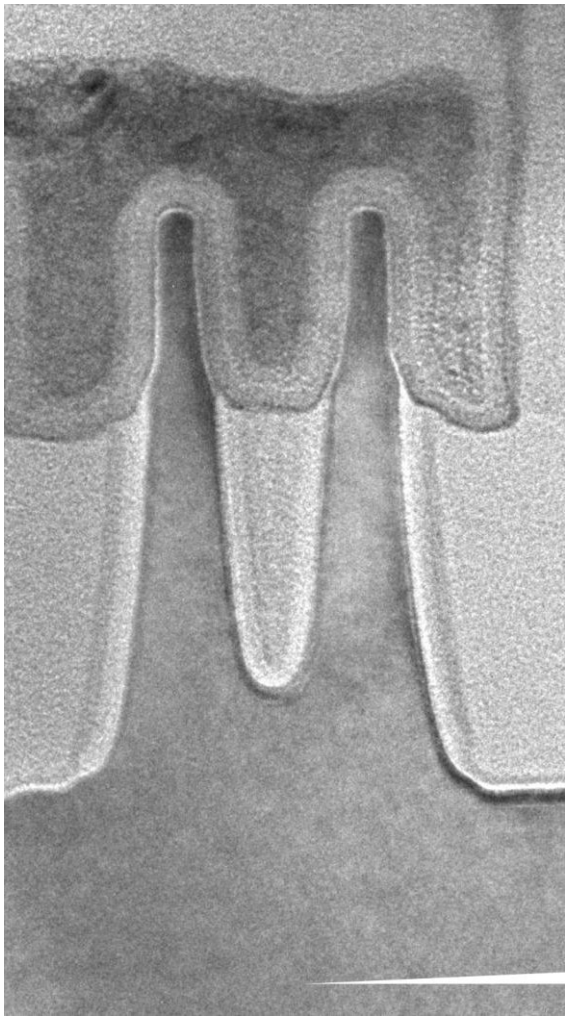
Transistor Fin Improvement





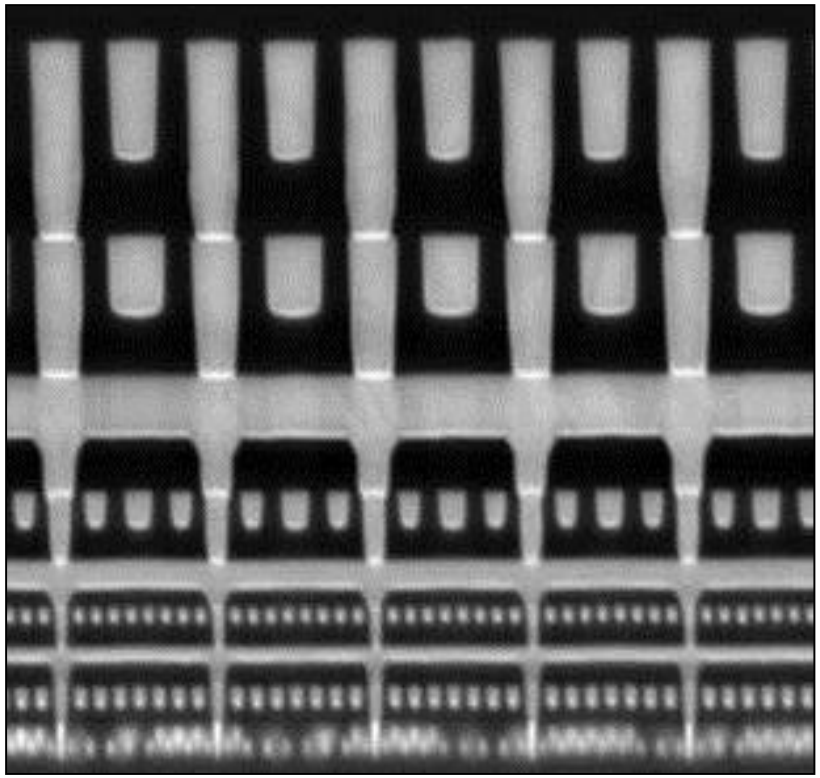
Transistor Fin Improvement





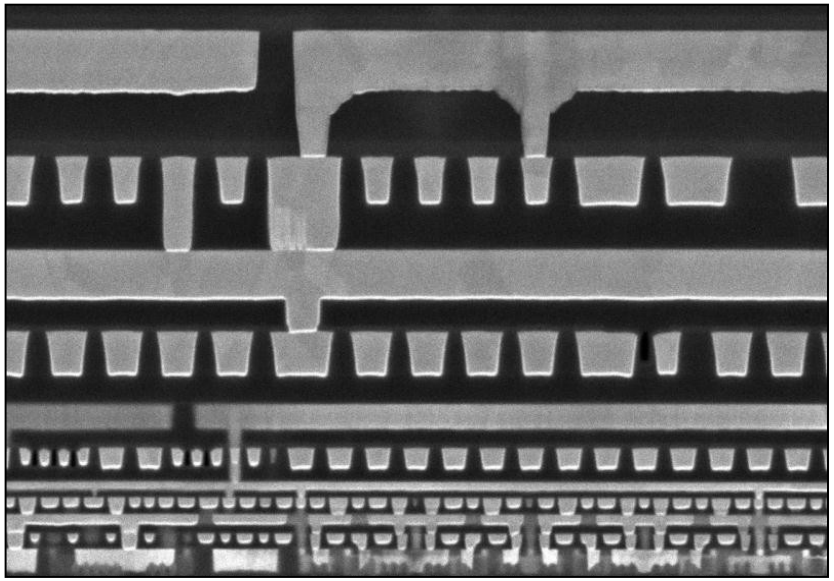
Interconnects

22 nm Process



80 nm minimum pitch

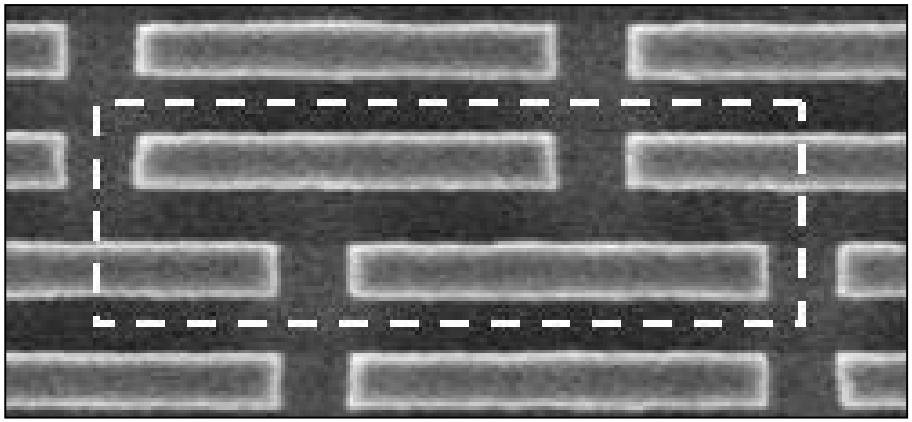
14 nm Process



52 nm minimum pitch

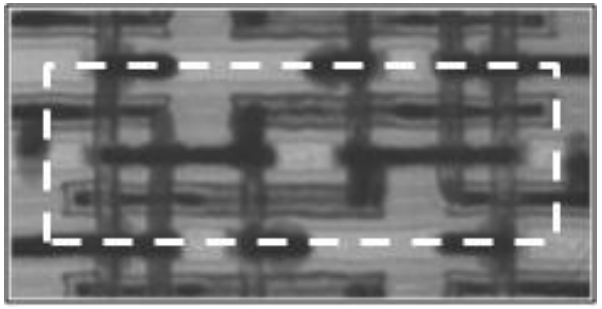
SRAM Memory Cells

22 nm Process



.108 um^2

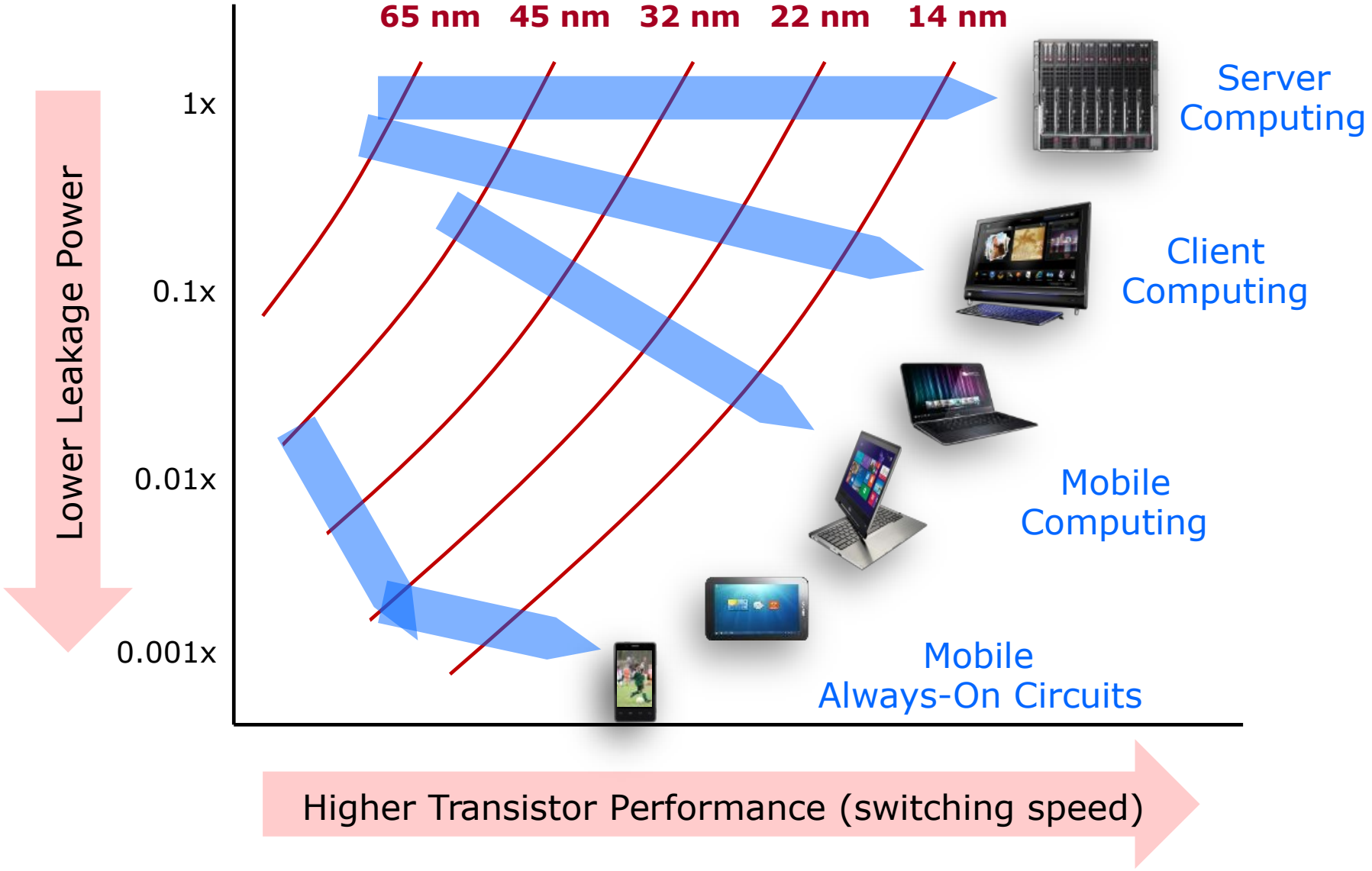
14 nm Process



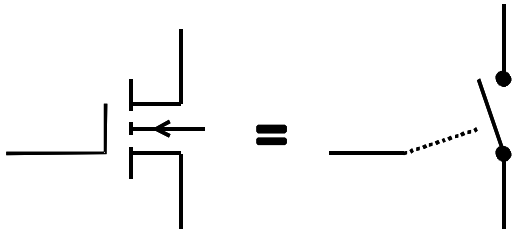
.0588 um^2

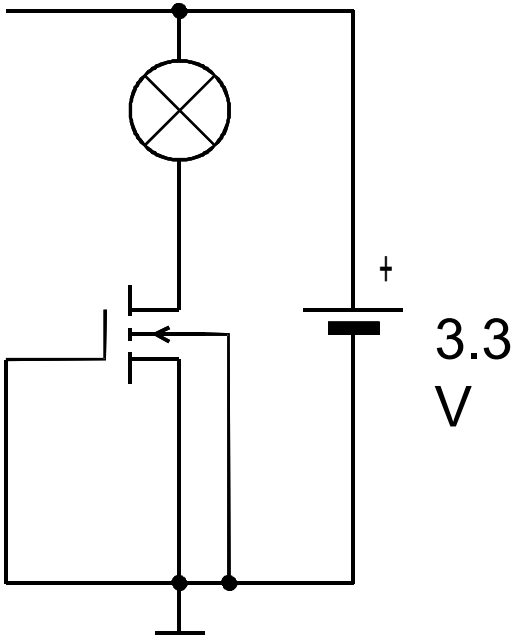
(Used on CPU products)

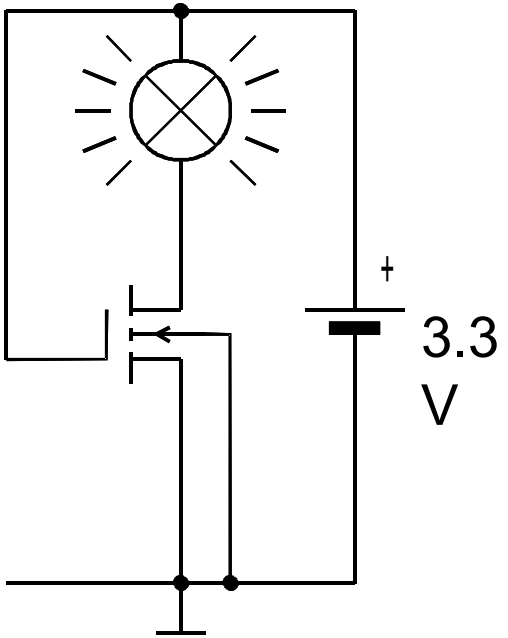
Transistor Performance vs. Leakage



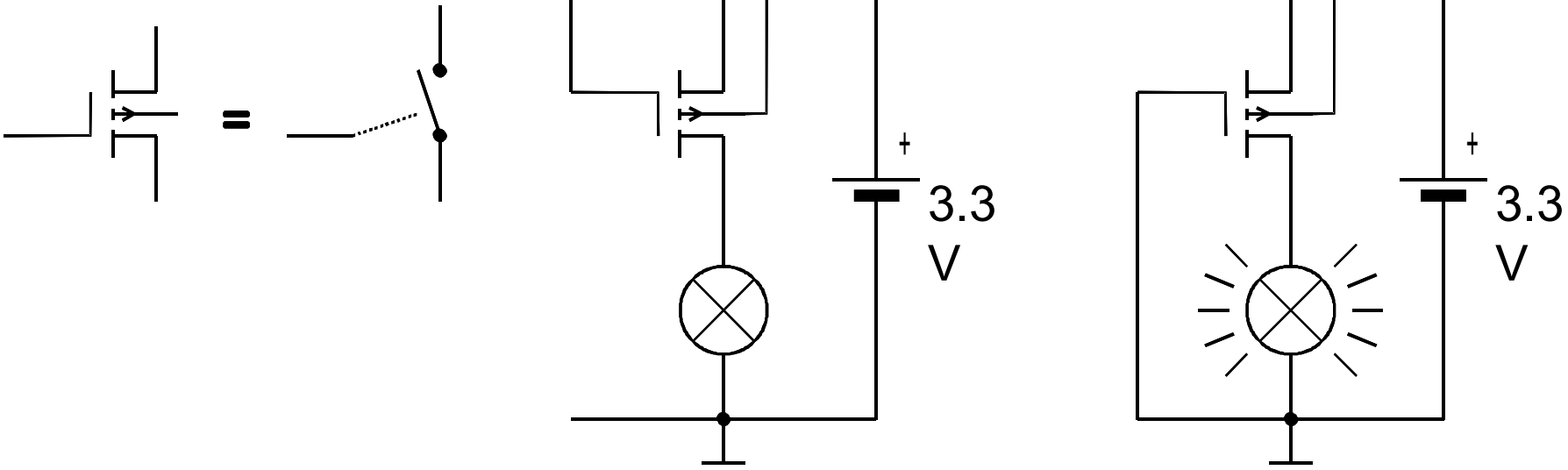
NMOS as a switch



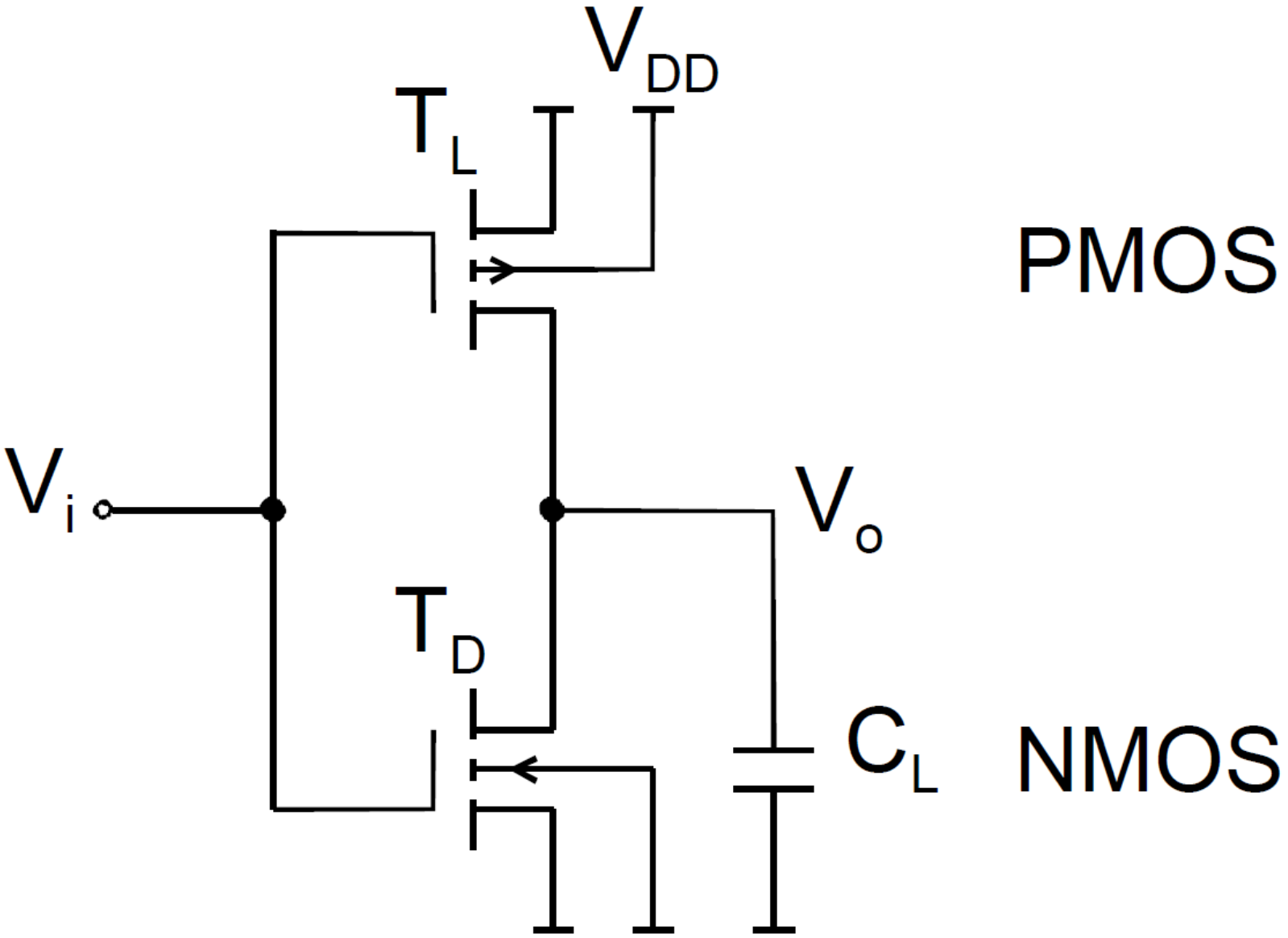




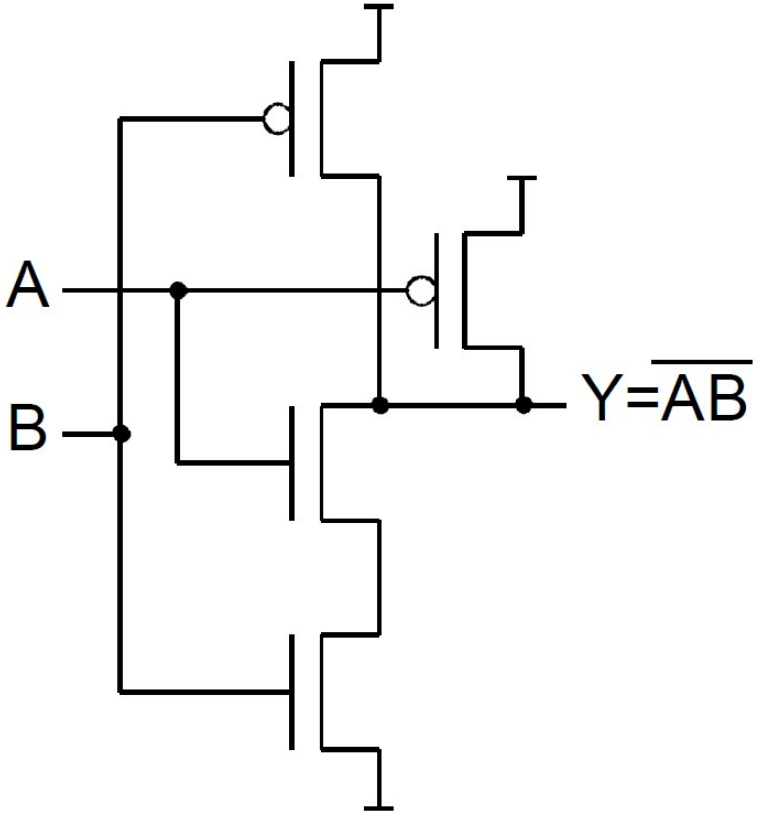
PMOS as a switch

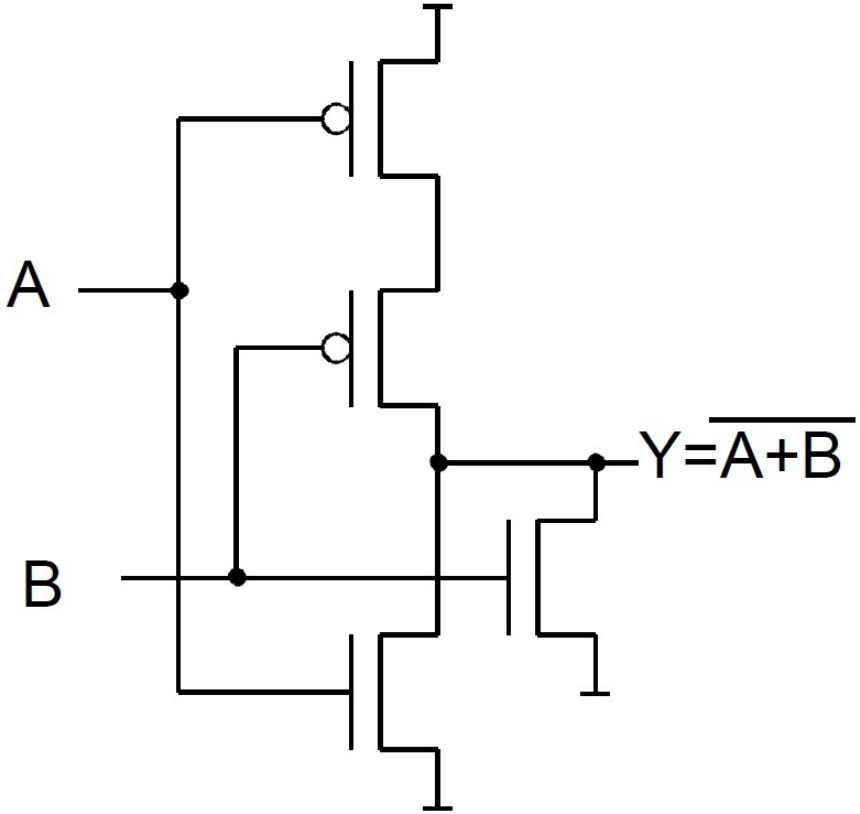


CMOS inverter

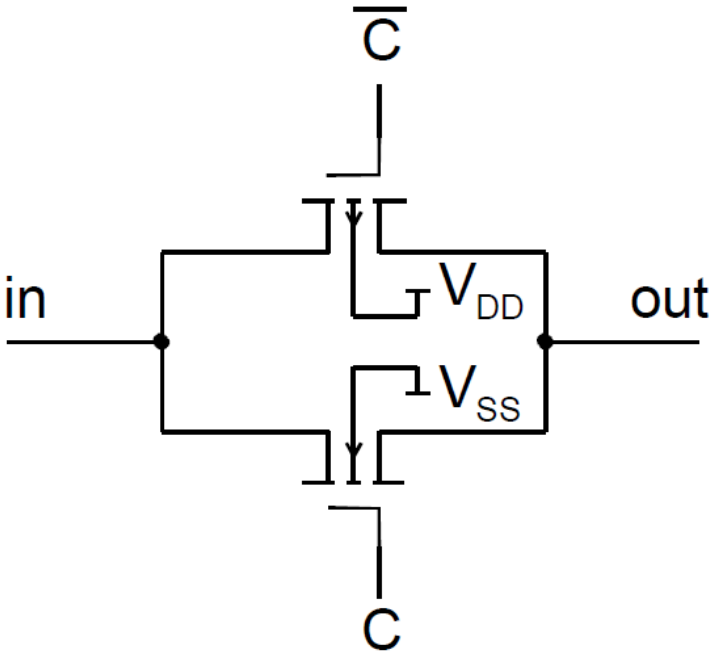


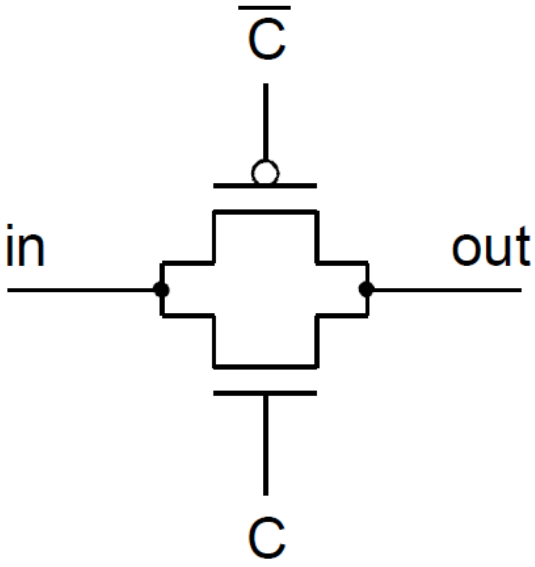
CMOS gates: NAND and NOR

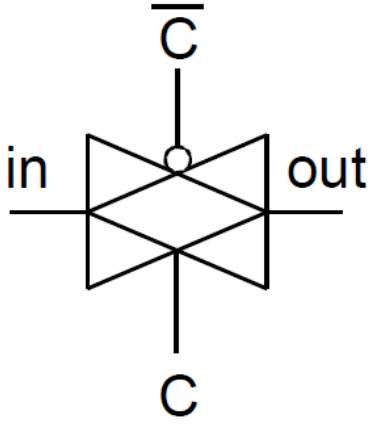




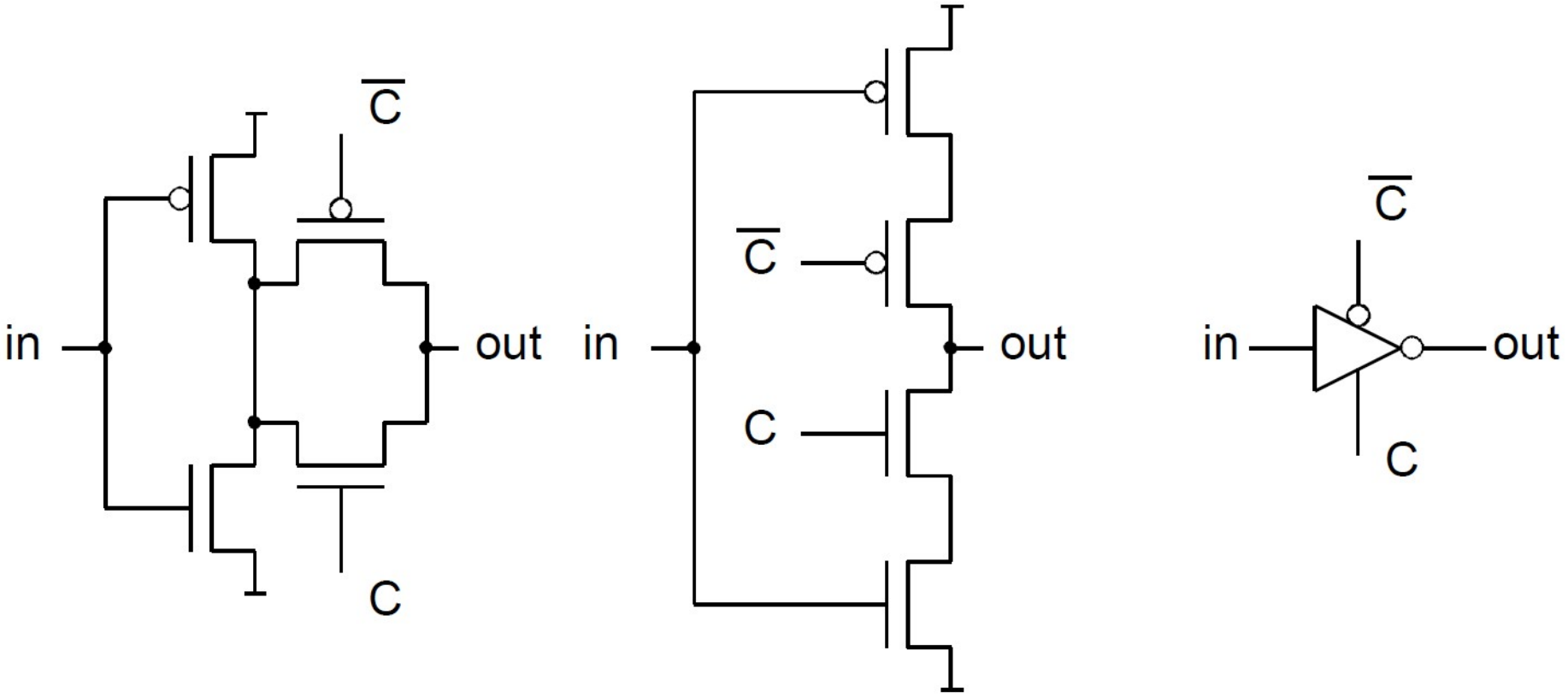
CMOS transmission gate





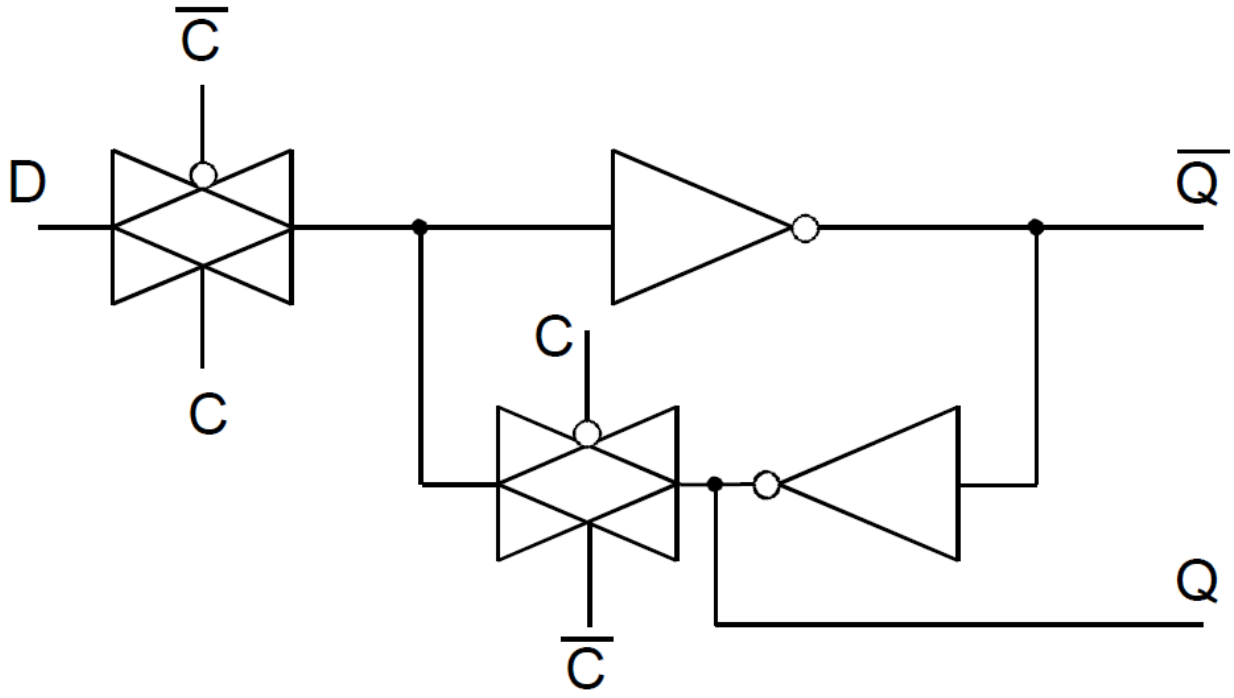


Three-state inverter

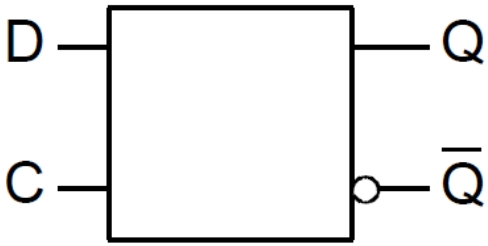


Latch

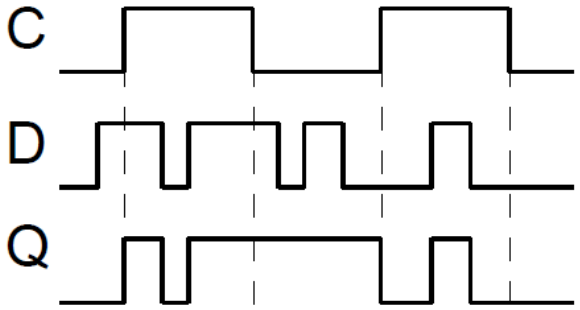
a)



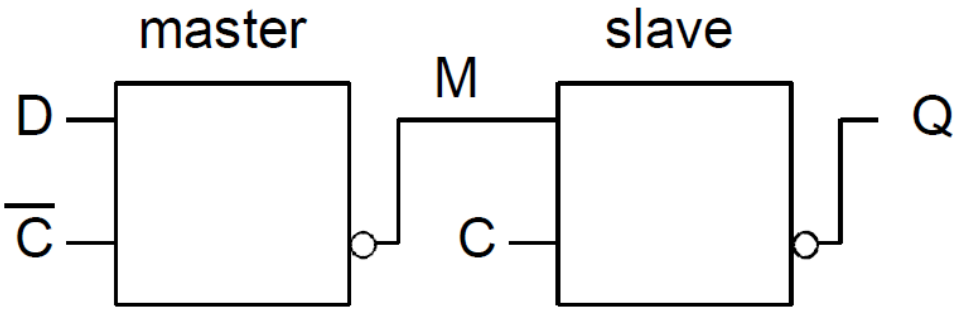
b)

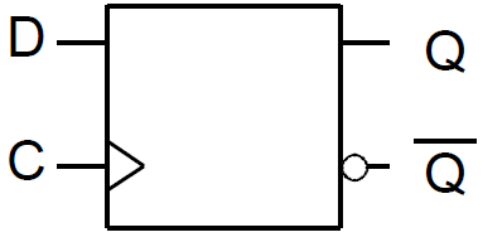


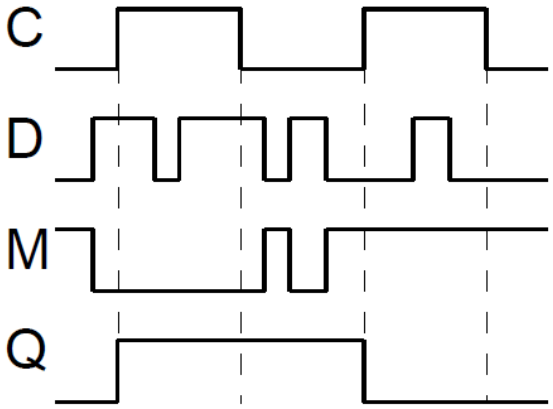
c)



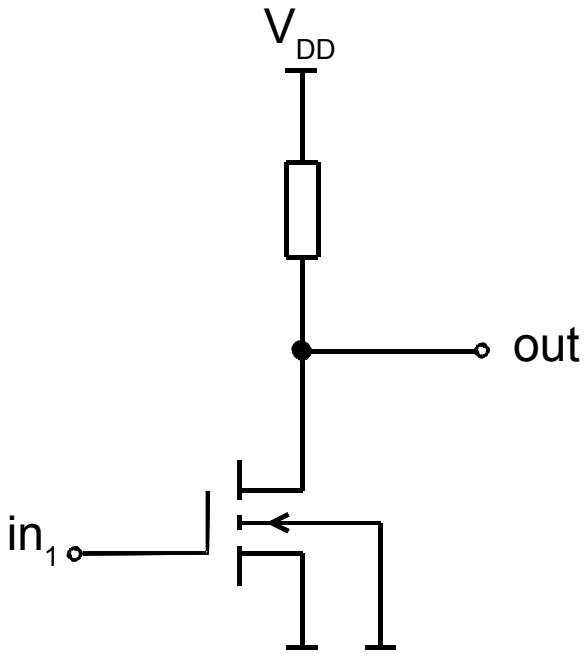
Flip-flop

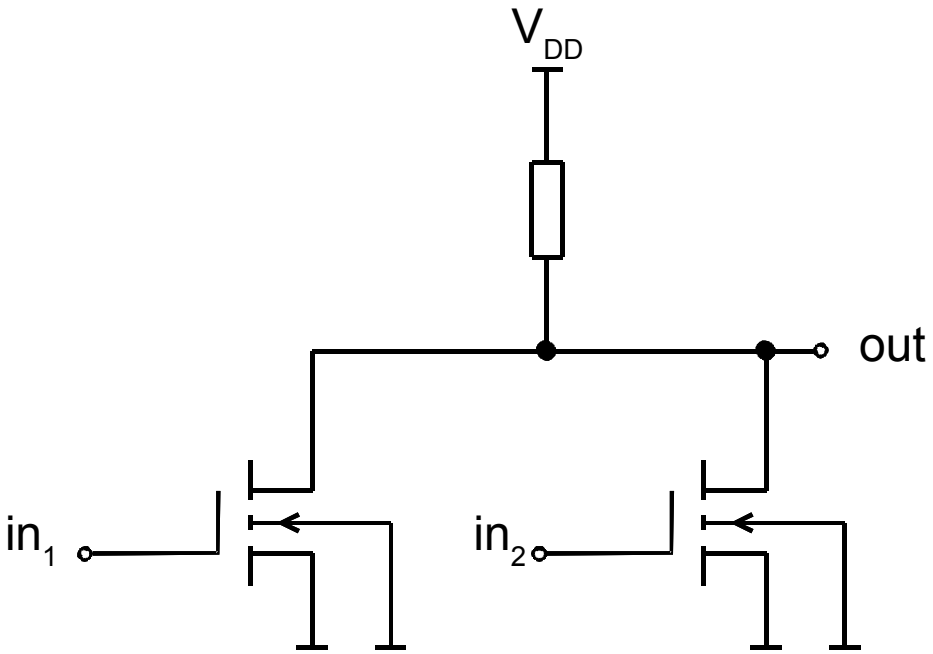




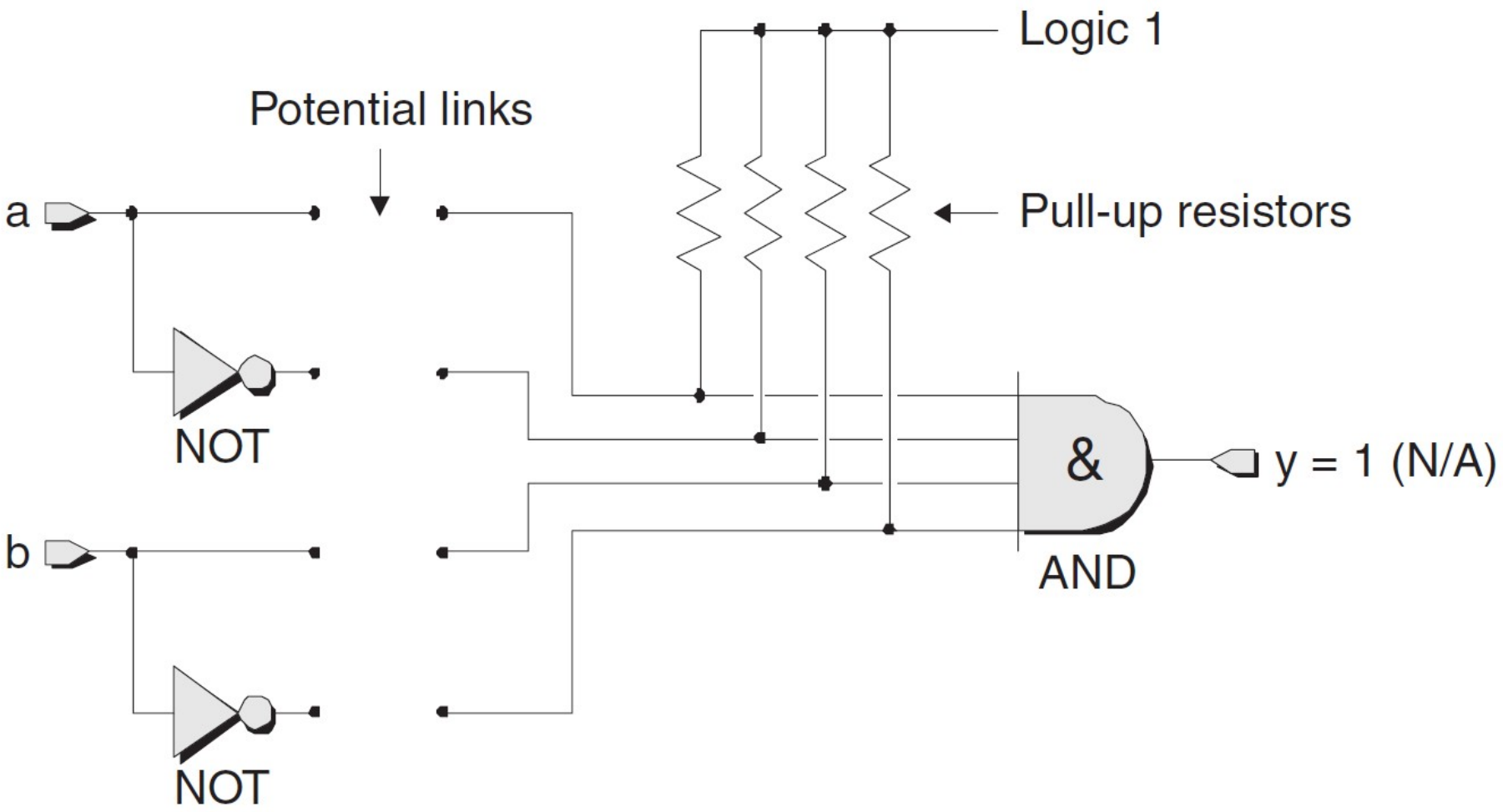


Wired NOR



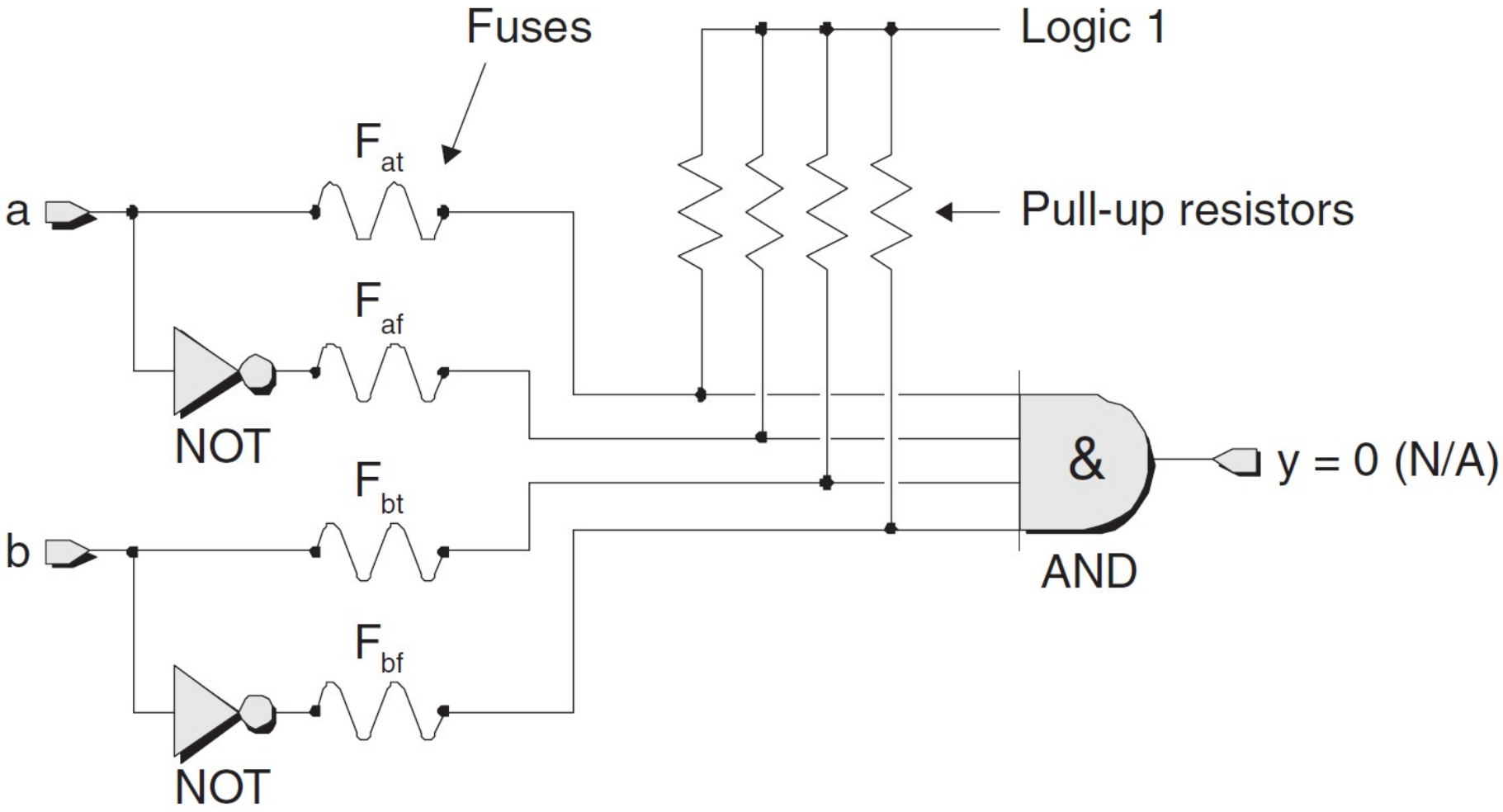


Programmable circuit



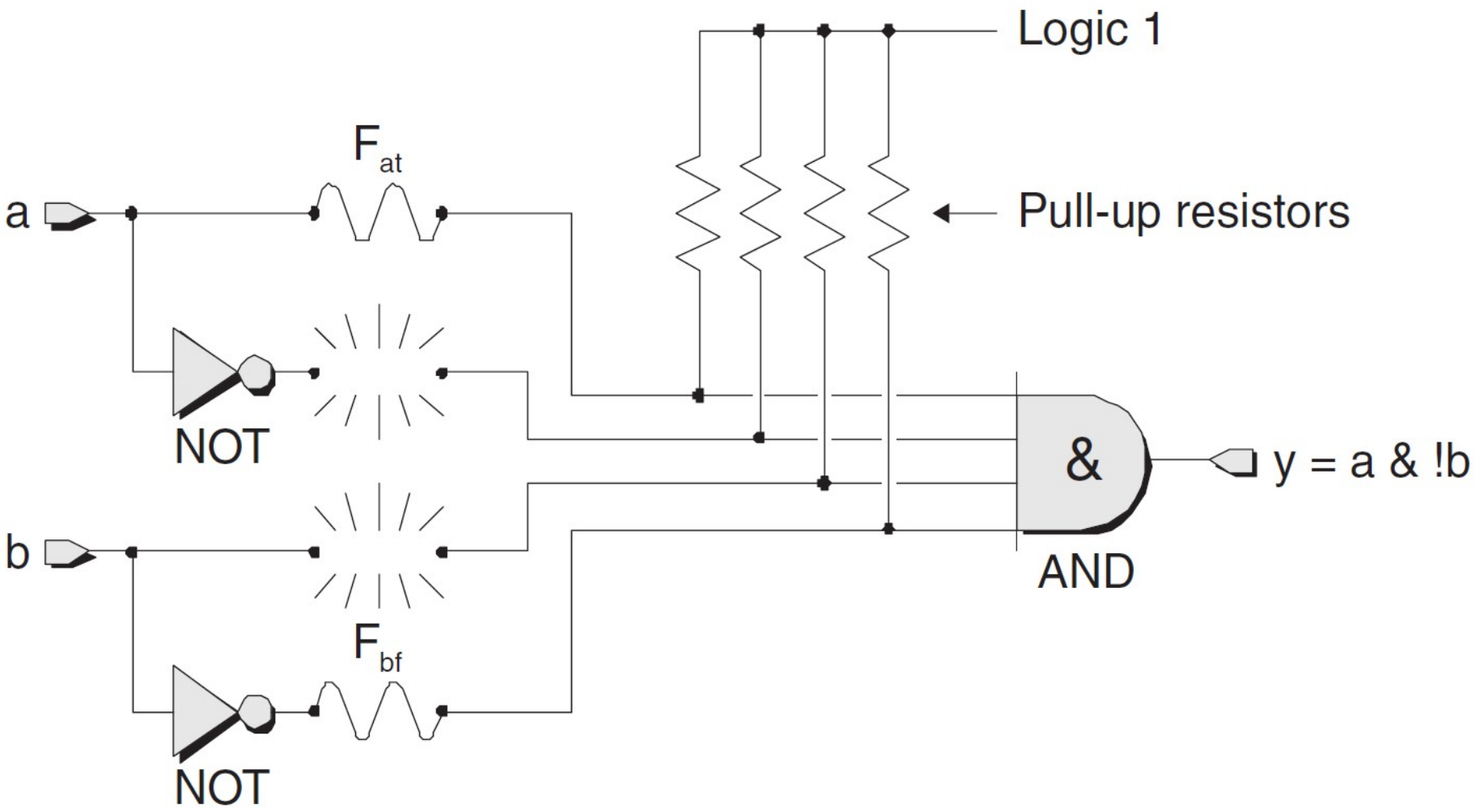
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Fuses technology



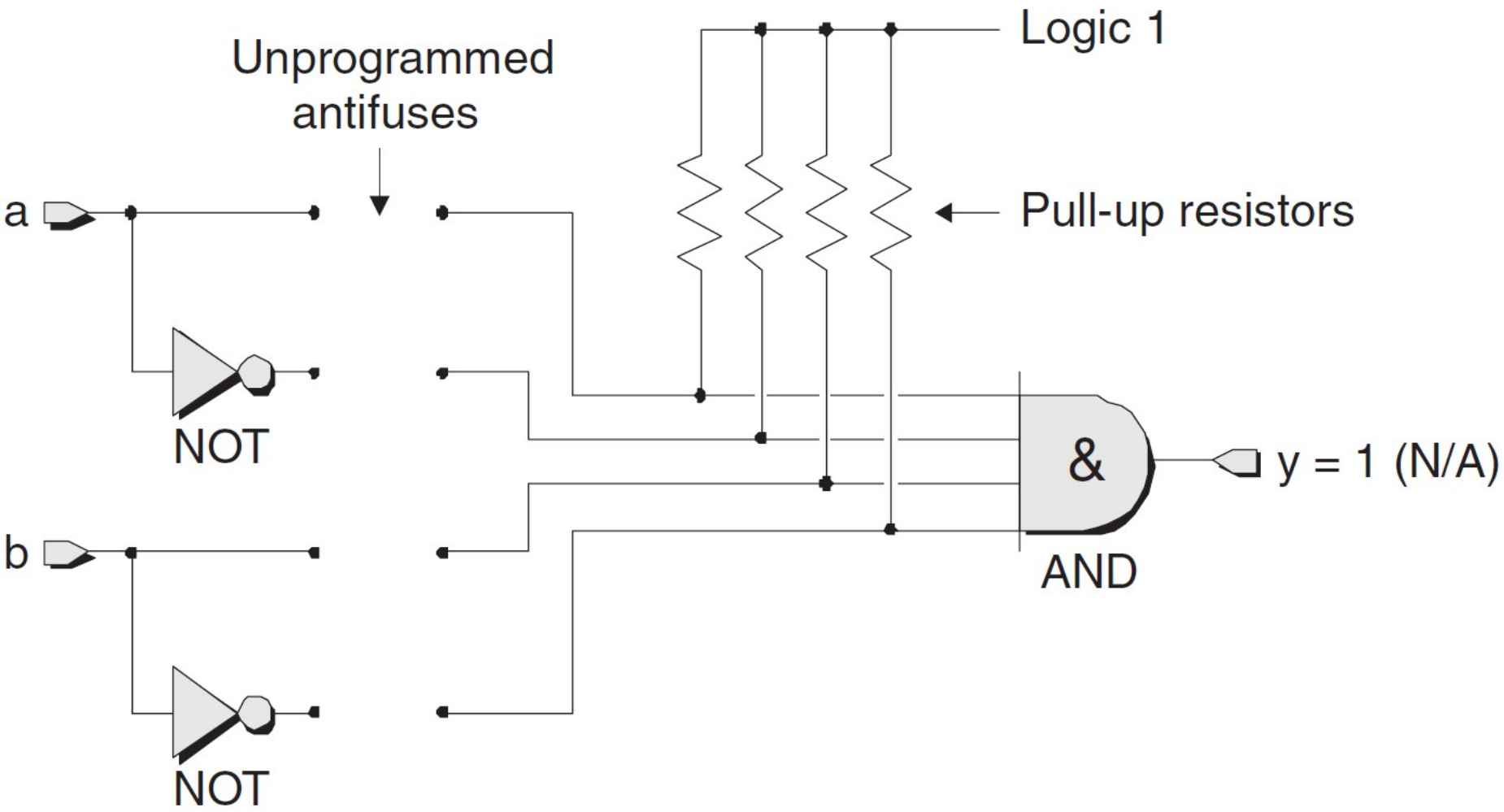
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Programmed circuit example



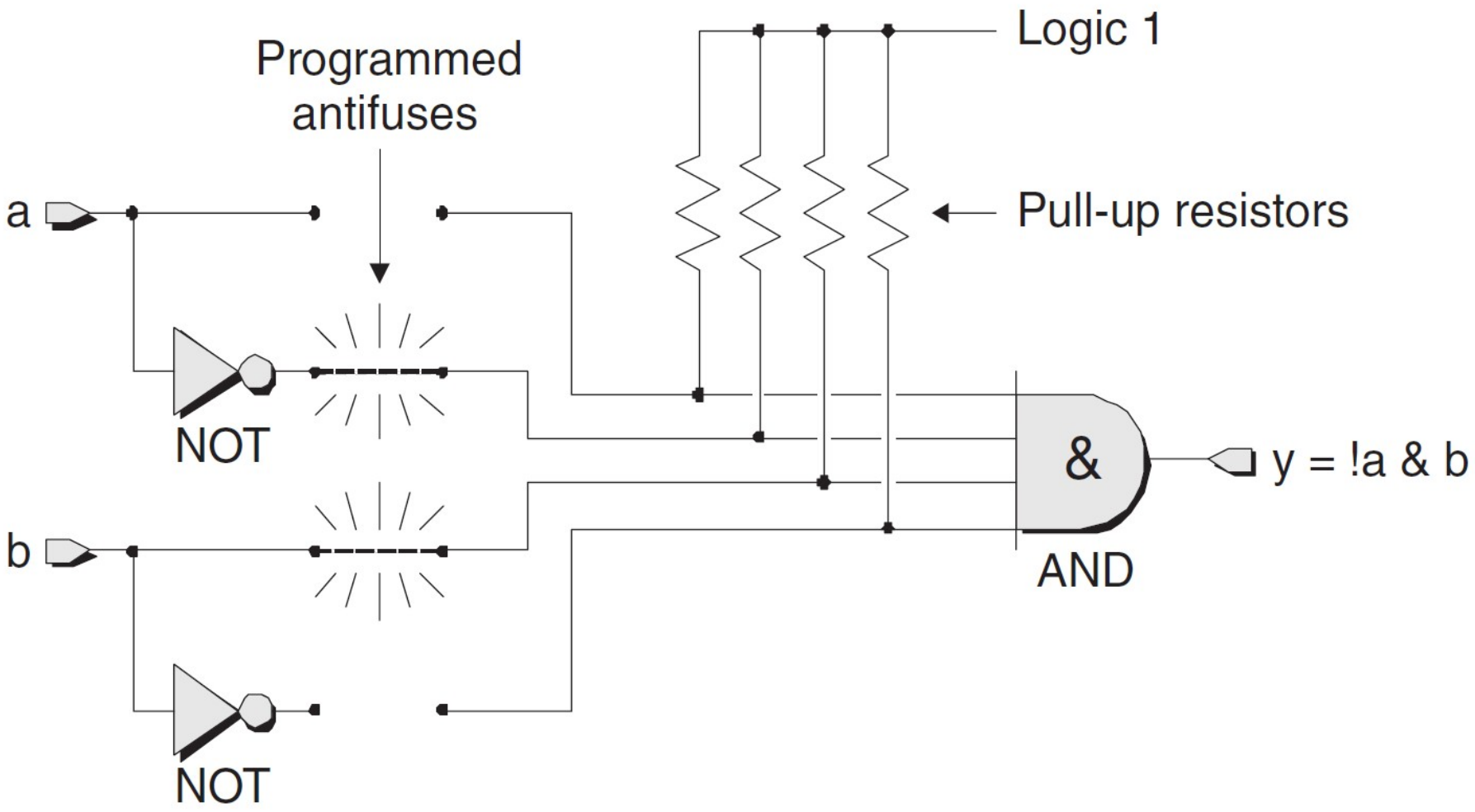
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Antifuse technology



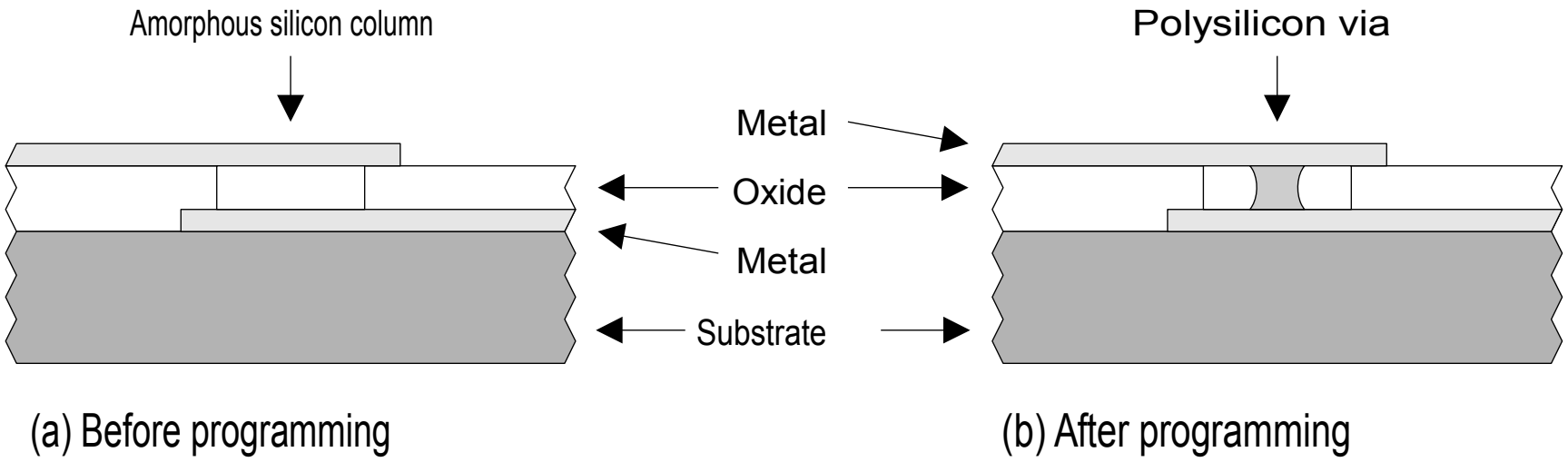
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Programmed circuit example



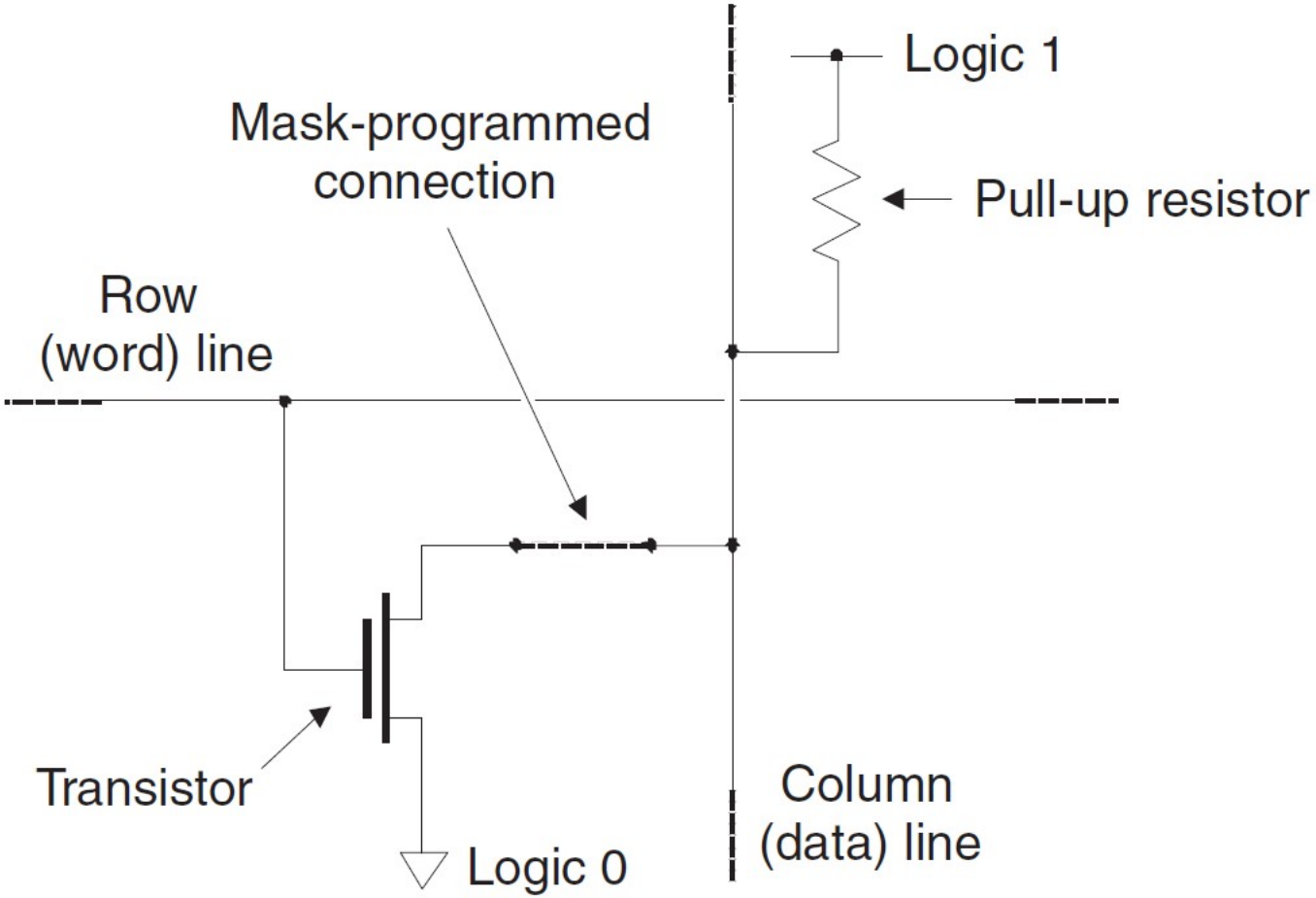
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Antifuse technology



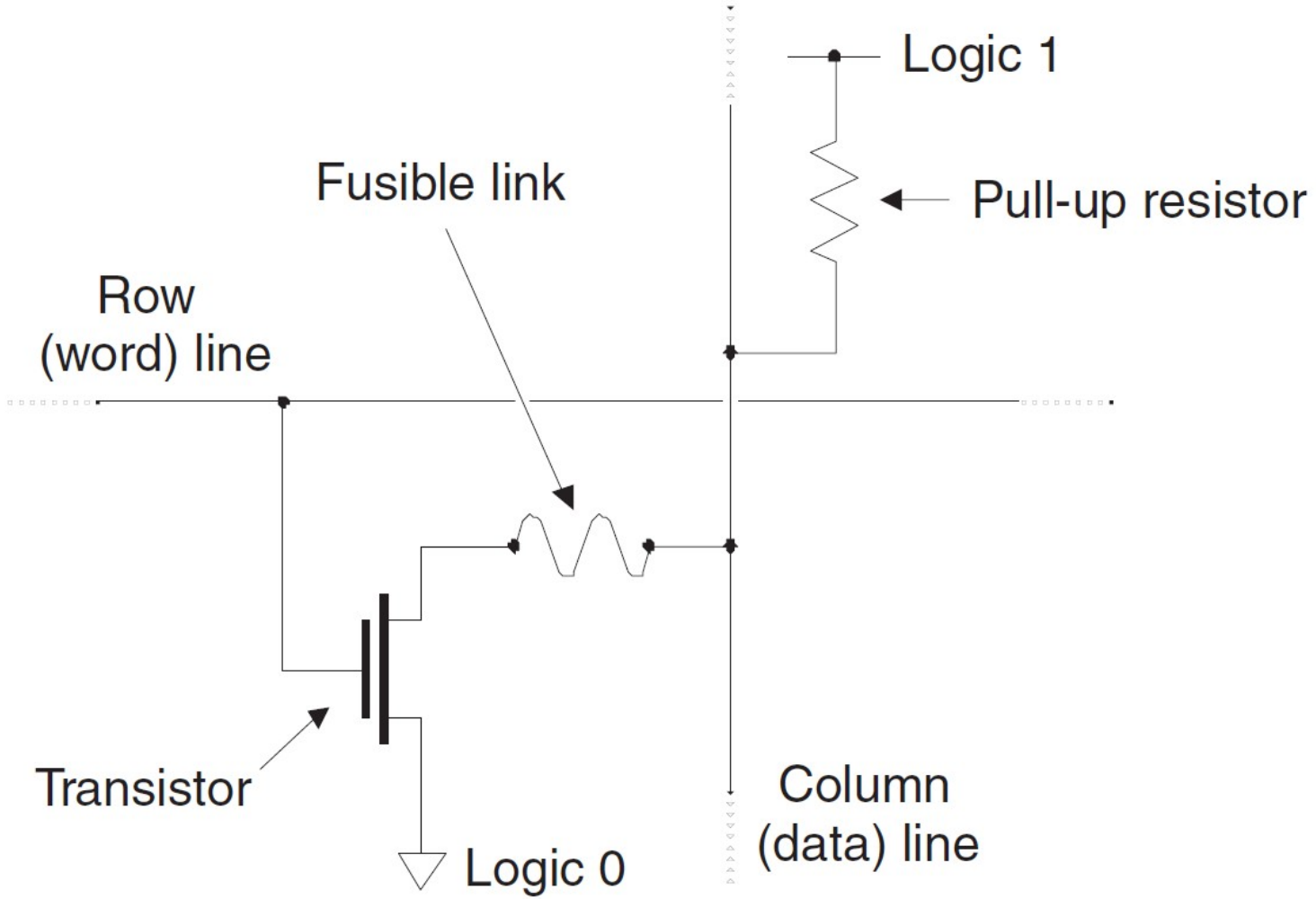
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Mask programming



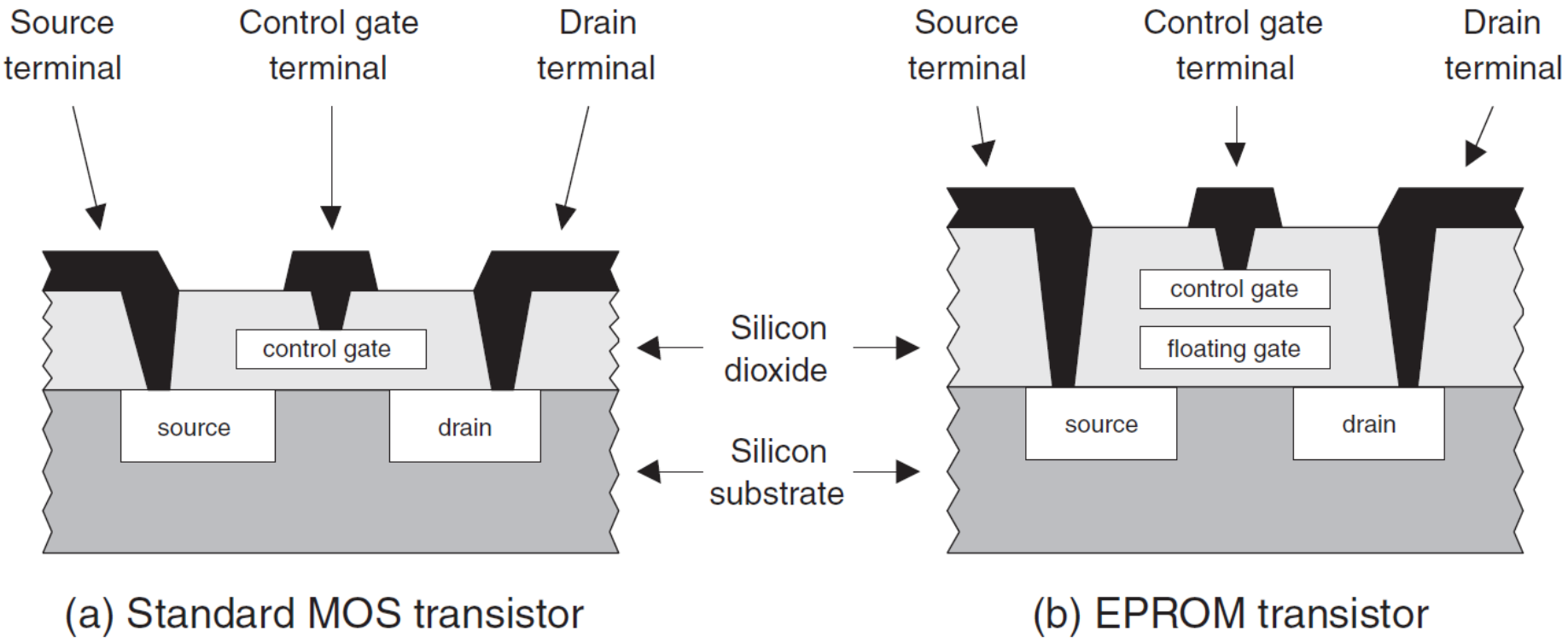
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

PROM (Programmable ROM)



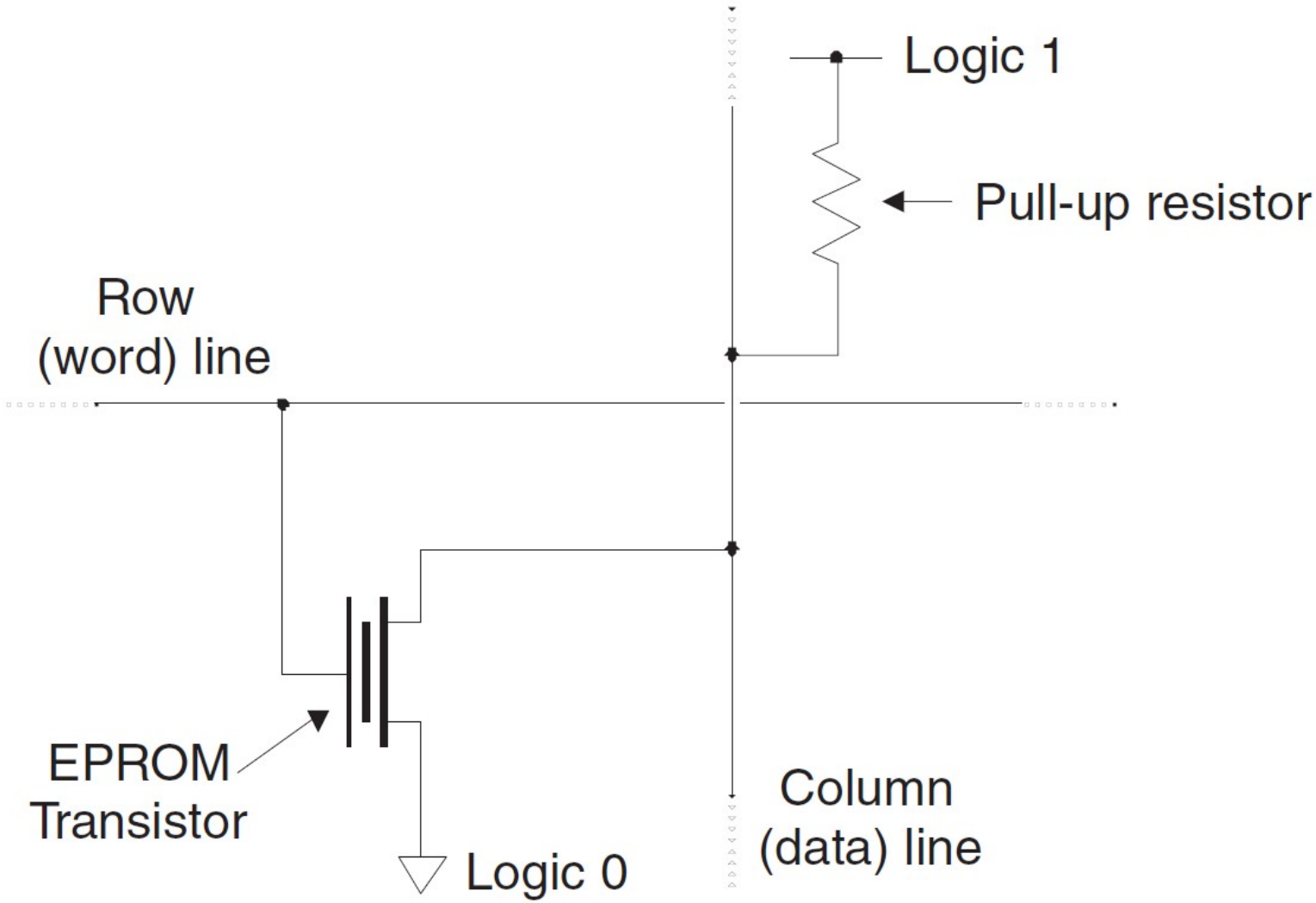
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

EPROM (Eraseable Programmable ROM)



Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

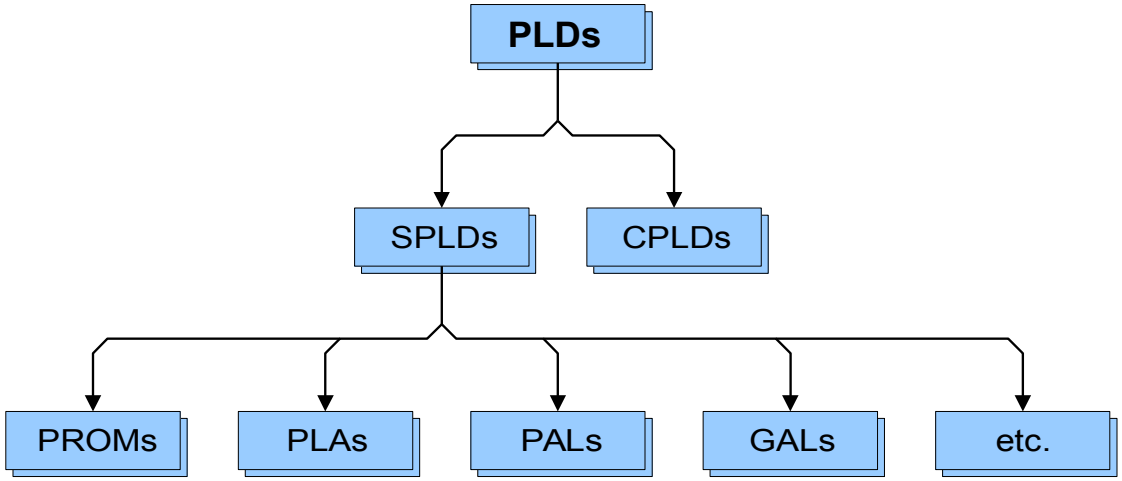
EPROM-based circuits



Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

PLD (Programmable Logic Devices)

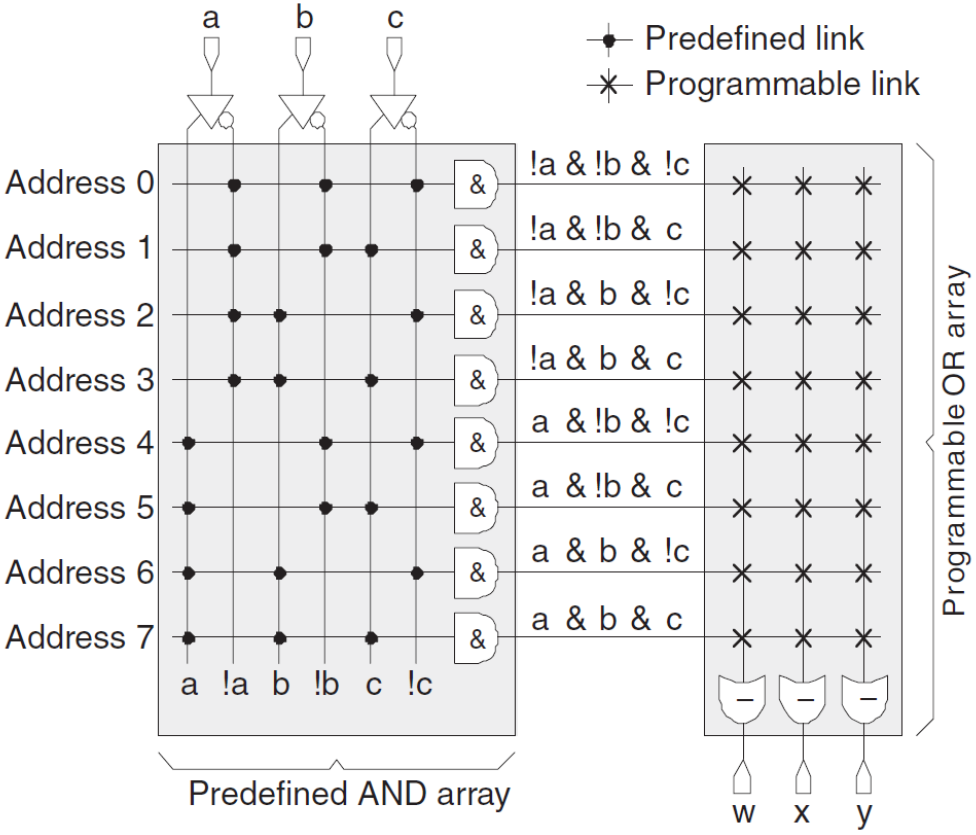
- First programmable logic devices were called PLD
- PLDs can be divided into two groups:
  - SPLDs : Simple PLDs
  - CPLDs: Complex PLDs
- The first programmable circuit (PROM) manufactured in 70-s
- CPLD – late 70-s and early 80-s



Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

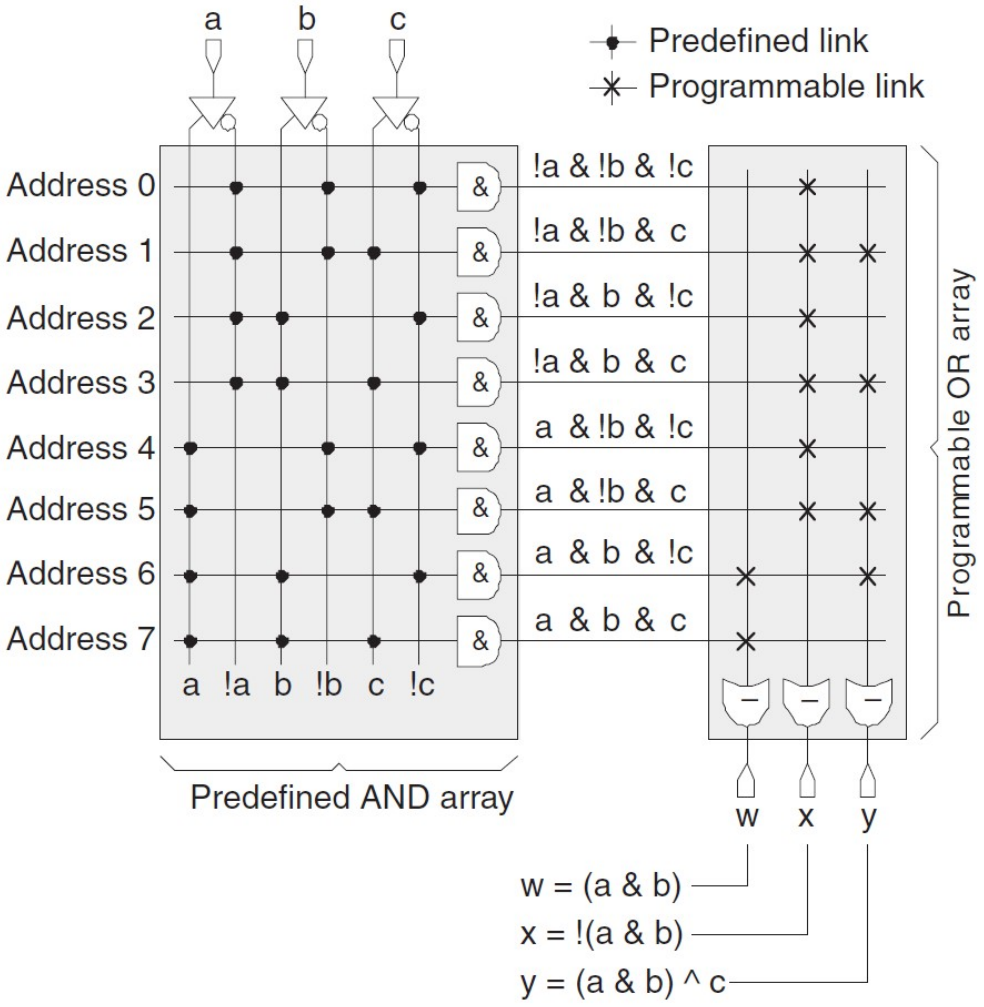
PROM

- The simplest Programmable Logic Device
- Predefined AND matrix, programmable OR matrix



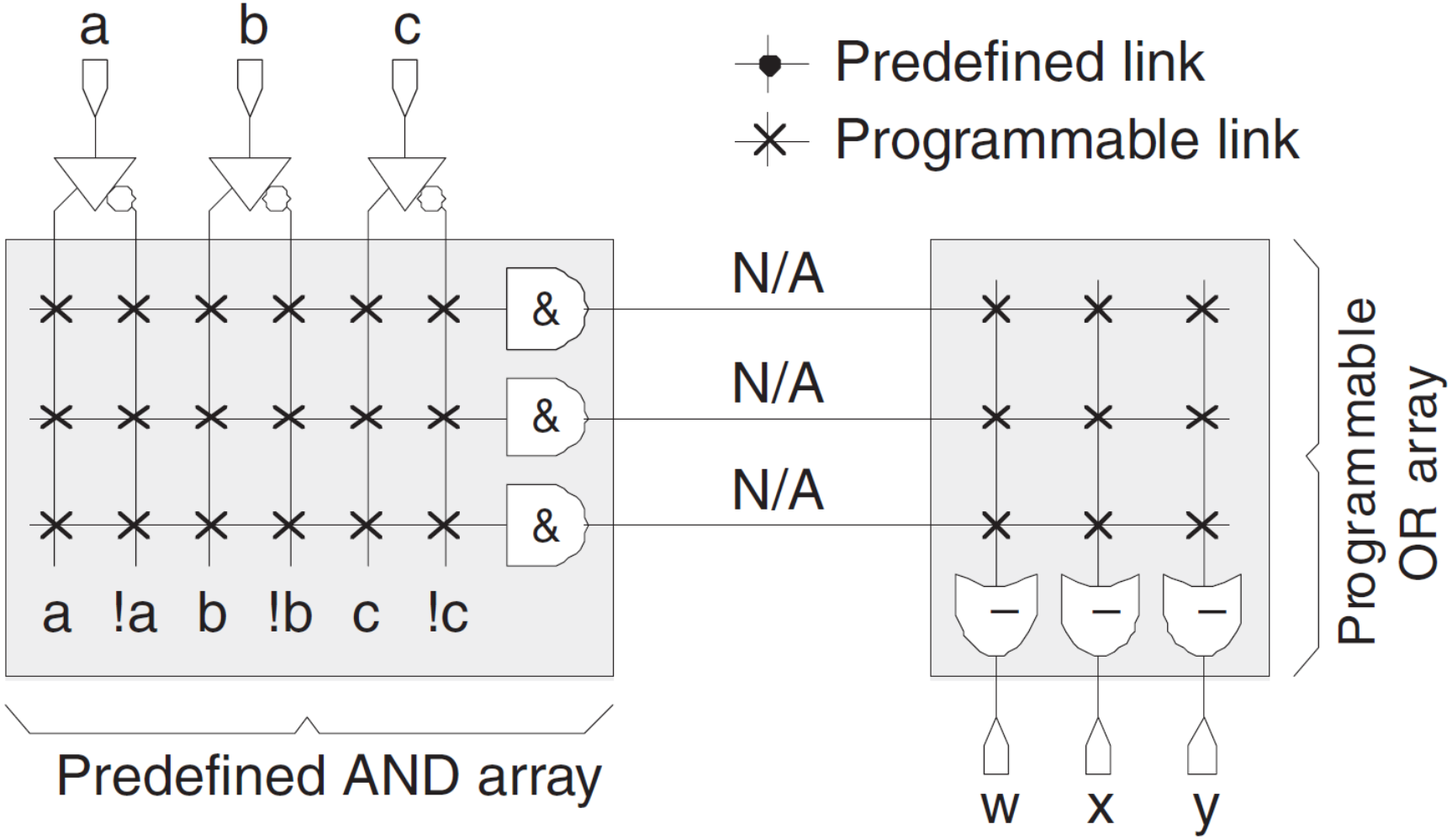
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

Programmed PROM



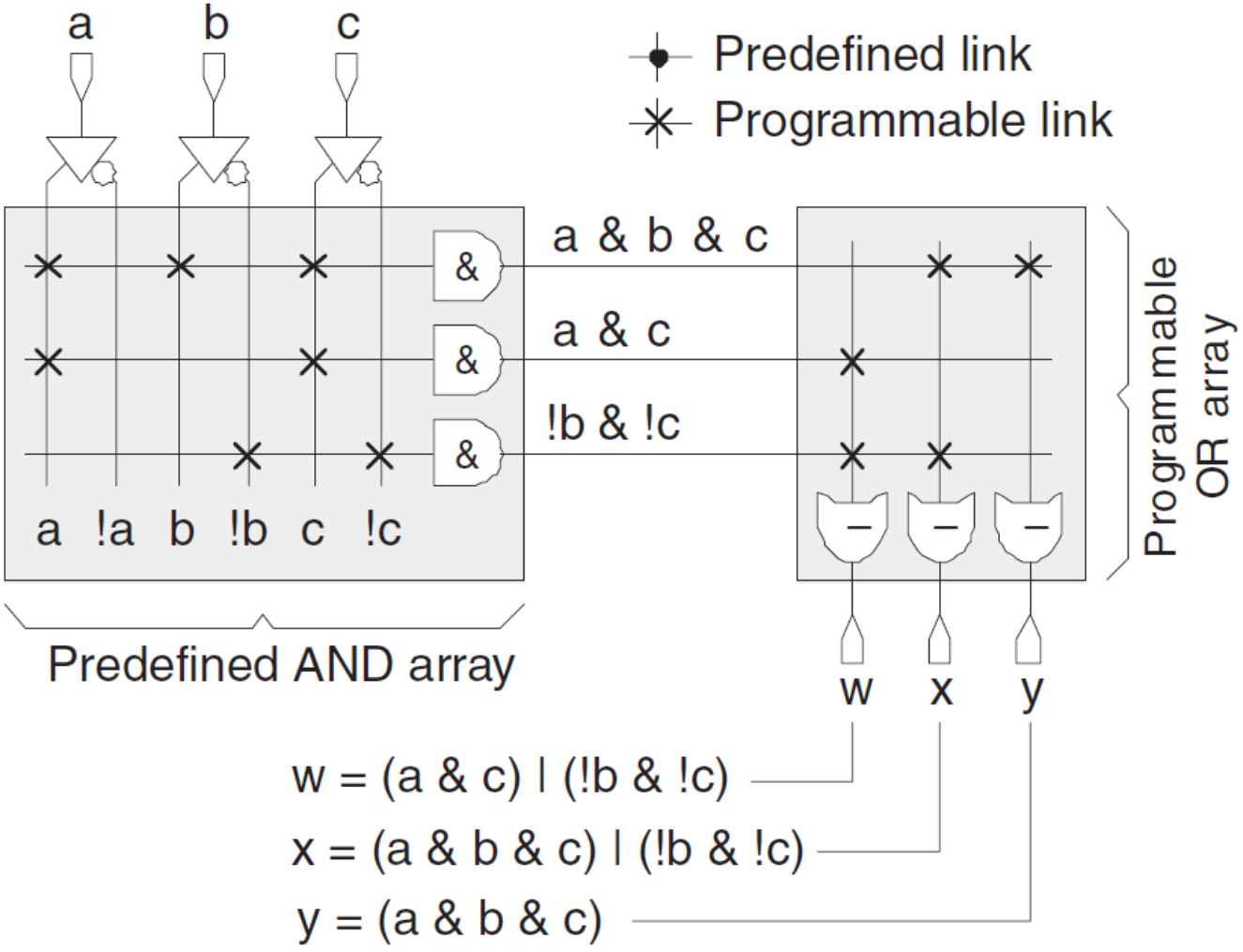
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

PLA (Programmable Logic Array)



Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

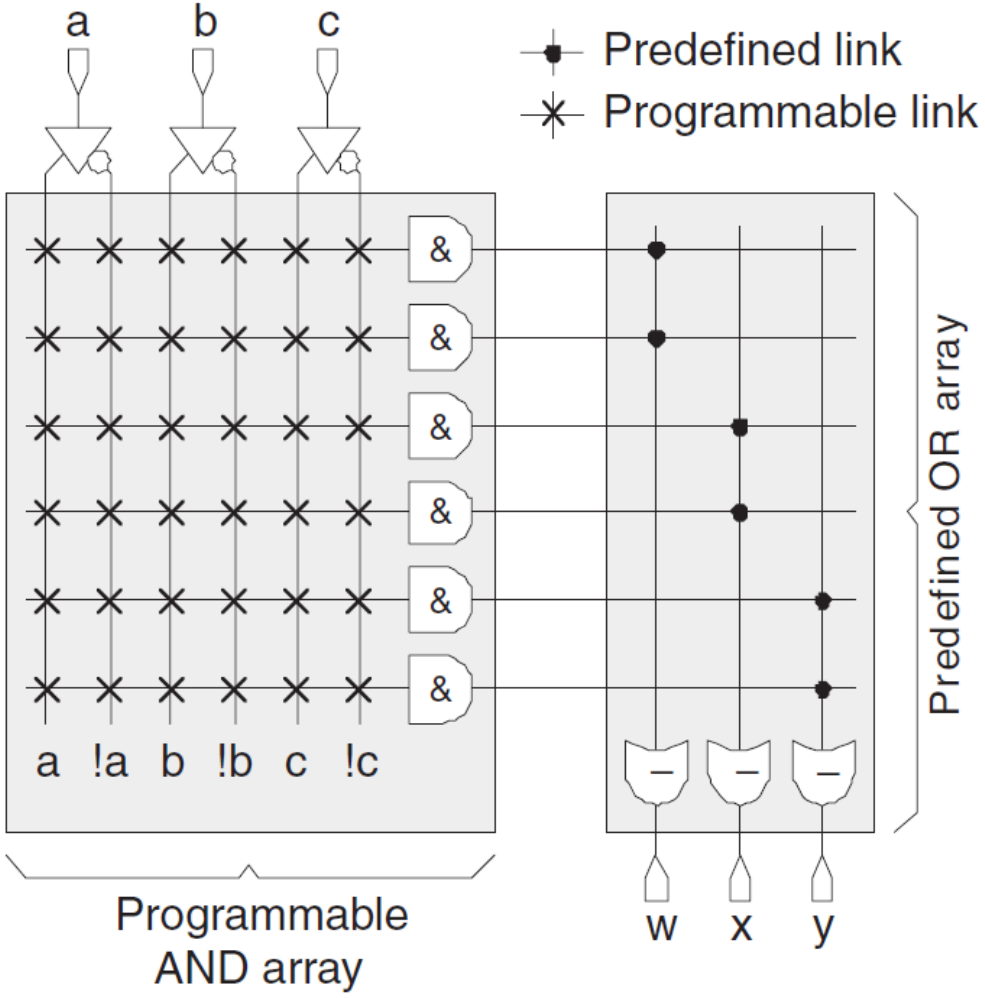
Programmed PLA



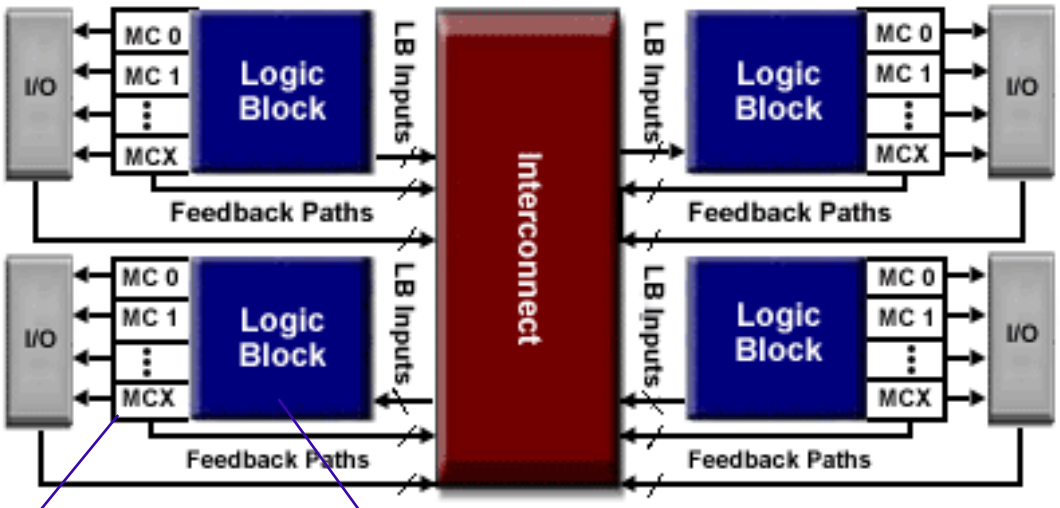
Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

PAL (Programmable Array Logic), GAL (Generic Array Logic)

- Complementary to PROM
- Programmable AND matrix, predefined OR matrix



Complex Programmable Logic Devices

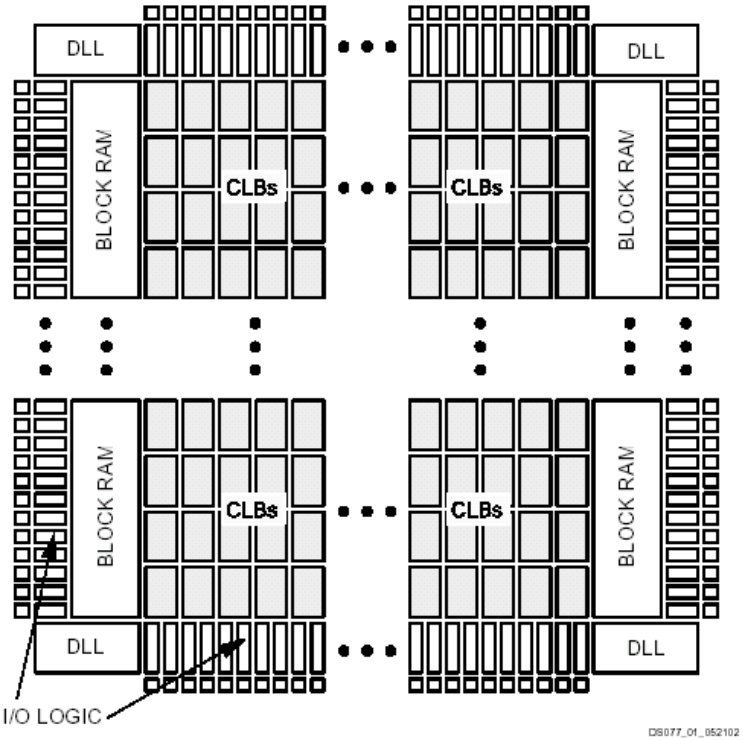


macrocells

fully programmable AND/OR array

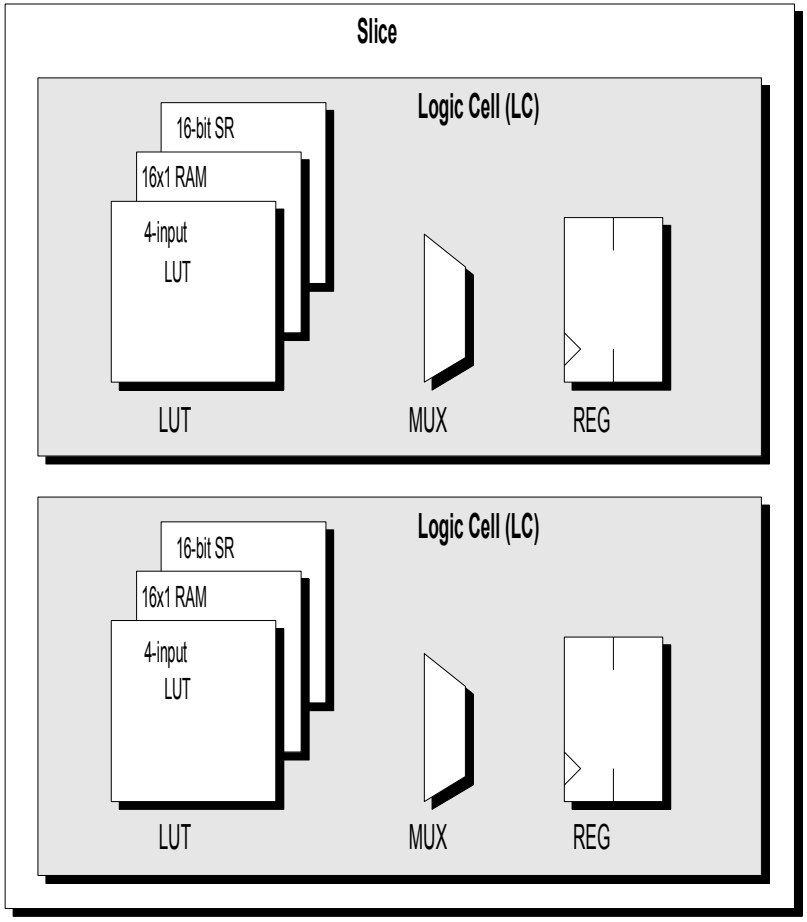
FPGAs

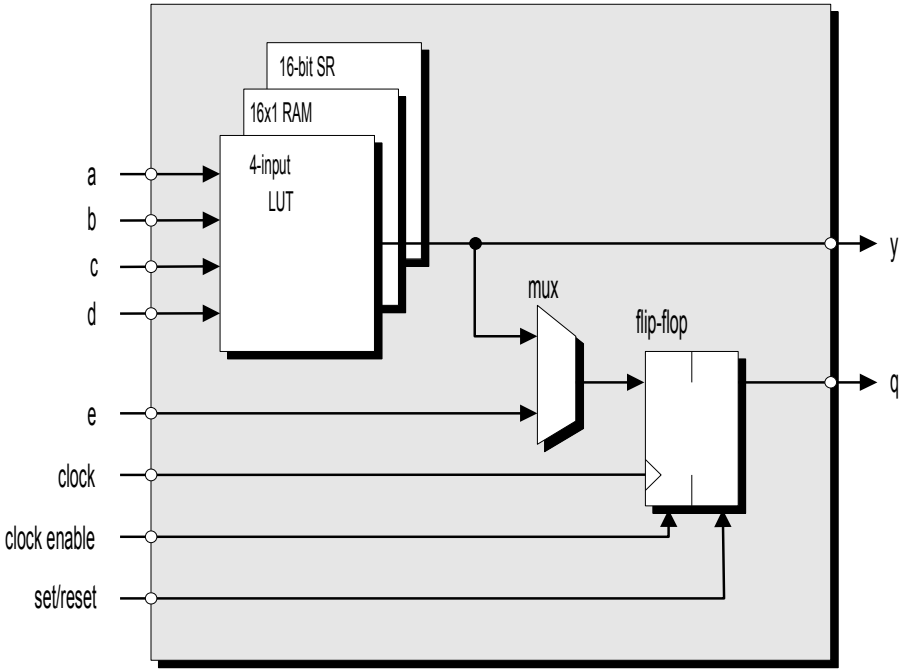
- Three main components:
  - Configurable Logic Blocks (CLB)
  - Programmable input/output blocks
  - Programmmable connections



CLB Slice

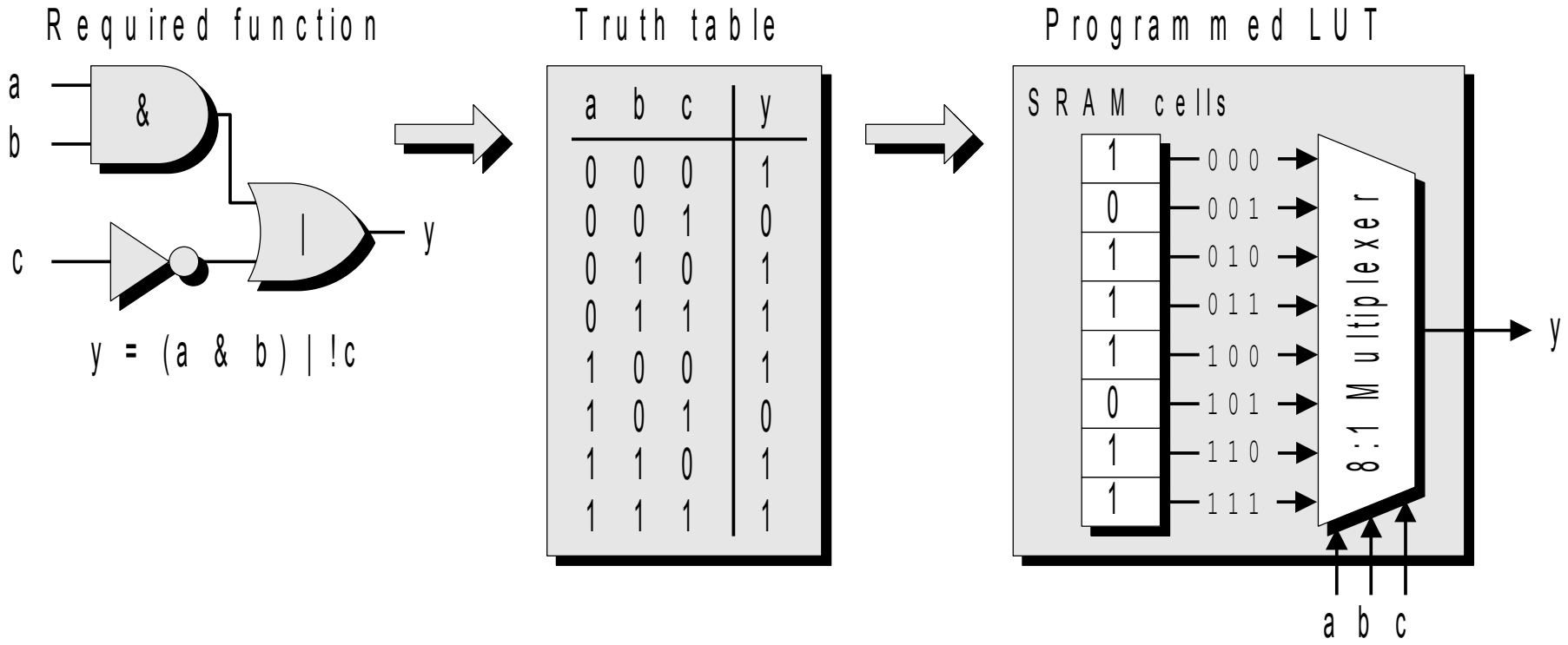
- Every slice contains two logic cells



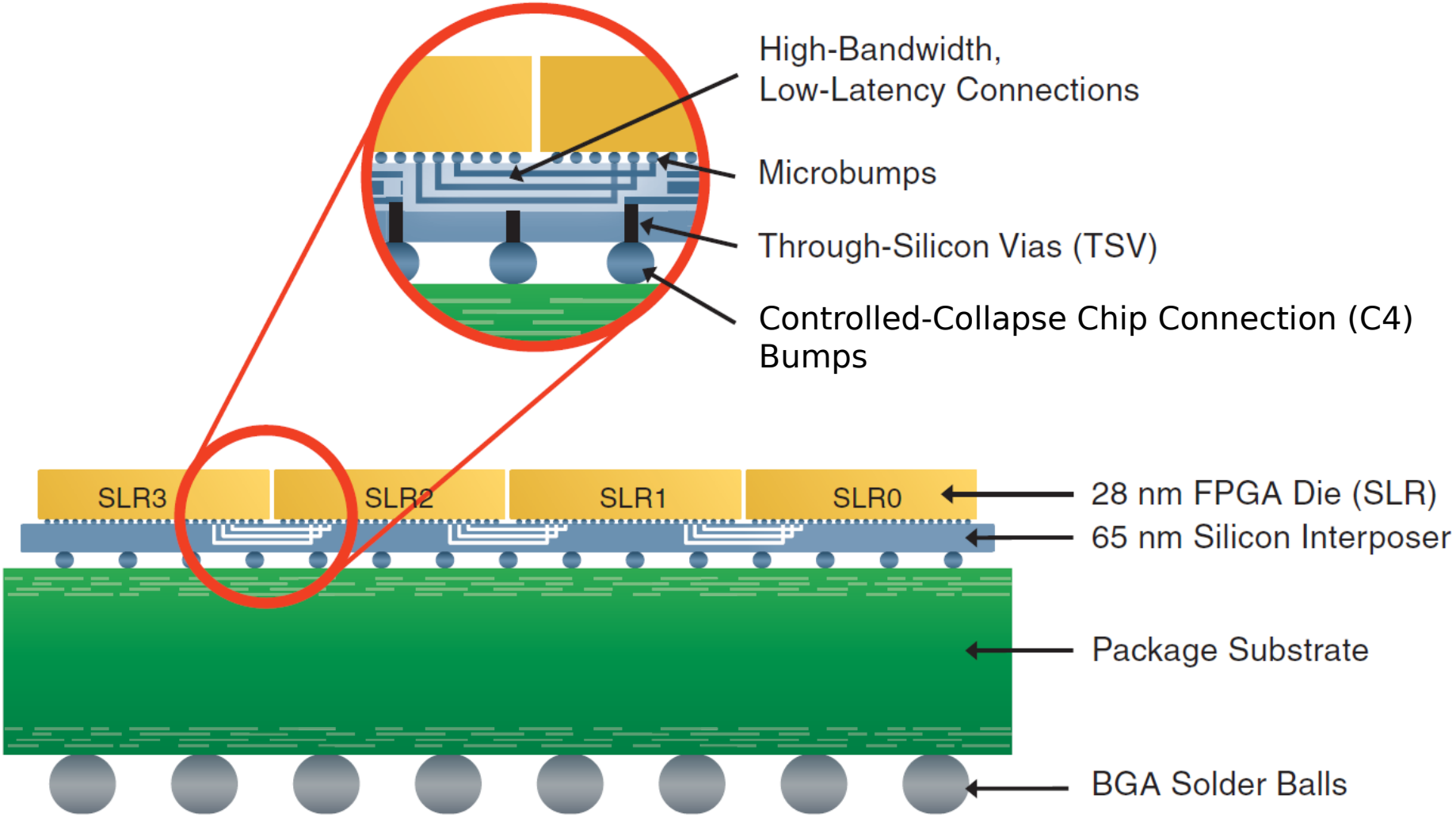


Source: Maxfield C., "The Design Warrior's Guide to FPGAs"

LUT (Look-Up Table)



Stacked Silicon Interconnect technology



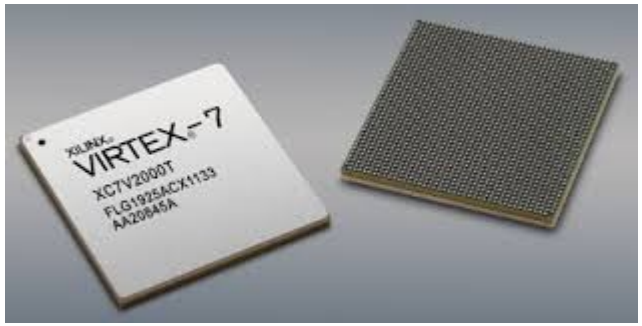
Source: Xilinx

Leading FPGA Manufacturers

- Giants
  - Xilinx Inc., 47% market share in 2012
  - Altera Corp., 41% market share in 2012
- Niche players
  - Lattice Semiconductor Corp.
  - Microsemi (Actel)
  - QuickLogic Corp.
- Legacy devices
  - Atmel
  - Cypress
- Startups
  - Tabula
  - Achronix
  - SiliconBlue

Xilinx

- Main products: FPGA circuits and design software



VIVADO

- The company does not own a silicon foundry (fabless company)
- Manufactures its chips in the factories of:
  - UMC (Taiwan)
    - Xilinx owns UMC shares since 1996
  - Seiko Epson (Japan)
  - TSMC (Taiwan)

Xilinx FPGA families

- **High-performance families**
  - **Virtex (220 nm)**
  - **Virtex-E, Virtex-EM (180 nm)**
  - **Virtex-II (130 nm)**
  - **Virtex-II PRO (130 nm)**
  - **Virtex-4 (90 nm)**
  - **Virtex-5 (65 nm)**
  - **Virtex-6 (40 nm)**
  - **Virtex-7 (28 nm)**
- **Low Cost Family**
  - **Spartan/XL – derived from XC4000**
  - **Spartan-II – derived from Virtex**
  - **Spartan-IIE – derived from Virtex-E**
  - **Spartan-3 (90 nm)**
  - **Spartan-3E (90 nm) – logic optimized**
  - **Spartan-3A (90 nm) – I/O optimized**
  - **Spartan-3AN (90 nm) – non-volatile,**
  - **Spartan-3A DSP (90 nm) – DSP optimized**
  - **Spartan-6 (45 nm)**
  - **Artix-7 (28 nm)**

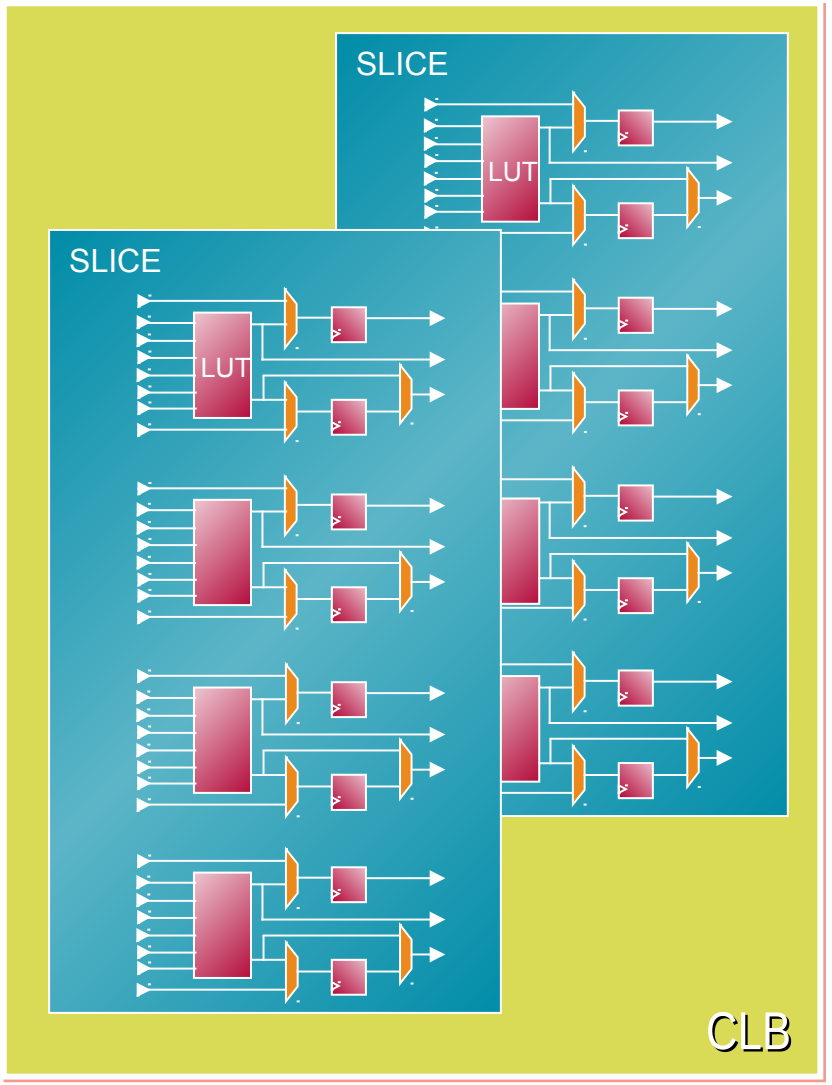
7 Series Xilinx FPGA Families

Maximum Capability	ARTIX-7 Lowest Power and Cost	KINTEX-7 Industry's Best Price/Performance	VIRTEX-7 Industry's Highest System Performance
Logic Cells	20K – 355K	70K – 480K	285K – 2,000K
Block RAM	12 Mb	34 Mb	65 Mb
DSP Slices	40 – 700	240 – 1,920	700 – 3,960
Peak DSP Perf.	504 GMACS	2,450 GMACs	5,053 GMACS
Transceivers	4	32	88
Transceiver Performance	3.75Gbps	6.6Gbps and 12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps
Memory Performance	1066Mbps	1866Mbps	1866Mbps
I/O Pins	450	500	1,200
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

Source: Xilinx

Xilinx 7-series CLB Structure

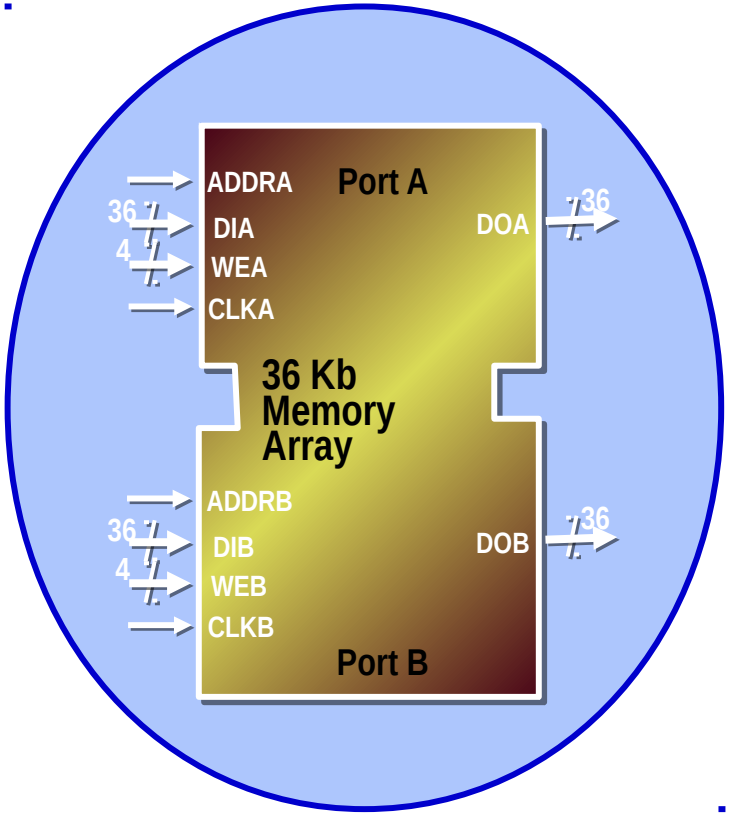
- Two side-by-side slices per CLB
  - Slice_M are memory-capable
  - Slice_L are logic and carry only
- Four 6-input LUTs per slice
  - Single LUT in Slice_M can be a 32-bit shift register or 64 x 1 RAM
- Two flip-flops per LUT



Source: Xilinx

Block RAM

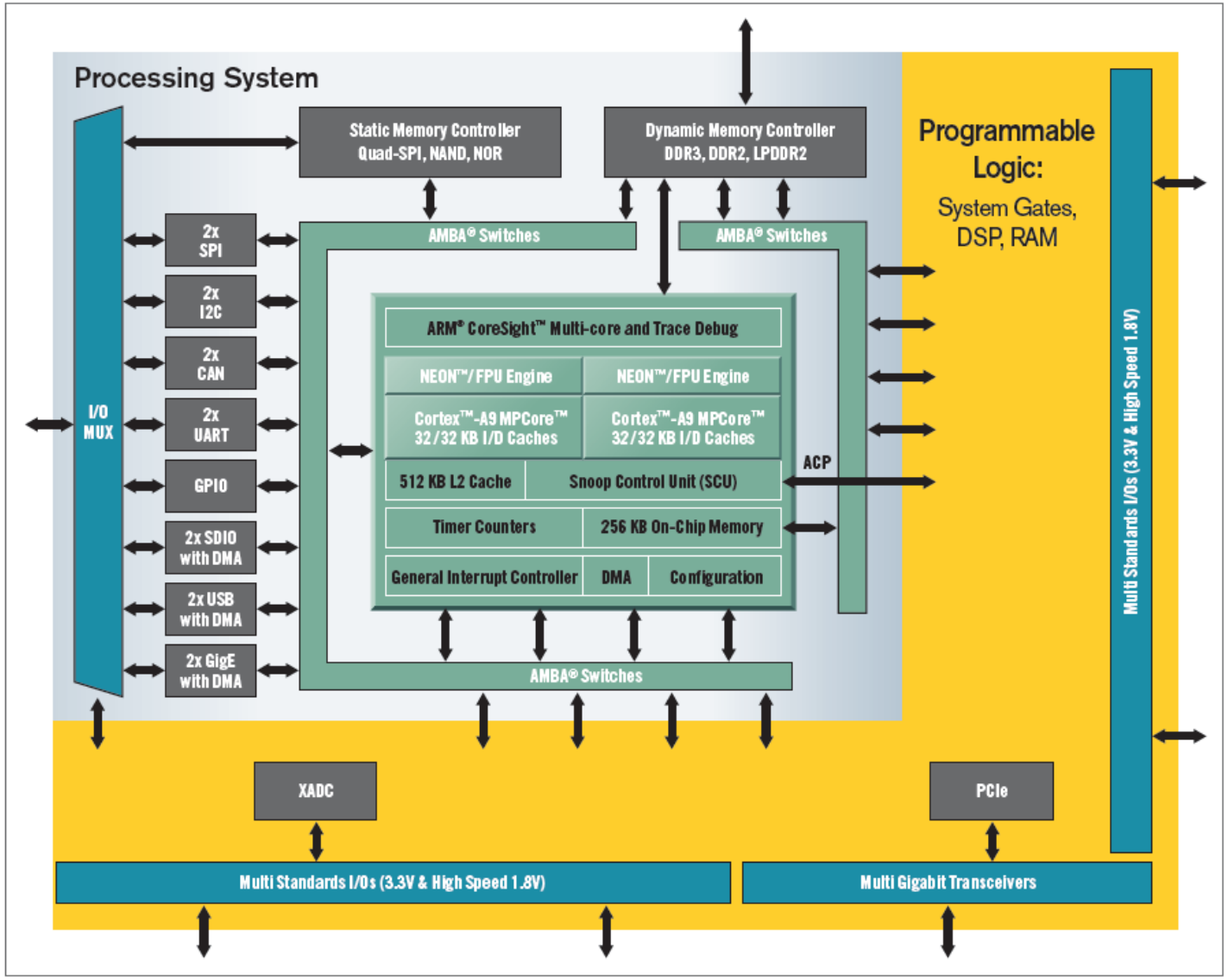
- 36K/18K block RAM
  - 32k x 1 to 512 x 72 in one 36K block
  - Simple dual-port and true dual-port configurations
  - Built-in FIFO logic
  - 64-bit error correction coding per 36K block
  - Adjacent blocks combine to 64K x 1 without extra logic



High-Speed Serial I/O Transceivers

- Available in all families
- GTP transceivers – up to 3.75 Gbps
  - Ultra high volume transceiver
  - Wire bond package capable
- GTX transceivers – up to 12.5 Gbps
  - Support for the most common 10 Gbps protocols
- GTH transceivers – up to 13.1 Gbps
  - Support for 10 Gbps protocols with high FEC overhead
- GTZ transceivers – up to 28 Gbps
  - Enables next generation 100–400Gbps system line cards

Zynq - Extensible Processing Platform



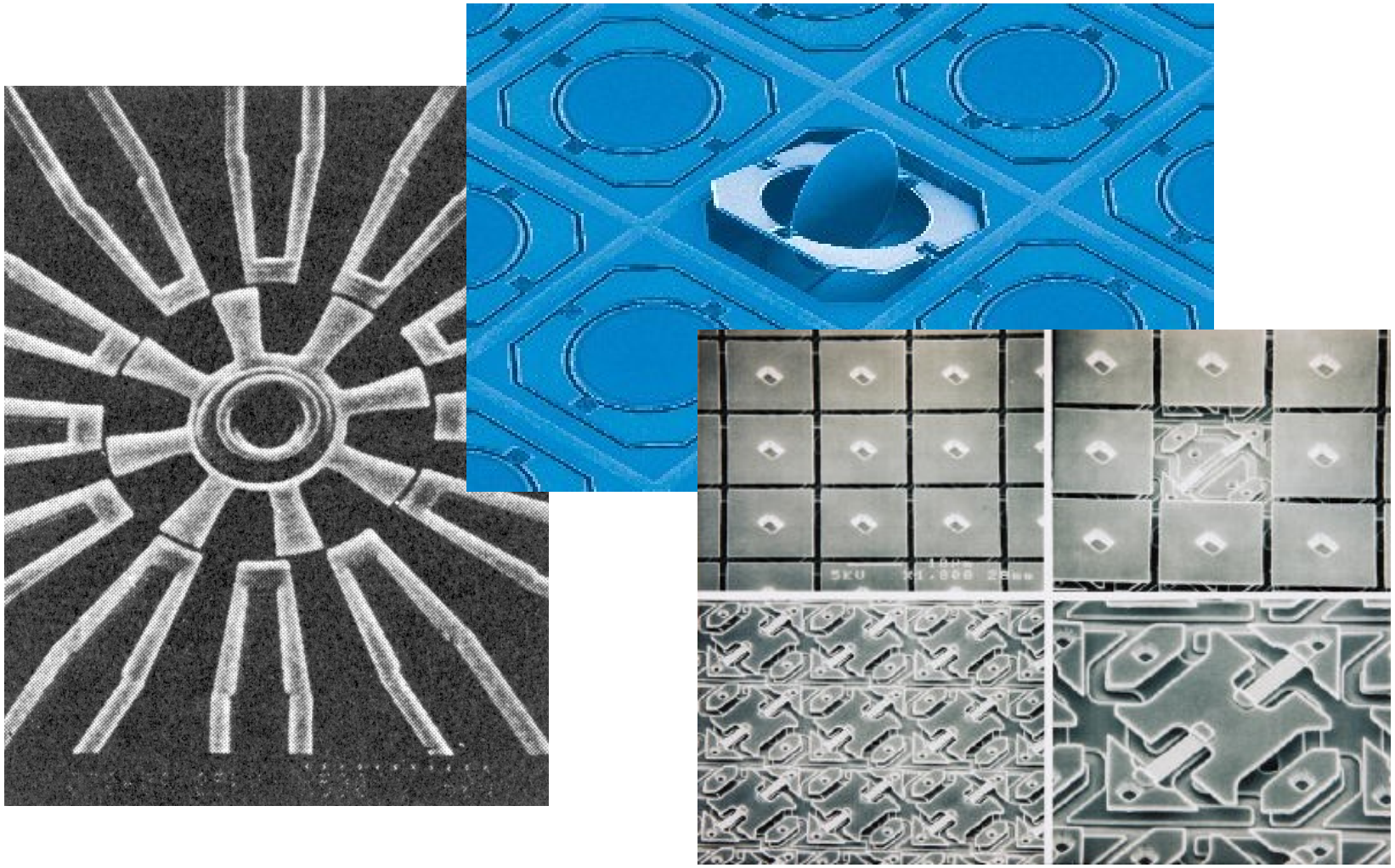
Zynq-7000 Product Table (Software View)

Device Name	Z-7010	Z-7020	Z-7030	Z-7045
Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
Processor Extensions	NEON™ and Single/Double Precision Floating Point			
Maximum Frequency	800 MHz			
L1 Cache	32 KB Instruction, 32 KB Data per processor			
L2 Cache	512 KB			
On-Chip Memory	256 KB			
External Memory Support	DDR3, DDR2, LPDDR2			
External Static Memory Support	2x QSPI-SPI, NAND, NOR			
DMA Channels	8 (4 dedicated to Programmable Logic)			
Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
Security	AES and SHA 256b for secure boot			
Peripherals and Static Memory Multiplexed I/O[1]	54			
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)
Programmable DSP Slices (18x25 MACCs)	80	220	400	900
Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS
PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
Security	AES and SHA 256b for secure configuration			
Multi-Standards 3.3V I/O[2]	100	200	250	350
Serial Transceivers[2]	—	—	4	16

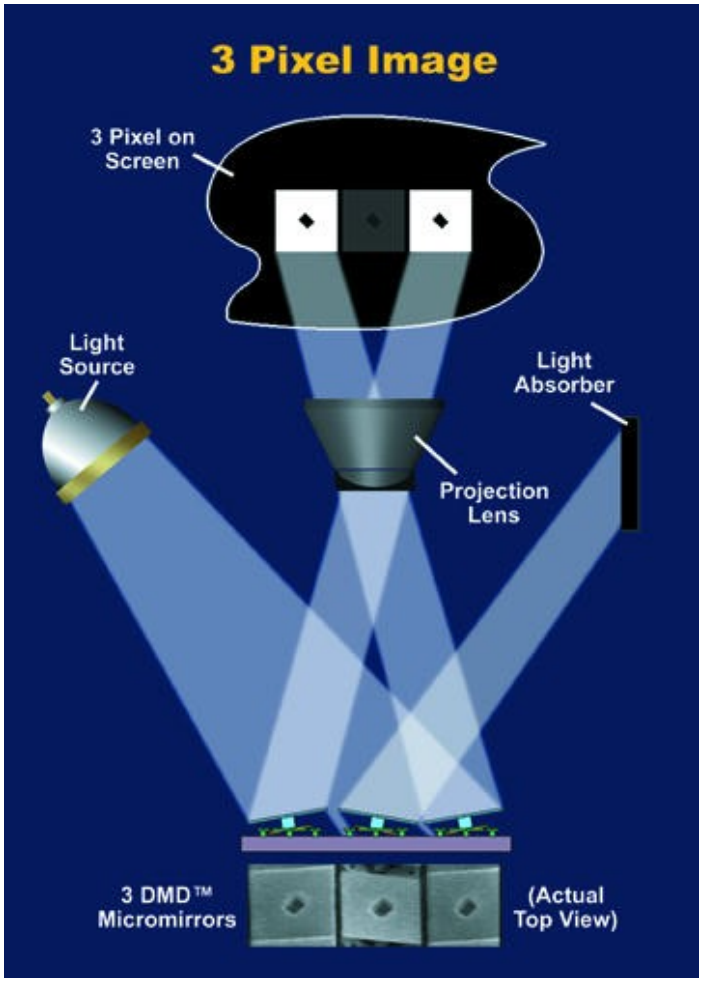
ASIC Advantages and Shortcomings

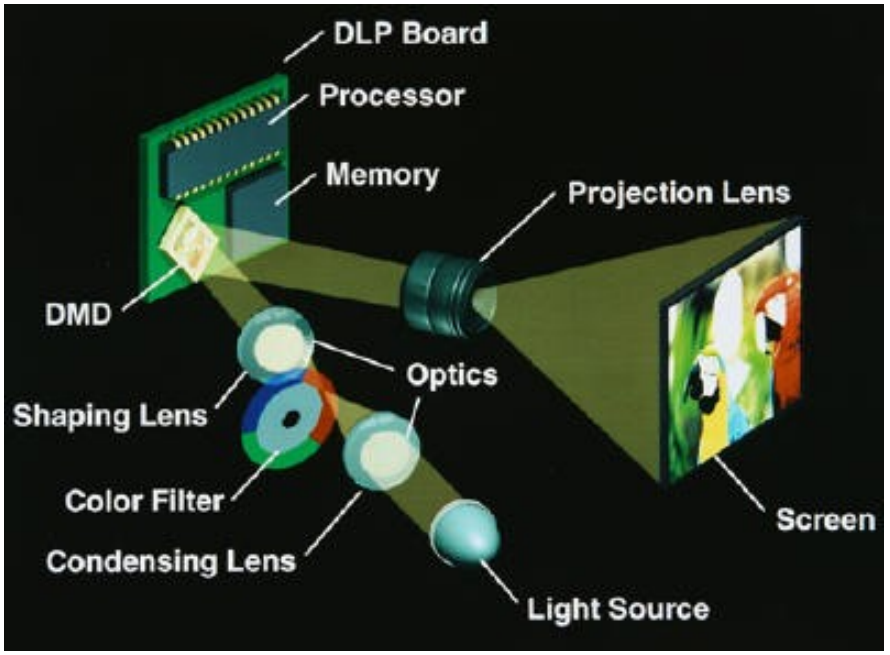
- ASIC Advantages
  - Optimized for a specific application
  - Effective area consumption
  - Higher performance (because of replacing a few circuits by one)
- ASIC Disadvantages
  - Higher cost
  - Development cost paid by the user
  - Single supplier
  - Need for own specialists in IC design
  - Long development cycle

The 90's – MEMS (Micro Electro-Mechanical Systems)



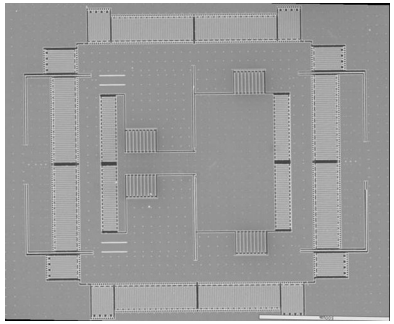
MEMS Application – Projection TV

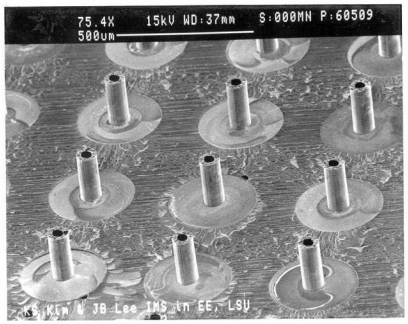


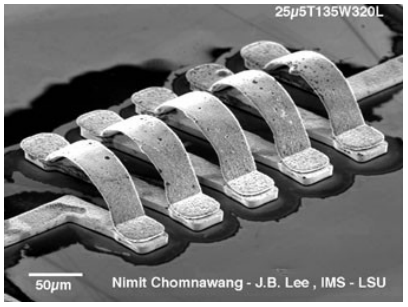


MEMS Applications

- Automotive sensors
  - Accelerometers, force/torque sensors, pressure sensors
- Bio MEMS
  - Micro total analysis system (μTAS), DNA sequencing chips, clinical diagnostics, drug delivery systems
- Chemistry
  - Lab-on-a-chip, microreactor
- Optics
  - Digital micromirror devices (TI), grating light valve (GLV)
  - Optical interconnects, switching
- Data storage
  - Precision servo, shock sensors for HDD, new data storage mechanisms
- RF, microwave for communication
- Power generation
  - Micromachined turbine engines, MEMS power generators



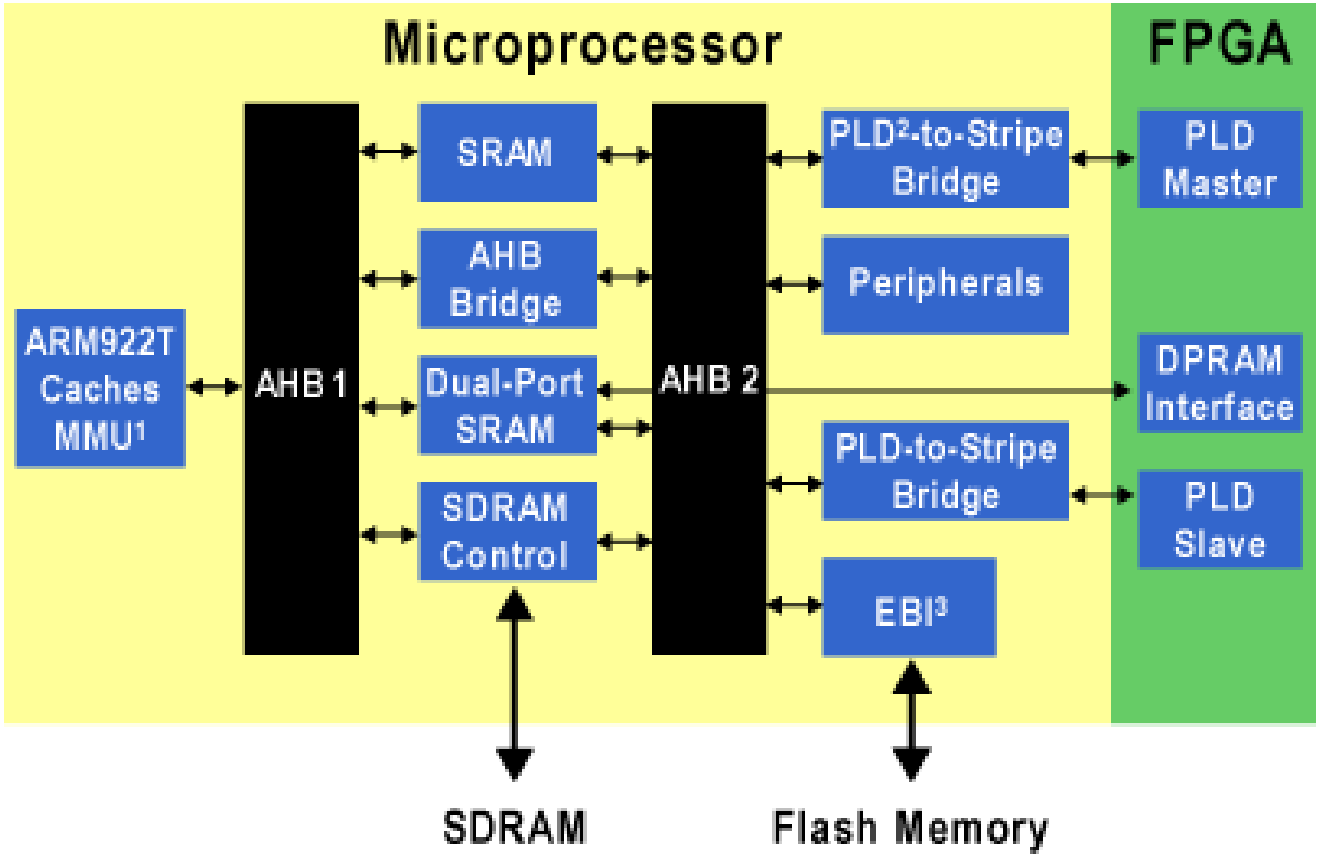




The 2000's – System on Chip (SoC)

- Processor core with external hardware (network, USB, PCI interface …) on the same chip
- Intelectual property (IP) -based design
- Design reuse
- Hardware-software co-design
- Custom or FPGA-based

Altera Excalibur Architecture

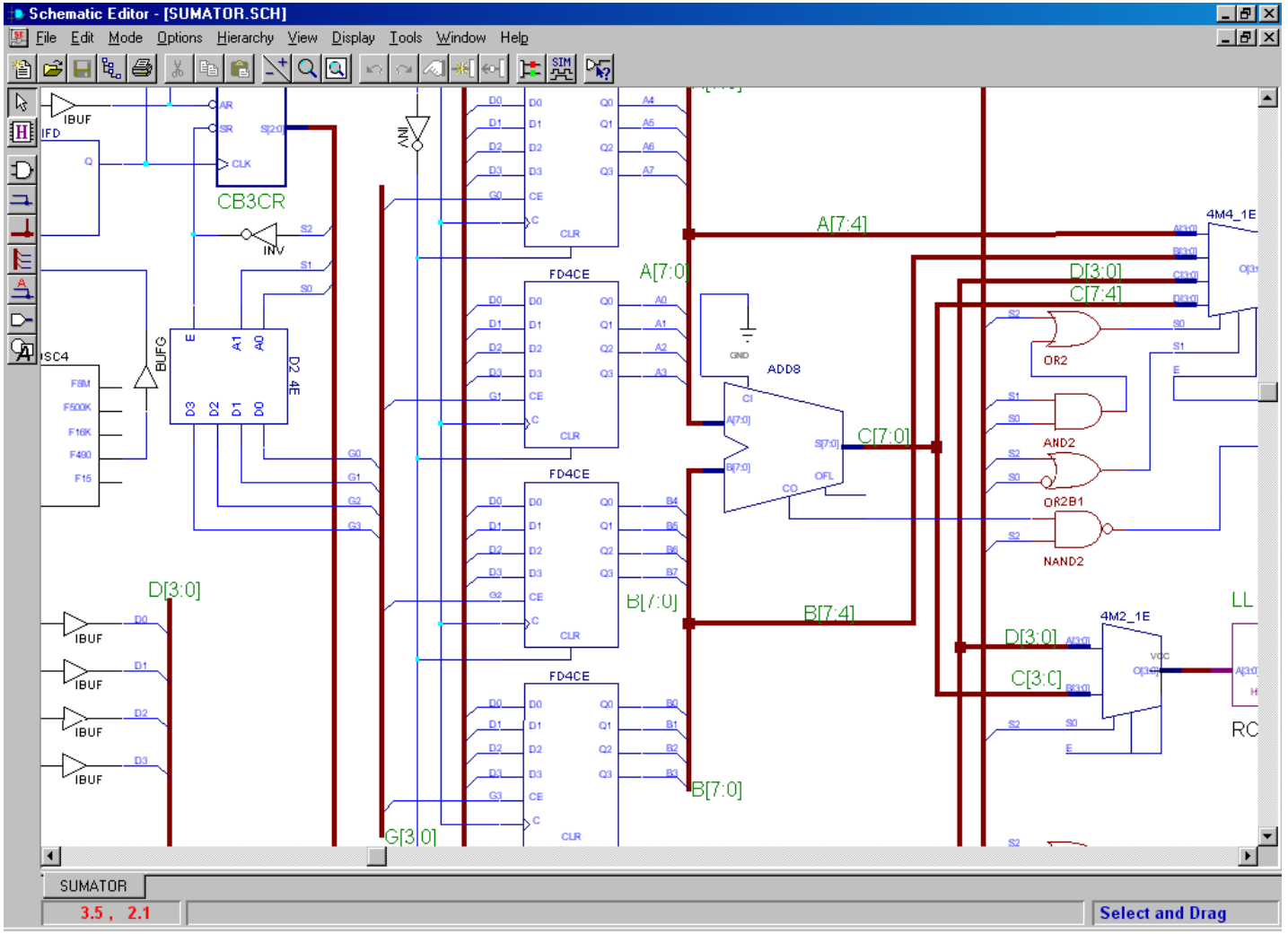


Tasks of A Designer

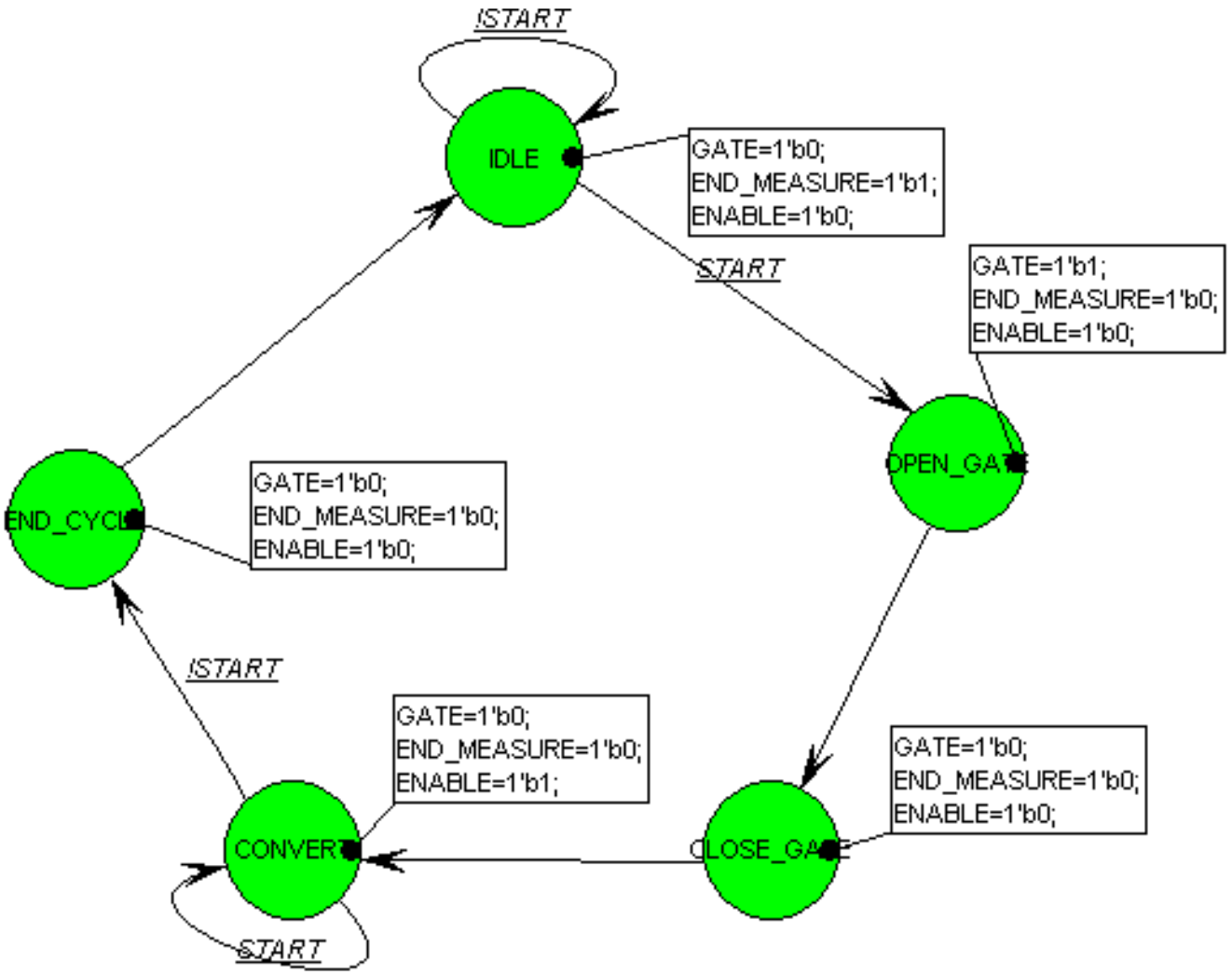
- Draw the schematic
- Draw the state diagram
- Describe in Hardware Description Language, e.g. VHDL* or Verilog
- Draw the masks

*VHDL - Very High Speed Integrated Circuits Hardware Description Language

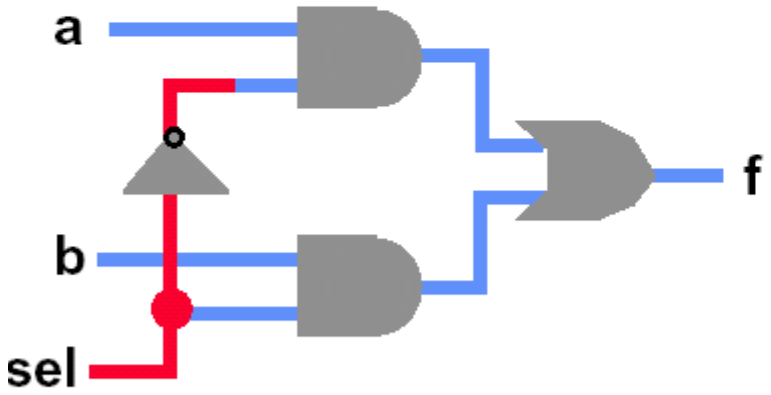
Draw The Schematic



Draw The State Diagram



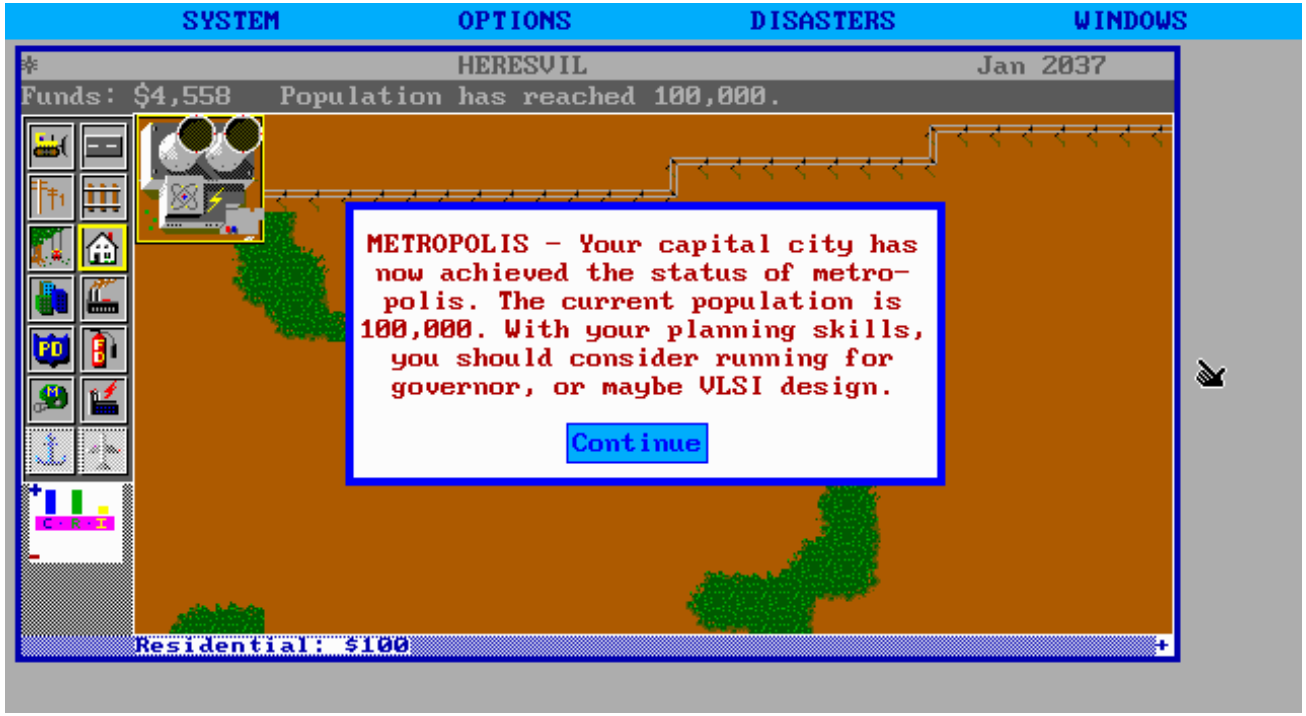
Describe in Hardware Description Language



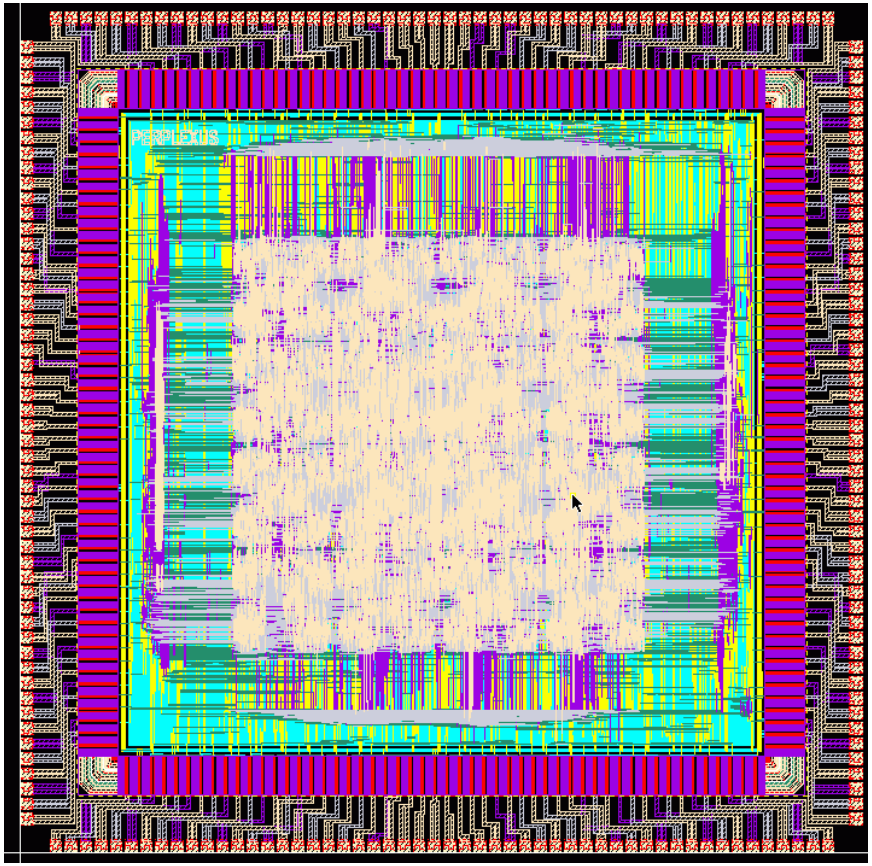

```
module mux (f, a, b, sel);
      output   f;
      input    a, b, sel;

      and #5   g1 (f1, a, nsel),
               g2 (f2, b, sel);
      or   #5  g3 (f, f1, f2);
      not      g4 (nsel, sel);
endmodule
```

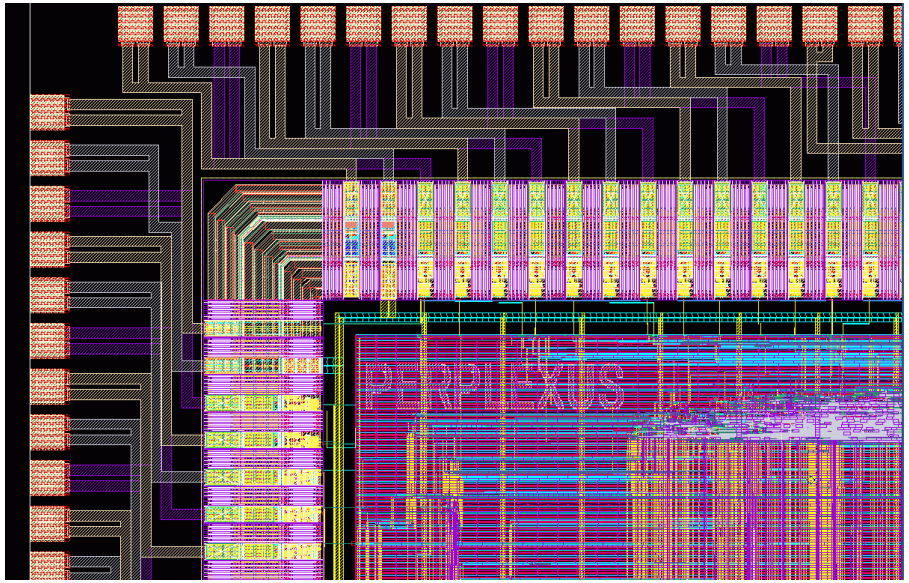
Draw The Masks

Draw The Masks

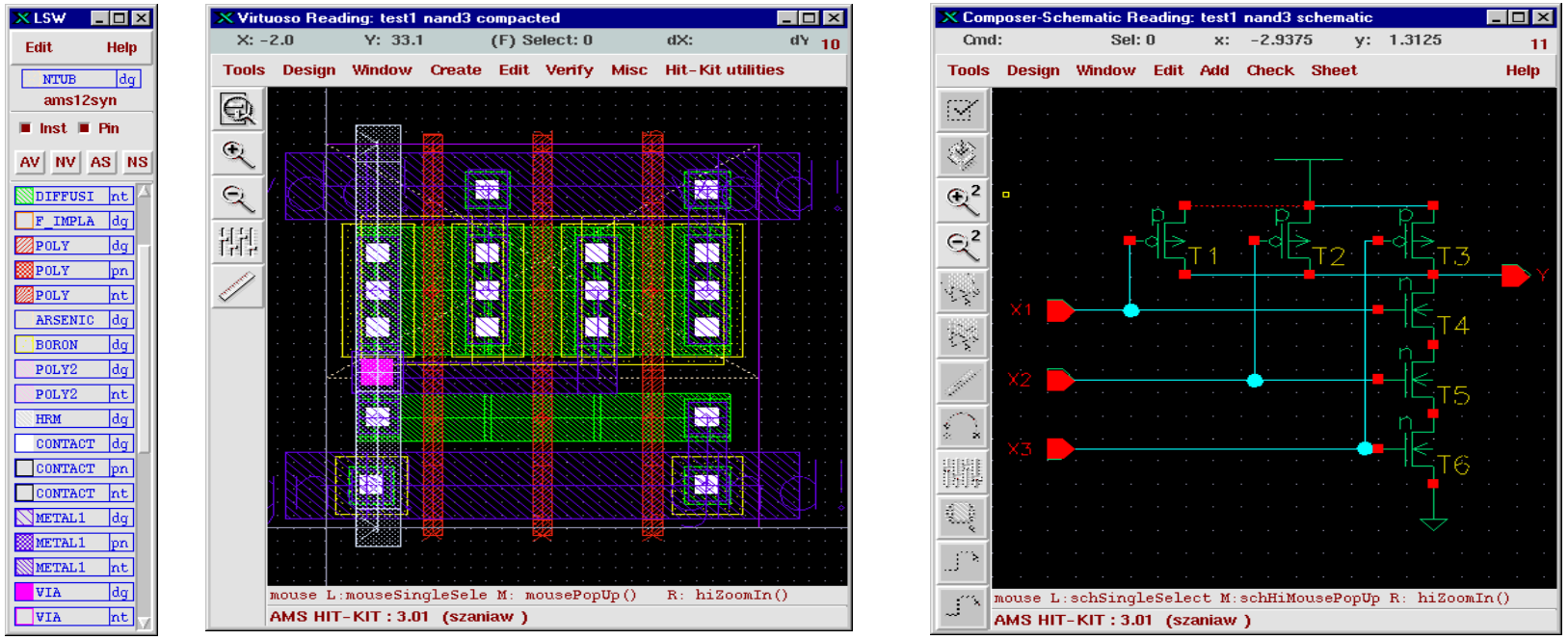


Draw The Masks

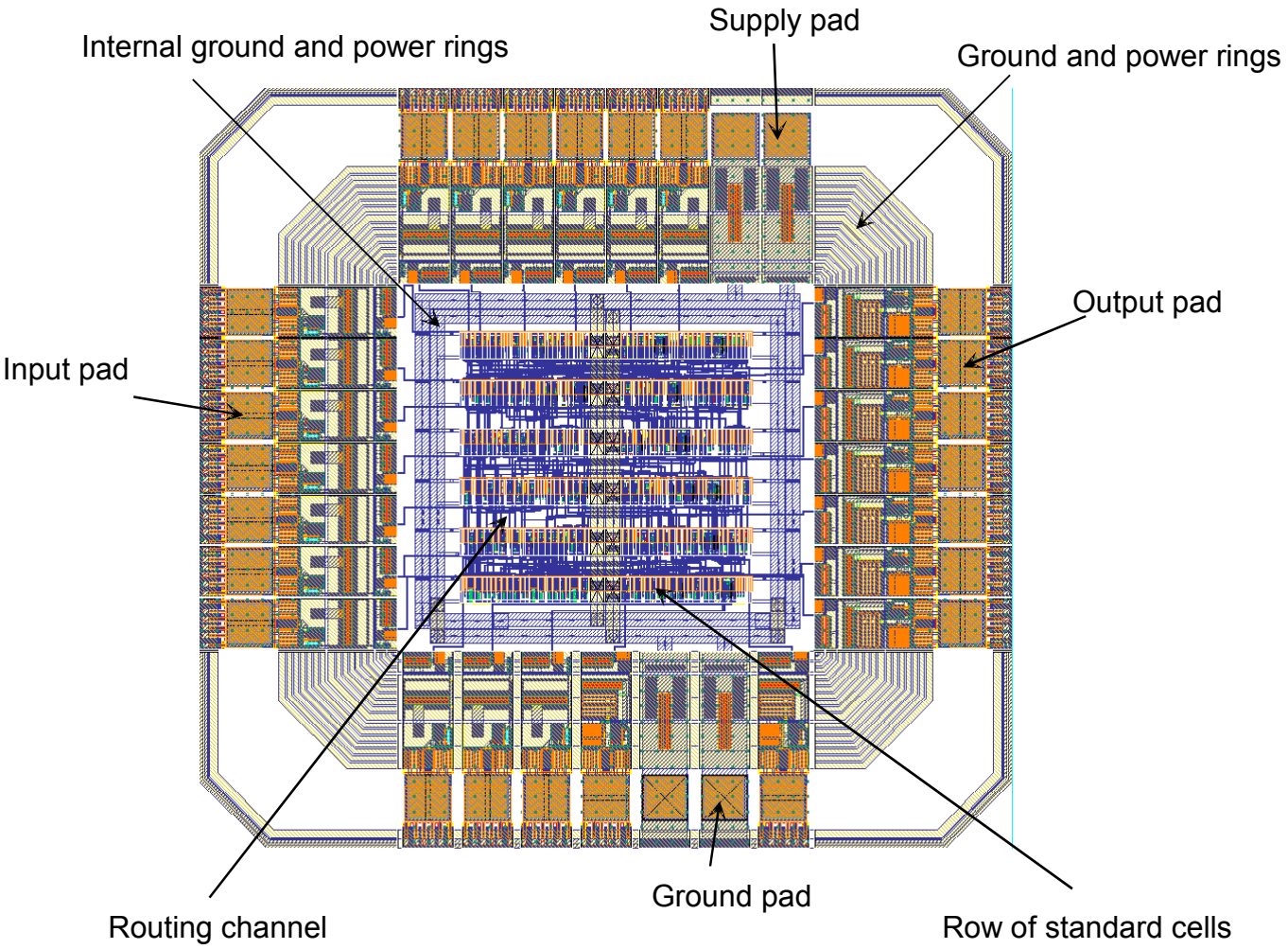




Masks and Schematic in Cadence



IC Layout


Internal ground and power rings
Supply pad
Ground and power rings
Output pad
Input pad
Routing channel
Ground pad
Row of standard cells

Design Tools

- Xilinx
- Synopsys
- Cadence
- Mentor Graphics

Functions of the Design Tools

- Edition of text, schematic, layout
- Logic synthesis
- Layout versus Schematic (LVS)
- Design/Electrical Rule Checking (DRC/ERC)
- Place and Route
- Simulation

ASICs in Poland

- Programmable circuits
- EUROPRACTICE
- IET Experimental Line
- Western/Far East Silicon Foundries