Yield, Reliability and Testing

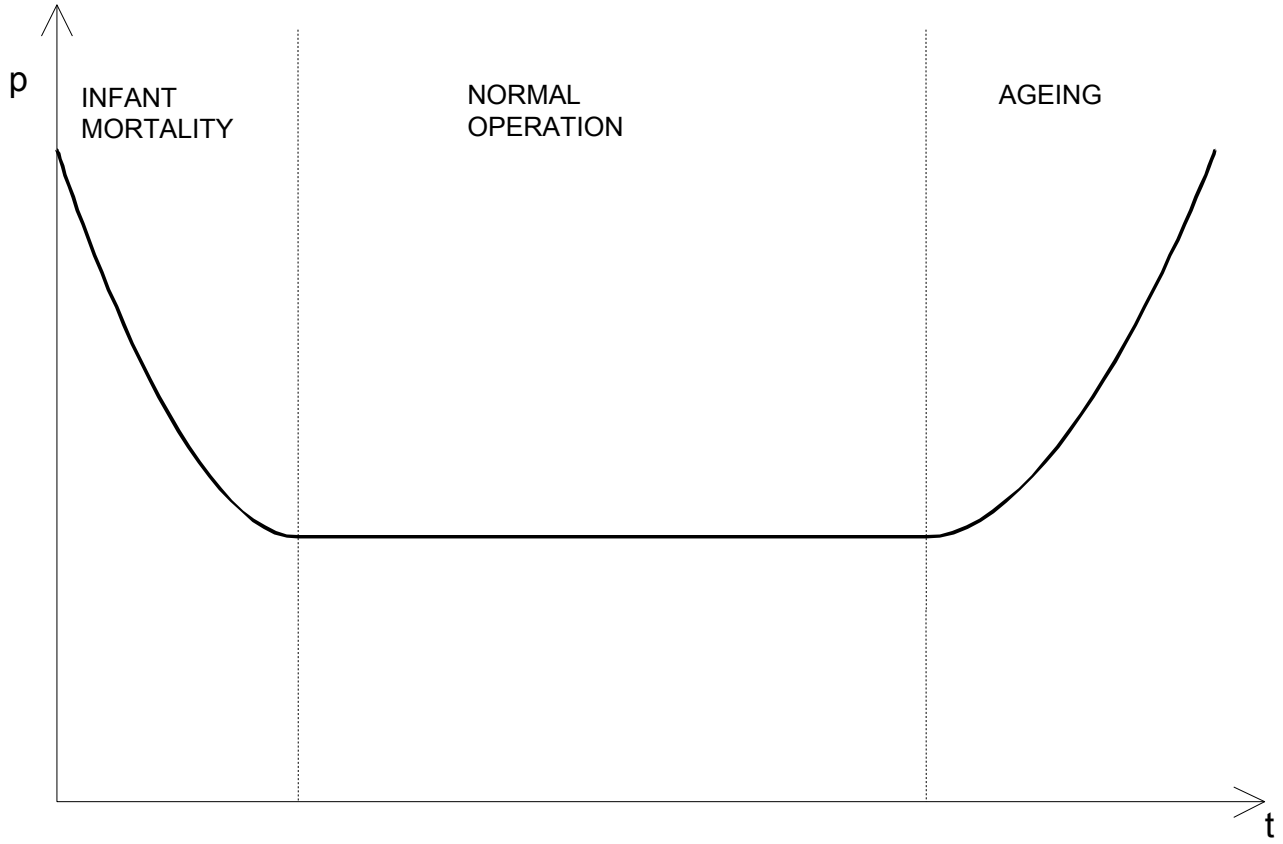
The Progressive Trend of IC Technology

Integration level	Year	Number of transistors	DRAM integration
SSI	1950s	less than 10^2	
MSI	1960s	10^2 - 10^3	
LSI	1970s	10^3 - 10^5	4K, 16K, 64K
VLSI	1980s	10^5 - 10^7	256K, 1M, 4M
ULSI	1990s	10^7 - 10^9	16M. 64M, 256M
SLSI	2000s	over 10^9	1G, 4G and above

Costs of Fault Detection

Production stage	Cost of detected fault
Die	US$ 0,01 - US$ 0,10
Packaged IC	US$ 0,10 - US$ 1,00
PCB	US$ 1,00 - US$ 10,00
Electronic system	US$ 10,00 - US$ 100,00
Shipped product	US$ 100,00 - US$ 1000,00

Failure Rate During Product Life



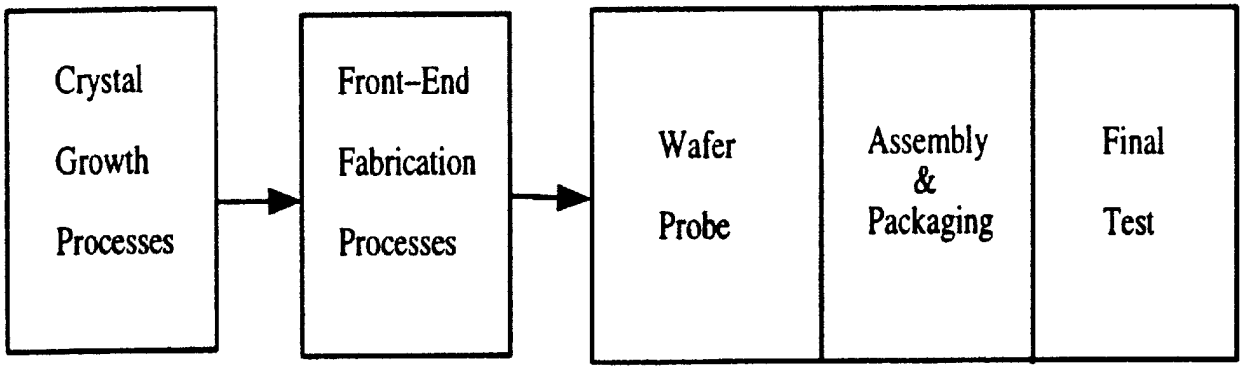
Failure Mechanisms

- Stress failures
  - Electrical Overstress (EOS)
  - Electrostatic Discharge (ESD)
- Intrinsic failures
  - Crystal defects, processing defects, gate oxide breakdown, ionic contamination etc.
- Extrinsic failures
  - Packaging, metallization, bonding, attachment, radiation

Yield

$$\text{Yield} = \frac{\text{Number of working devices}}{\text{Number of manufactured devices}}$$

$$Y = Y_1 \cdot Y_2 \cdot \ldots \cdot Y_n$$



	Wafer Process Yield	Wafer Probe Yield	Assembly Yield	Final Test Yield
Typical Average Yield	94%	50%	96%	90%

Some Yield Examples

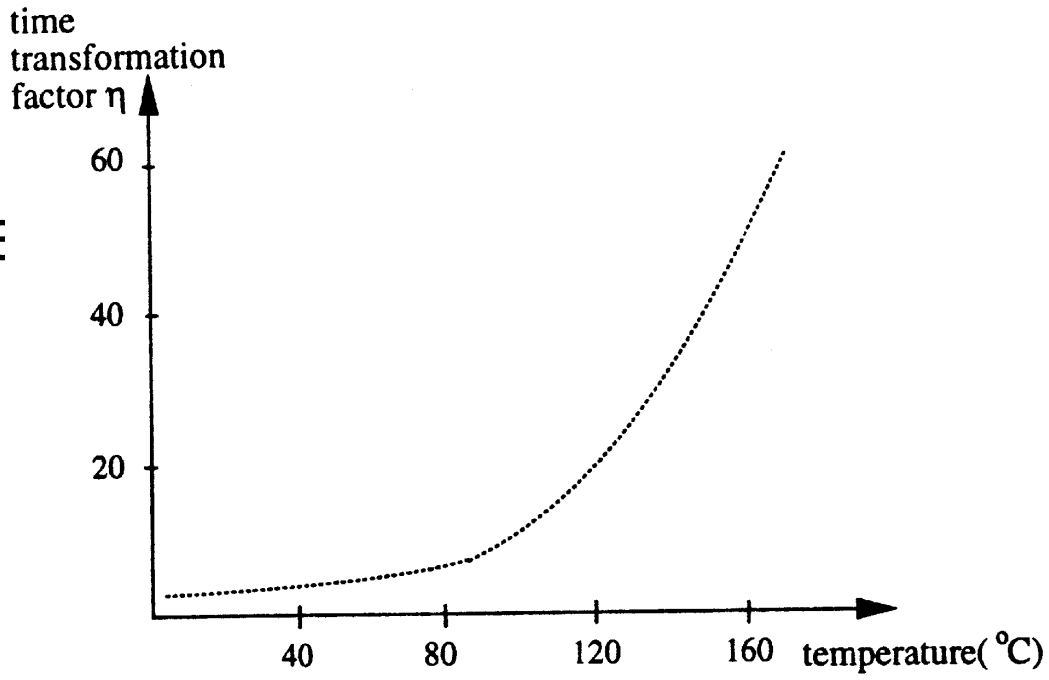
Product	4M DRAM	16M DRAM	16M DRAM	Pentium P54C
Feature size	0.6μ	0.5μ	0.35μ	0.6μ
Wafer size	150mm	200mm	200mm	200mm
Tested wafer cost	$600	$1,140	$1,410	$1,500
Die size	54.8mm^2	116.1mm^2	100mm^2	163mm^2
Total dice available / wafer	254	212	253	148
Defect density	0.5/cm^2	1.0/cm^2	0.6/cm^2	1.5/cm^2
Probe yieid	80%	35%	58%	15%
Number of good dice	203	74	146	22
Factory cost /die	$4.14	$23.25	$12.63	$153.31
Average selling price / die	$12	$60	$27	$700
Approx. revenue/wafer start	$2,140	$3,120	$3,430	$11,200
Revenue/sq. in. started	$70	$62	$68	$223
Gross margin	65%	61%	53%	78%

Testing Costs

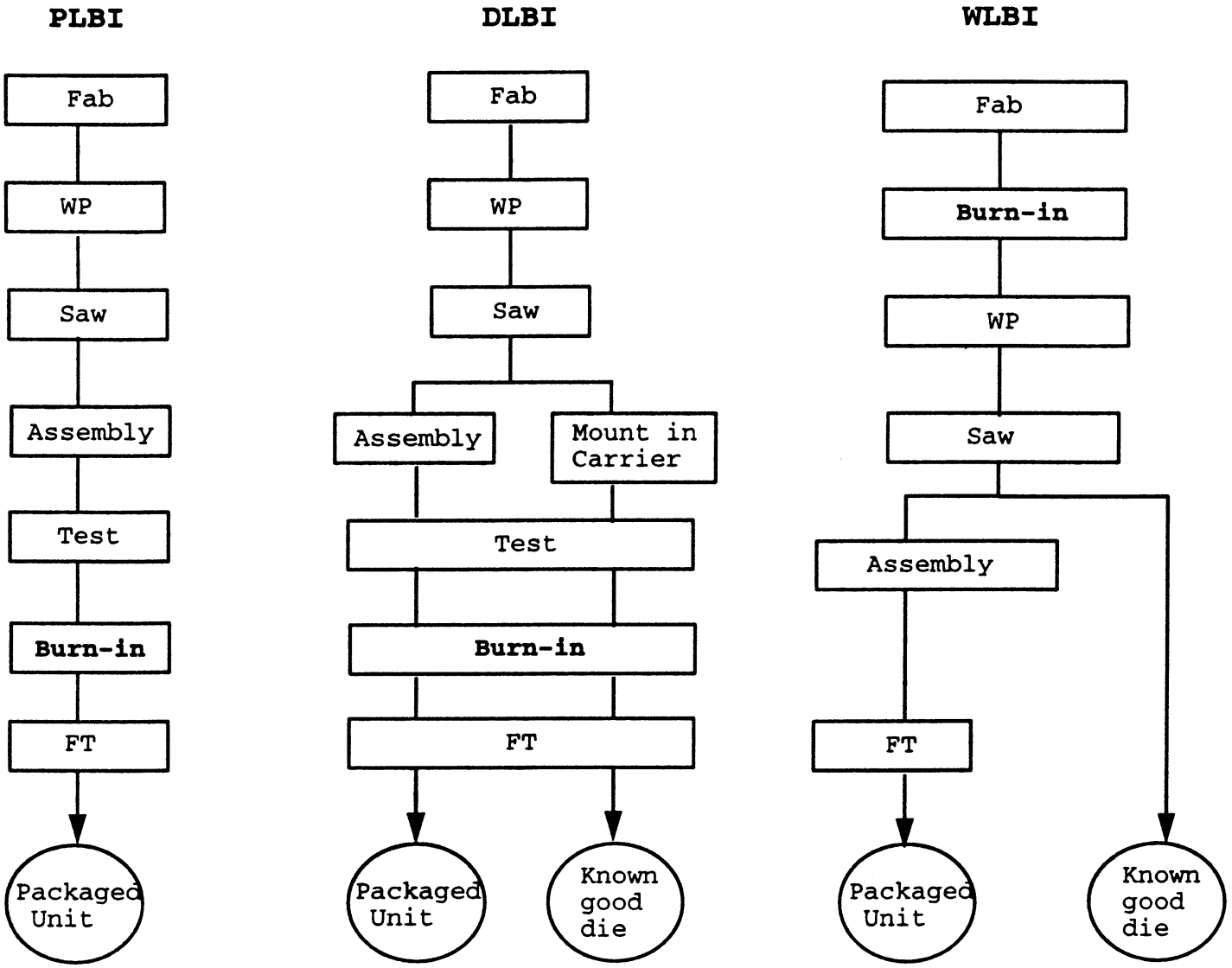
Product	Final test cost ($)	Final test yield(%)
8-bit MPU	0.10	95
20,000 gate array	0.80	90
1MDRAM	0.30	93
4M DRAM	0.40	90
16M DRAM	0.80	75
4K GaAs SRAM	1.00	80
32-bit MPU (386)	2.50	90
32-bit MPU (P54C)	25.00	75

Burn-in

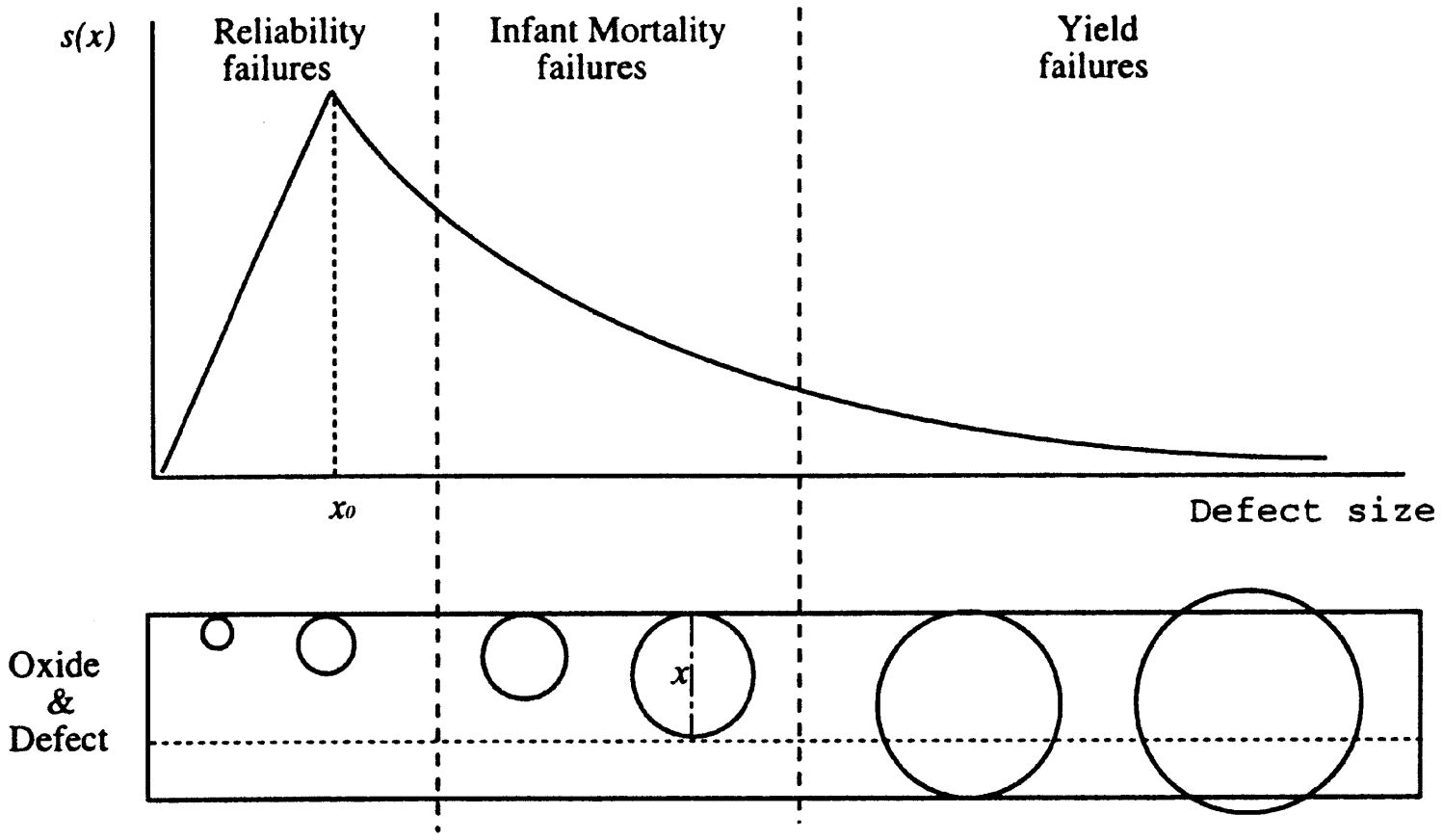
- Units subjected to higher than usual levels of stress
  - voltage
  - temperature
  - humidity
  - pressure



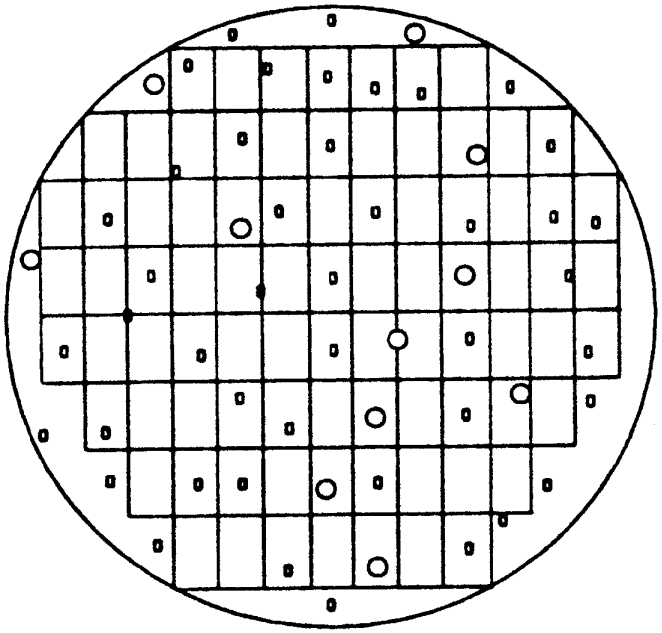
Burn-in (contd.)

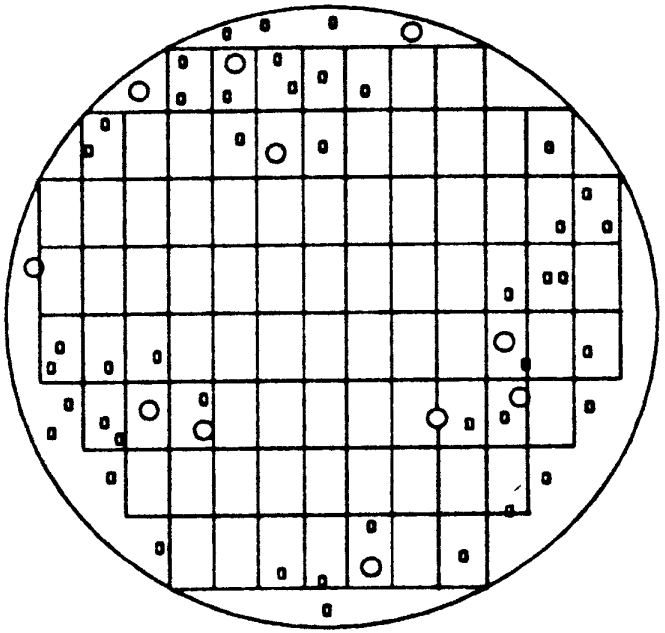


Yield and Reliability



Defect Clustering





Reliability Measures

- Mean Time Beetween Failures (MTBF)
- Mean Time To Failure (MTTF)
- Failures in Time (FITs),
  - 1FIT=1 failure in 10^9 h
  - To estimate FIT of the system, we add FITs of the components

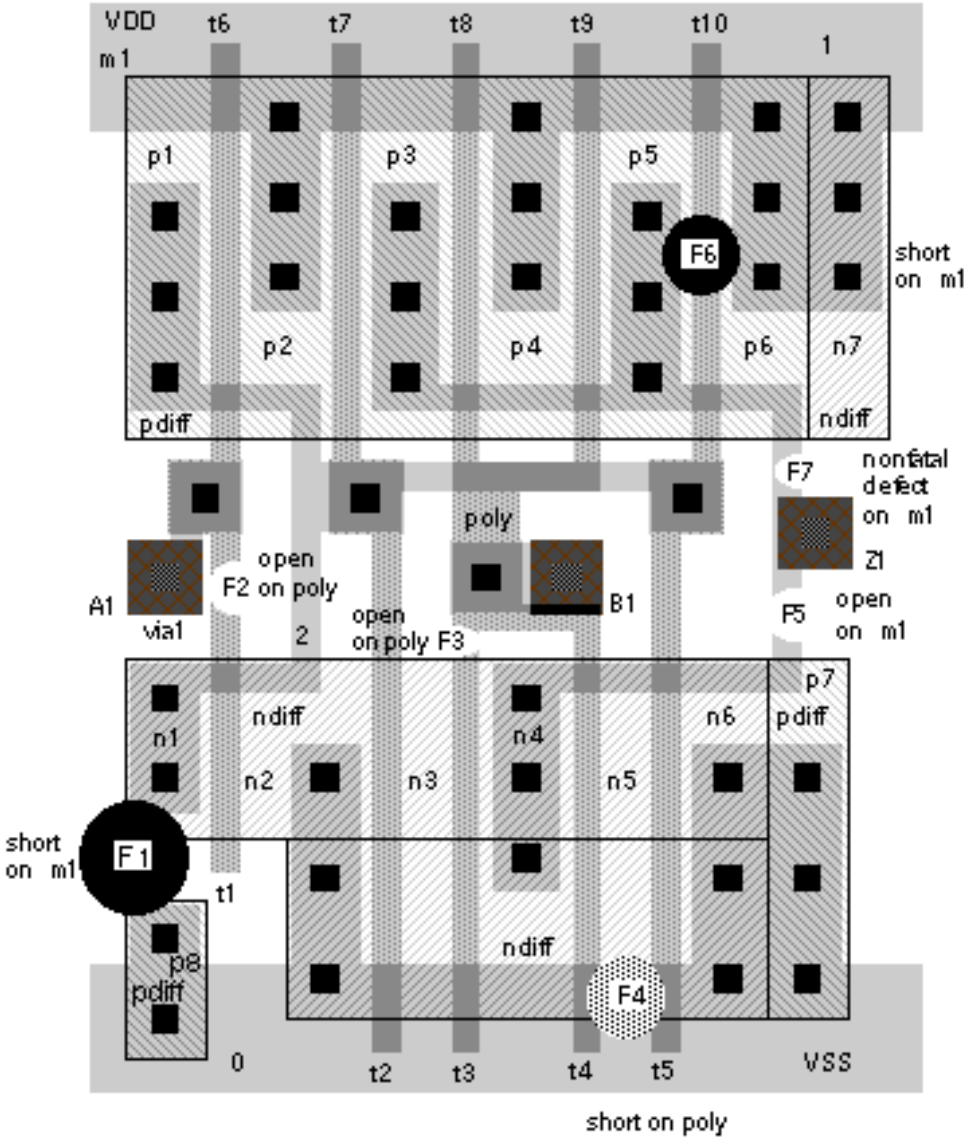
Reliability Example (SparcStation 1)

- Discrete components
  - Microprocessor (standard part) 5 FITs
  - 100 TTLs, 50 at 10 FITs, 50 at 15 FITs
  - 100 RAM chips, 6 FITs
  - Overall failure rate: 5+50*10+50*15+100*6=1855 FITs
- With ASICs
  - Microprocessor (custom) 7 FITs
  - 9 ASICs, 10 FITs
  - 5 SIMMs, 15 FITs
  - Overall failure rate: 7+9*10+5*15=175 FITs

Physical and Logical Faults

Fault level	Physical fault	Logical fault		
		Degradation fault	Open-circuit fault	Short-circuit fault
Chip	Leakage or short between package leads	✓		✓
	Broken, misaligned, or poor wire bonding		✓	
	Surface contamination, moisture	✓		
	Metal migration, stress, peeling		✓	✓
	Metallization (open or short)		✓	✓
Gate	Contact opens		✓	
	Gate to S/D junction short	✓		✓
	Field-oxide parasitic device	✓		✓
	Gate-oxide imperfection, spiking	✓		✓
	Mask misalignment	✓		✓

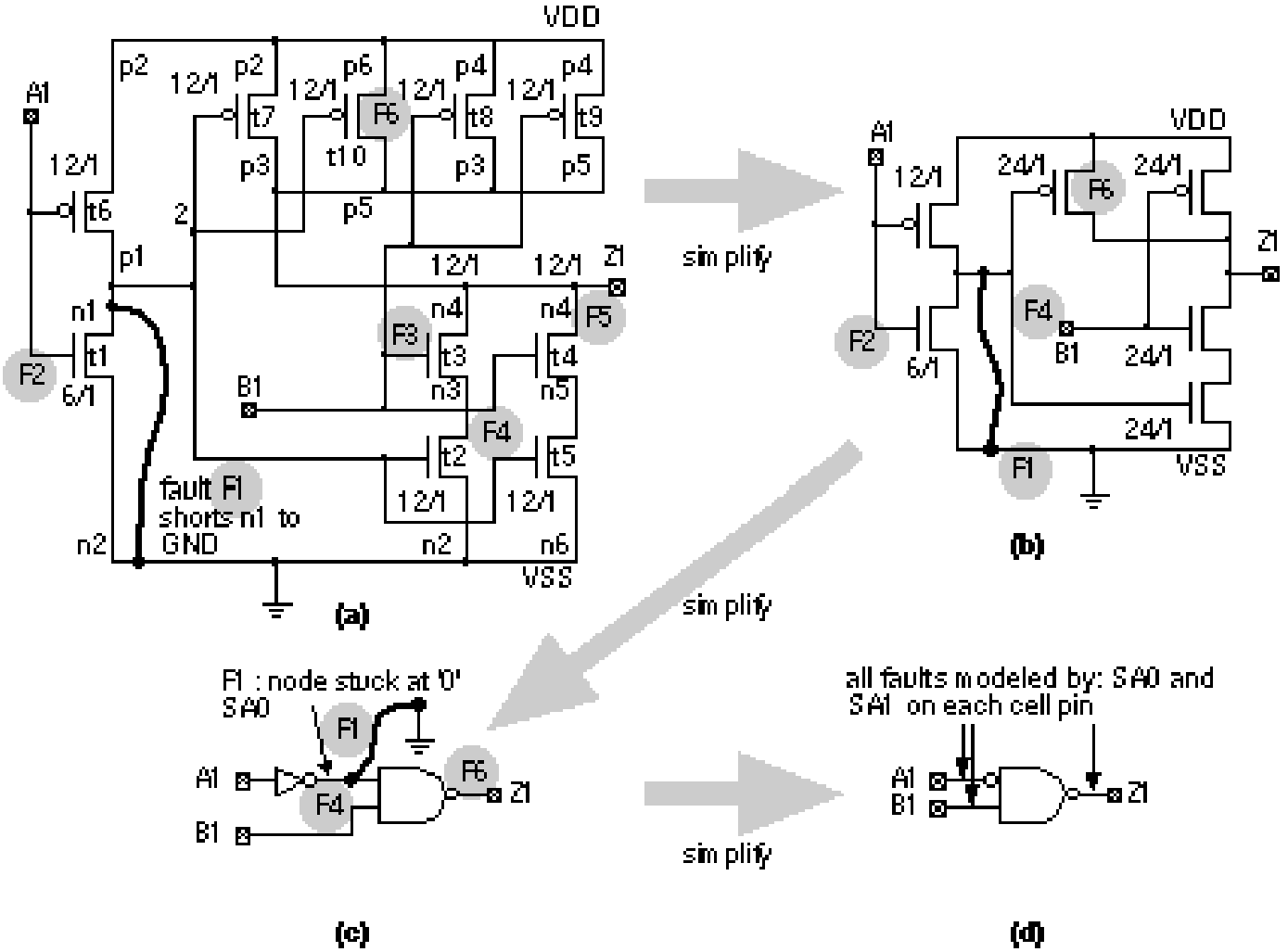
Defects and Physical Faults



Logical Faults

- Single stuck-at fault model
  - Assuming just one fault in a tested logic
  - Two kinds of logical faults
    - stuck-at-0
    - stuck-at-1
- Applied to the pins of logic cells (AND, OR, flip-flop etc.)
- Faults propagate through the logic networks

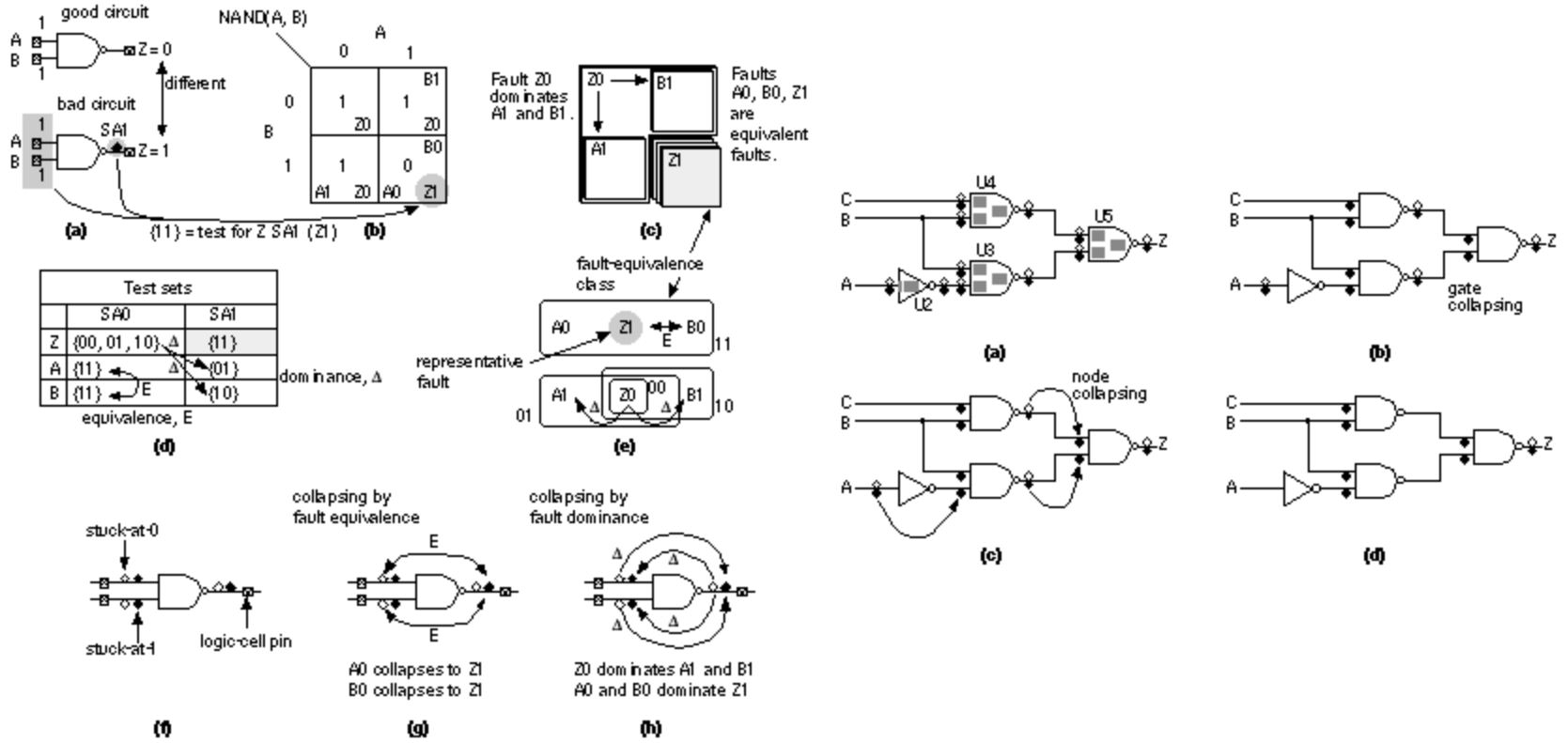
Mapping Physical Faults to Logical Ones



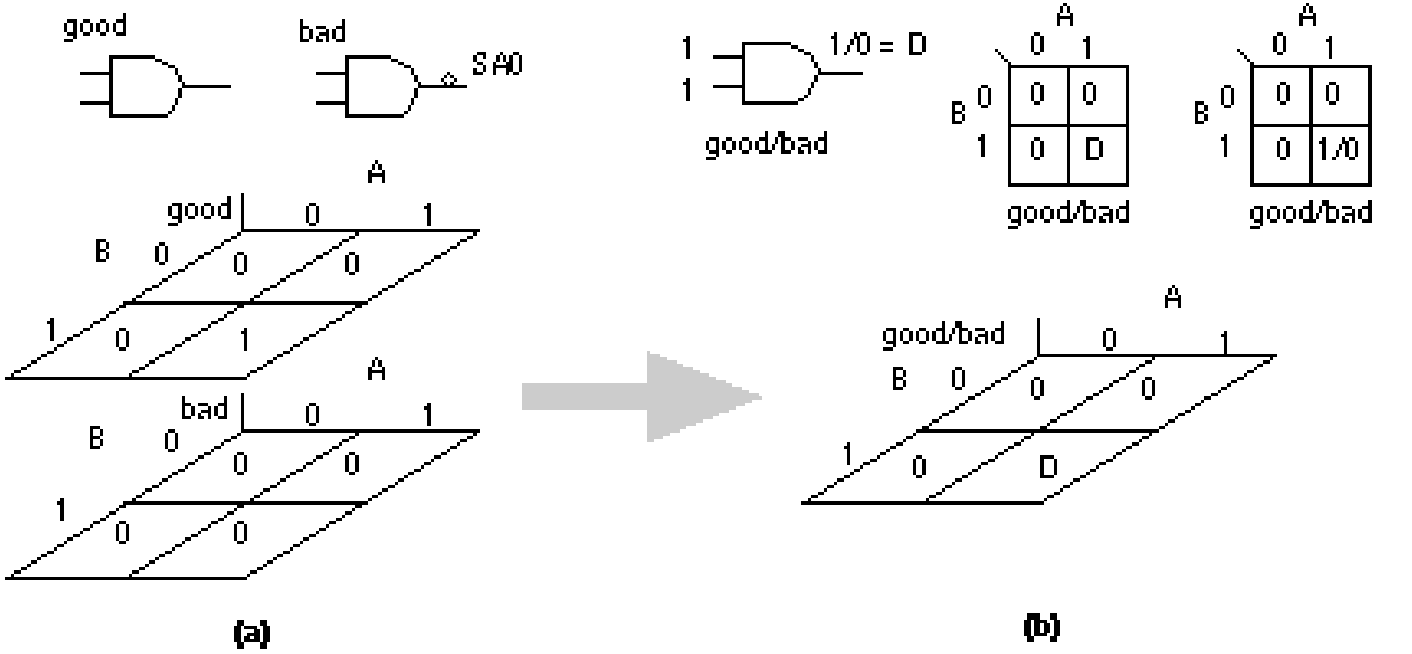
IDDQ Testing

- Test quiescent supply current of the circuit
- Very fast and simple
- Can detect bridging faults

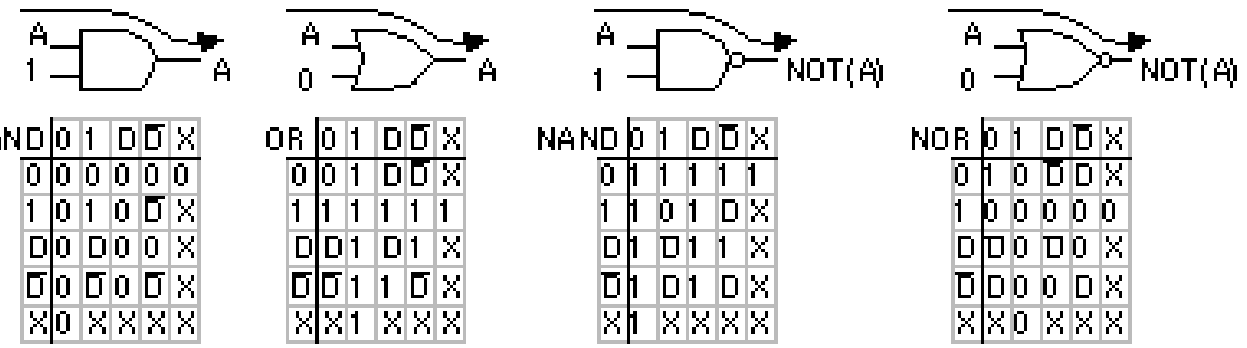
Fault Collapsing



Fault Propagation - D-calculus



(c)



AND	0	1	D	$\bar{D}$	X
0	0	0	0	0	0
1	0	1	0	$\bar{D}$	X
D	0	D	0	0	X
$\bar{D}$	0	$\bar{D}$	0	$\bar{D}$	X
X	0	X	X	X	X

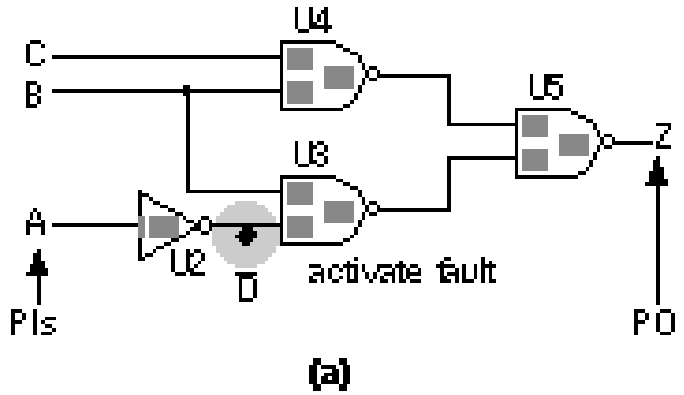
OR	0	1	D	$\bar{D}$	X
0	0	1	D	$\bar{D}$	X
1	1	1	1	1	1
D	D	1	D	1	X
$\bar{D}$	$\bar{D}$	1	1	$\bar{D}$	X
X	X	1	X	X	X

NAND	0	1	D	$\bar{D}$	X
0	1	1	1	1	1
1	1	0	1	D	X
D	1	D	1	1	X
$\bar{D}$	1	D	1	D	X
X	1	X	X	X	X

NOR	0	1	D	$\bar{D}$	X
0	1	0	$\bar{D}$	$\bar{D}$	X
1	0	0	0	0	0
D	$\bar{D}$	0	$\bar{D}$	0	X
$\bar{D}$	D	0	0	D	X
X	X	0	X	X	X

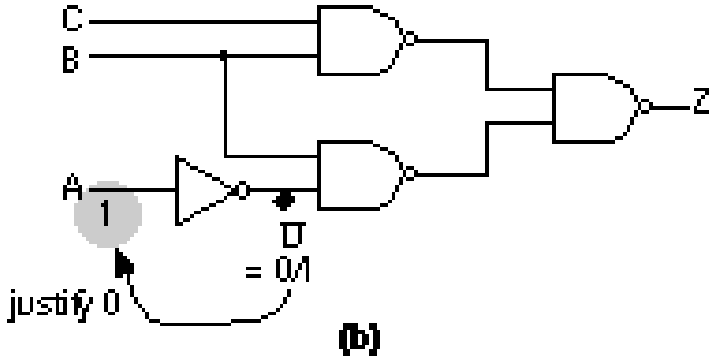
Fault Propagation

1. Choose a fault



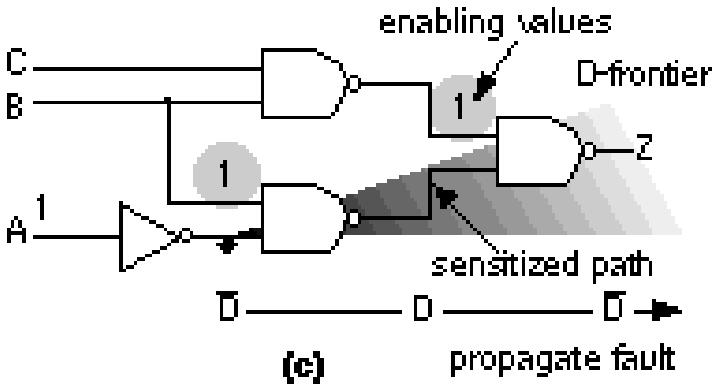
(a)

2. Work backward



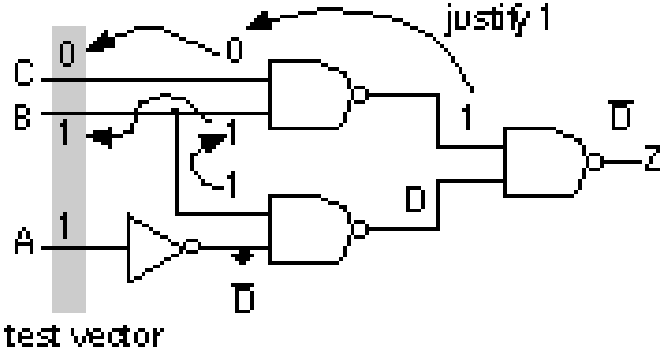
(b)

3. (N)AND gates to 1, (N)OR gates to 0



(c)

4. Work backward

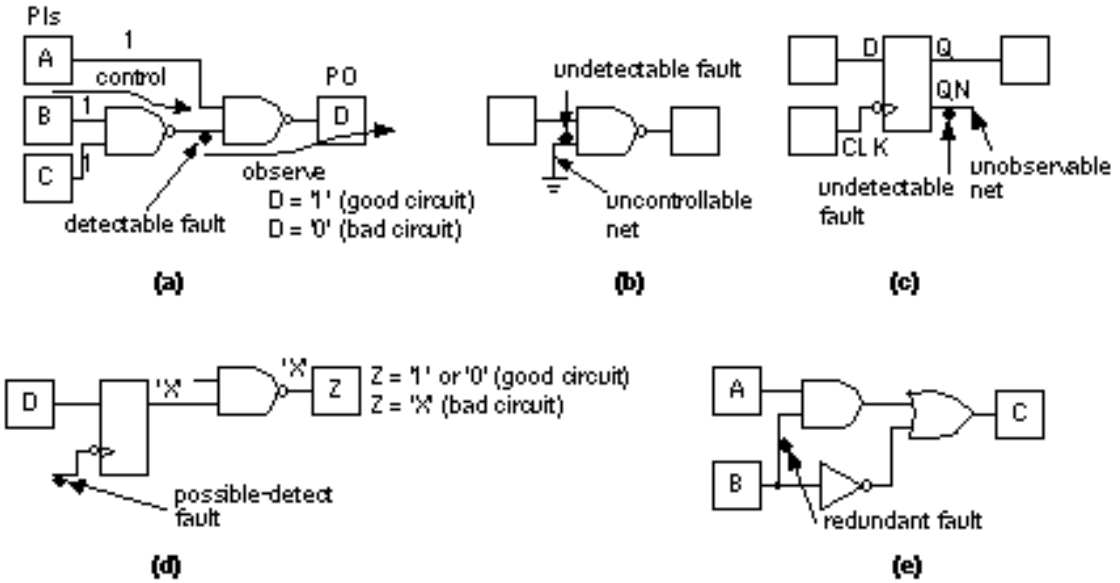


(d)

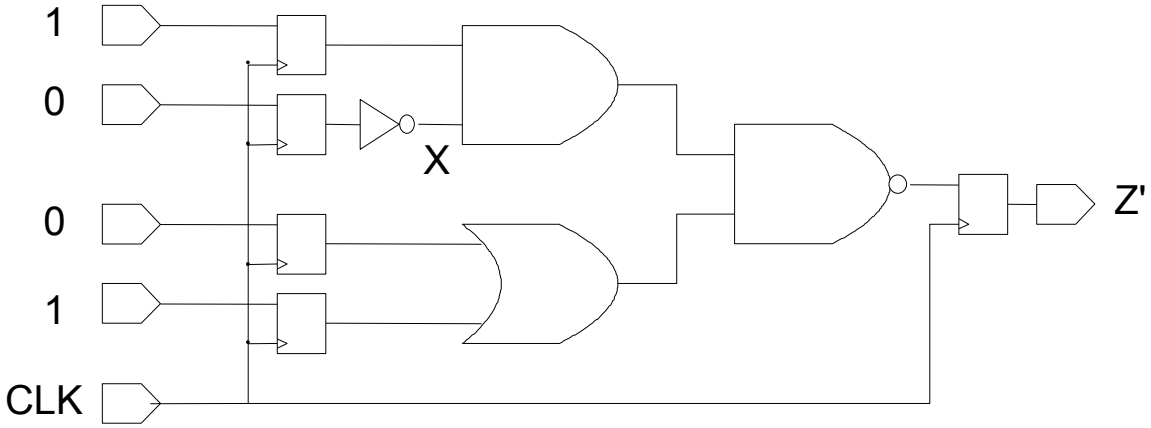
Fault Coverage

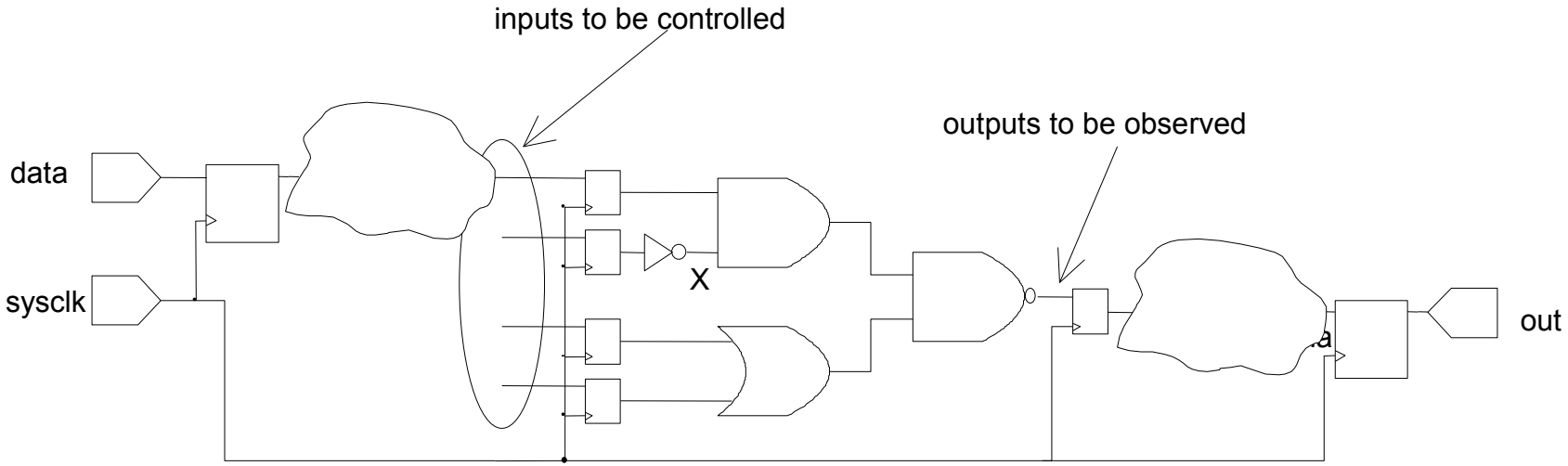
- Testing by applying a set of input vectors and observing output

$$FC = \frac{\text{Number of detected errors}}{\text{Number of detectable errors}}$$

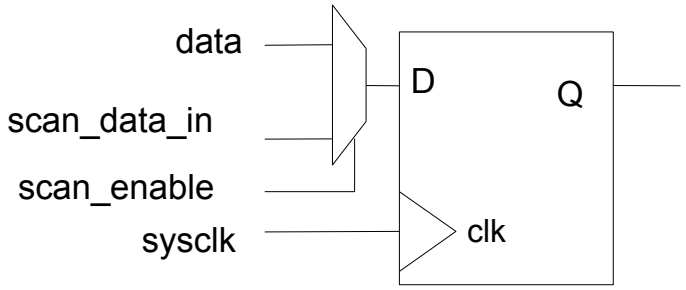


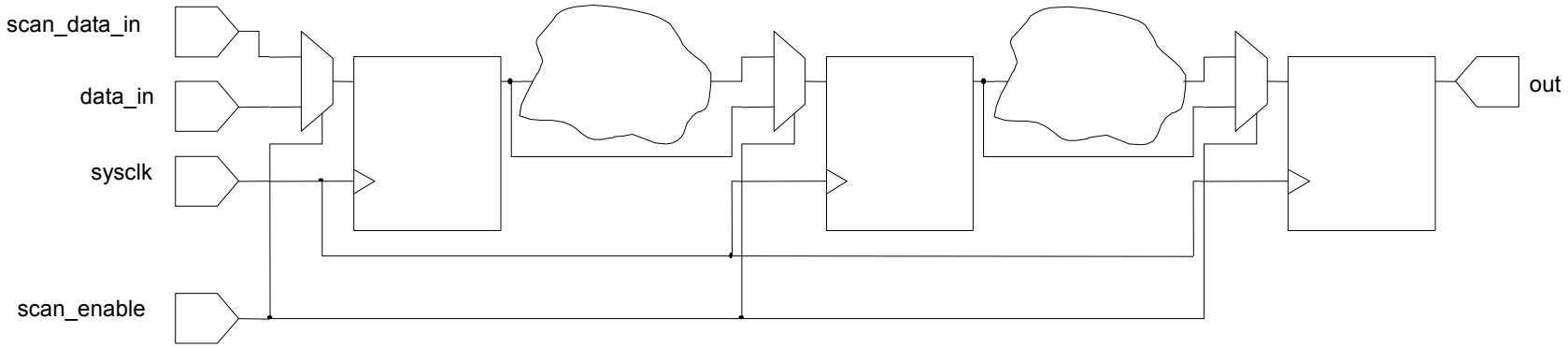
Testing of Sequential Circuits



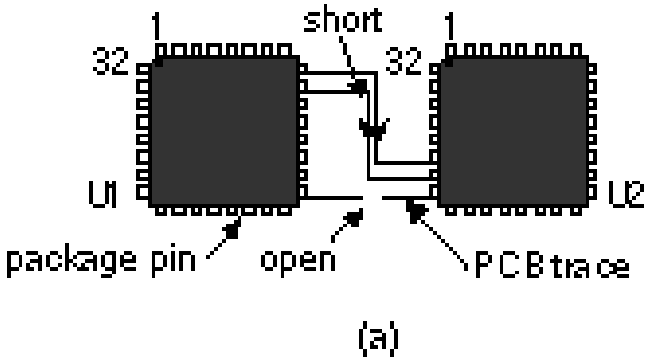


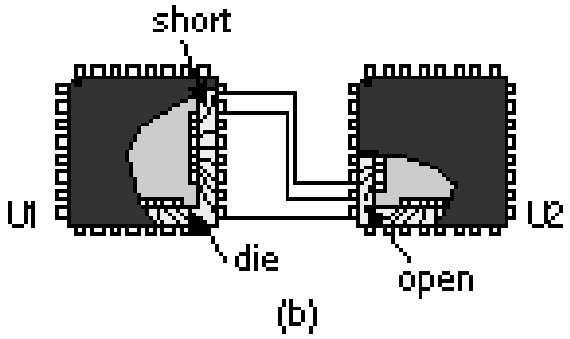
Scan Path

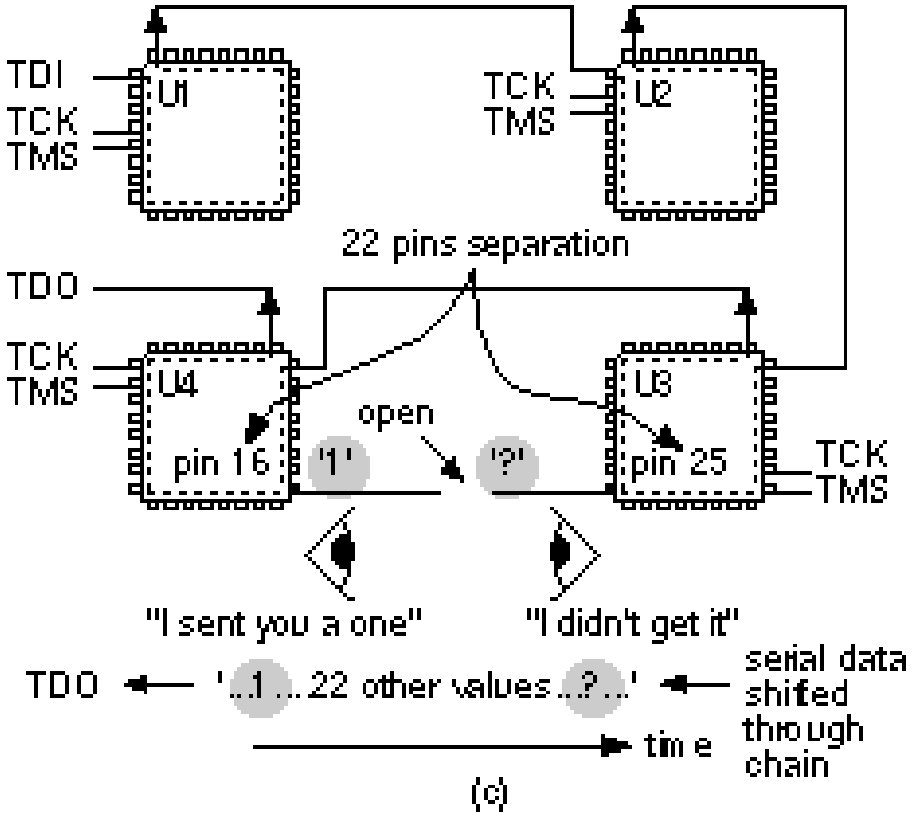

data
scan_data_in
scan_enable
sysclk
D
Q
clk


scan_data_in
data_in
sysclk
scan_enable
out

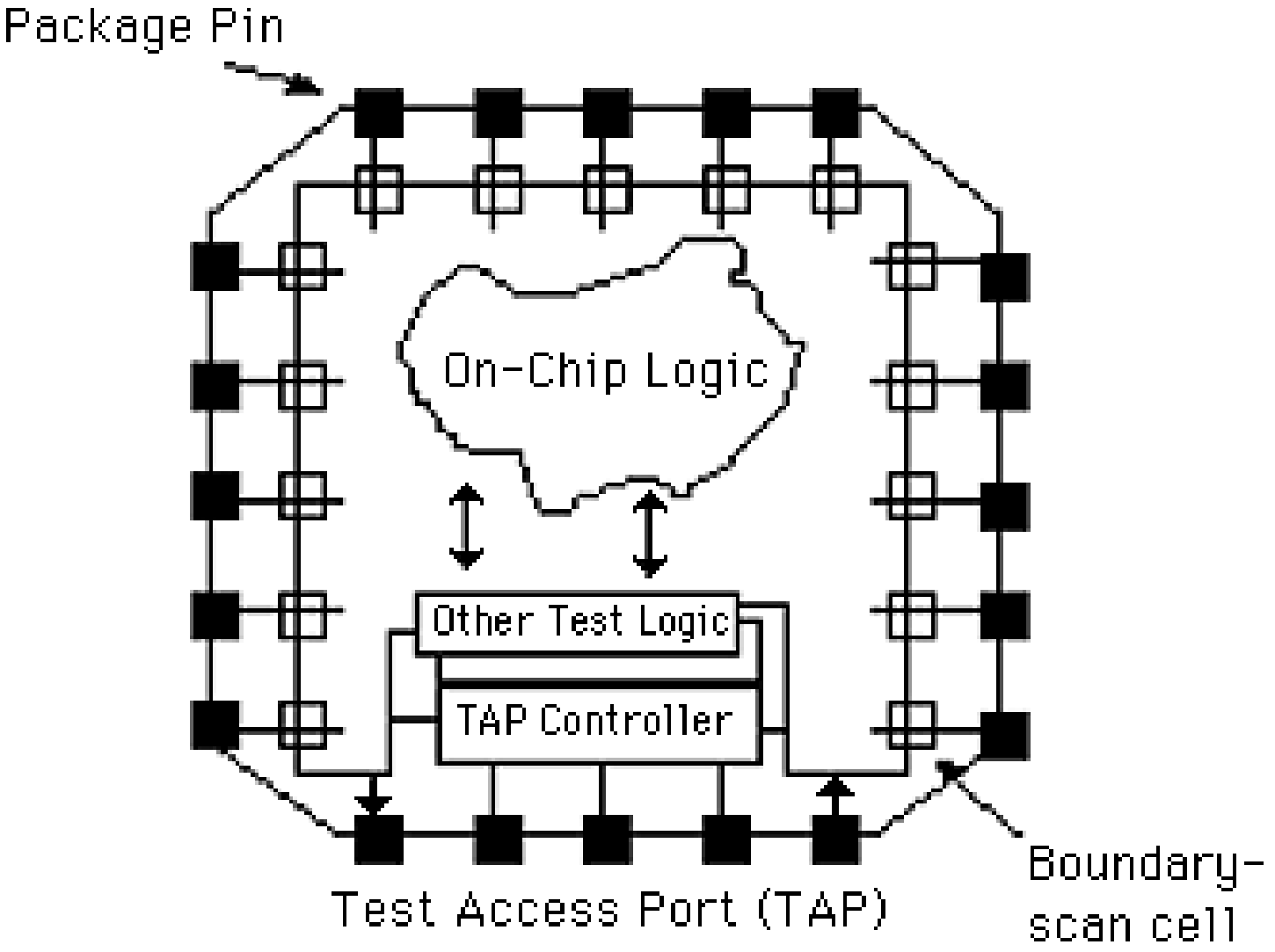
Boundary Scan Test
IEEE Standard 1149.1







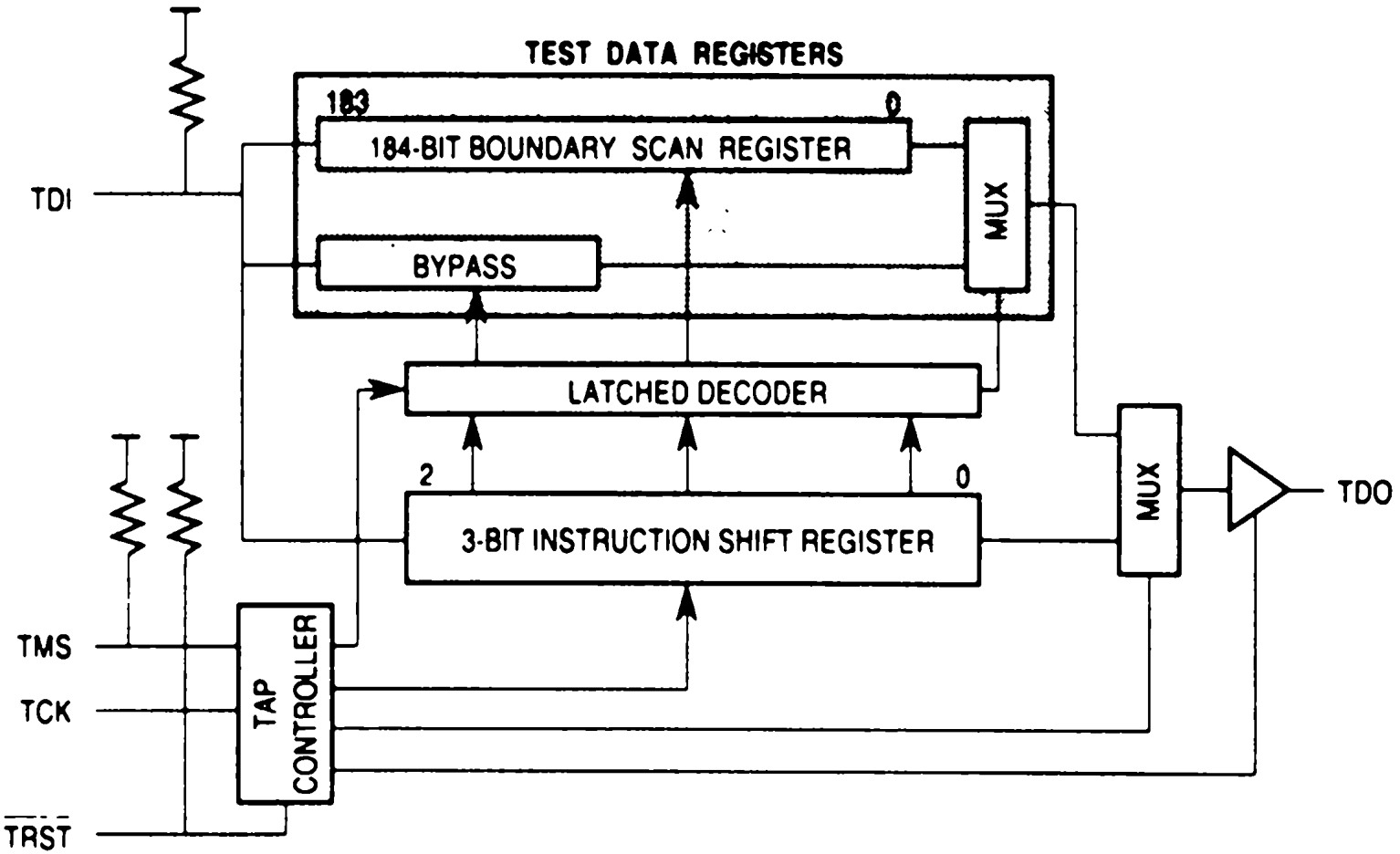
Boundary Scan Test Principle



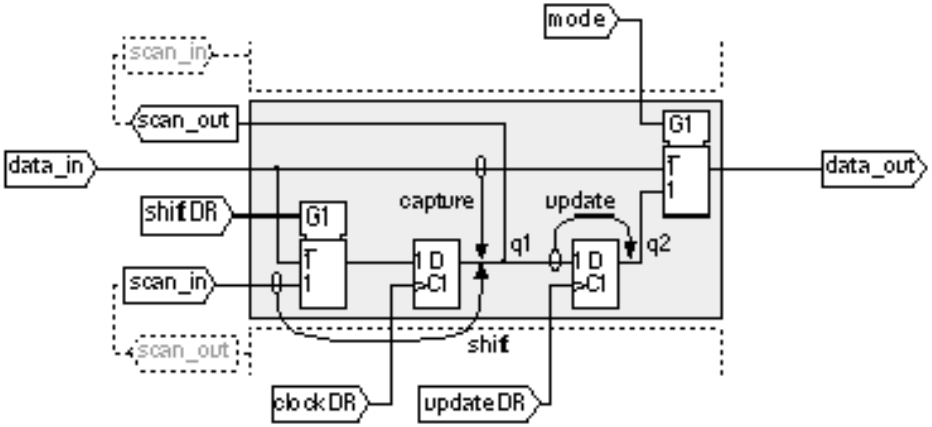
Boundary Scan Test Signals

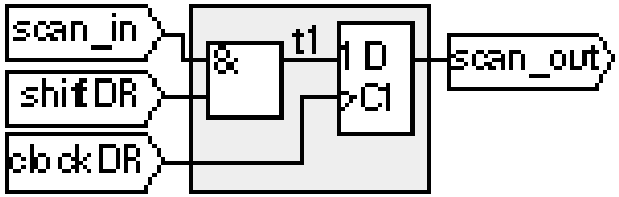
Acronym	Meaning	Explanation
BR	Bypass register	A TDR, directly connects TDI and TDO, bypassing BSR
BSC	Boundary-scan cell	Each I/O pad has a BSC to monitor signals
BSR	Boundary-scan register	A TDR, a shift register formed from a chain of BSCs
BST	Boundary-scan test	Not to be confused with BIST (built-in self-test)
IDCODE	Device-identification register	Optional TDR, contains manufacturer and part number
IR	Instruction register	Holds a BST instruction, provides control signals
JTAG	Joint Test Action Group	The organization that developed boundary scan
TAP	Test-access port	Four- (or five-)wire test interface to an ASIC
TCK	Test clock	A TAP wire, the clock that controls BST operation
TDI	Test-data input	A TAP wire, the input to the IR and TDRs
TDO	Test-data output	A TAP wire, the output from the IR and TDRs
TDR	Test-data register	Group of BST registers: IDCODE, BR, BSR
TMS	Test-mode select	A TAP wire, together with TCK controls the BST state
TRST* or nTRST	Test-reset input signal	Optional TAP wire, resets the TAP controller (active-low)

Boundary Scan Test Example (MC 68040)

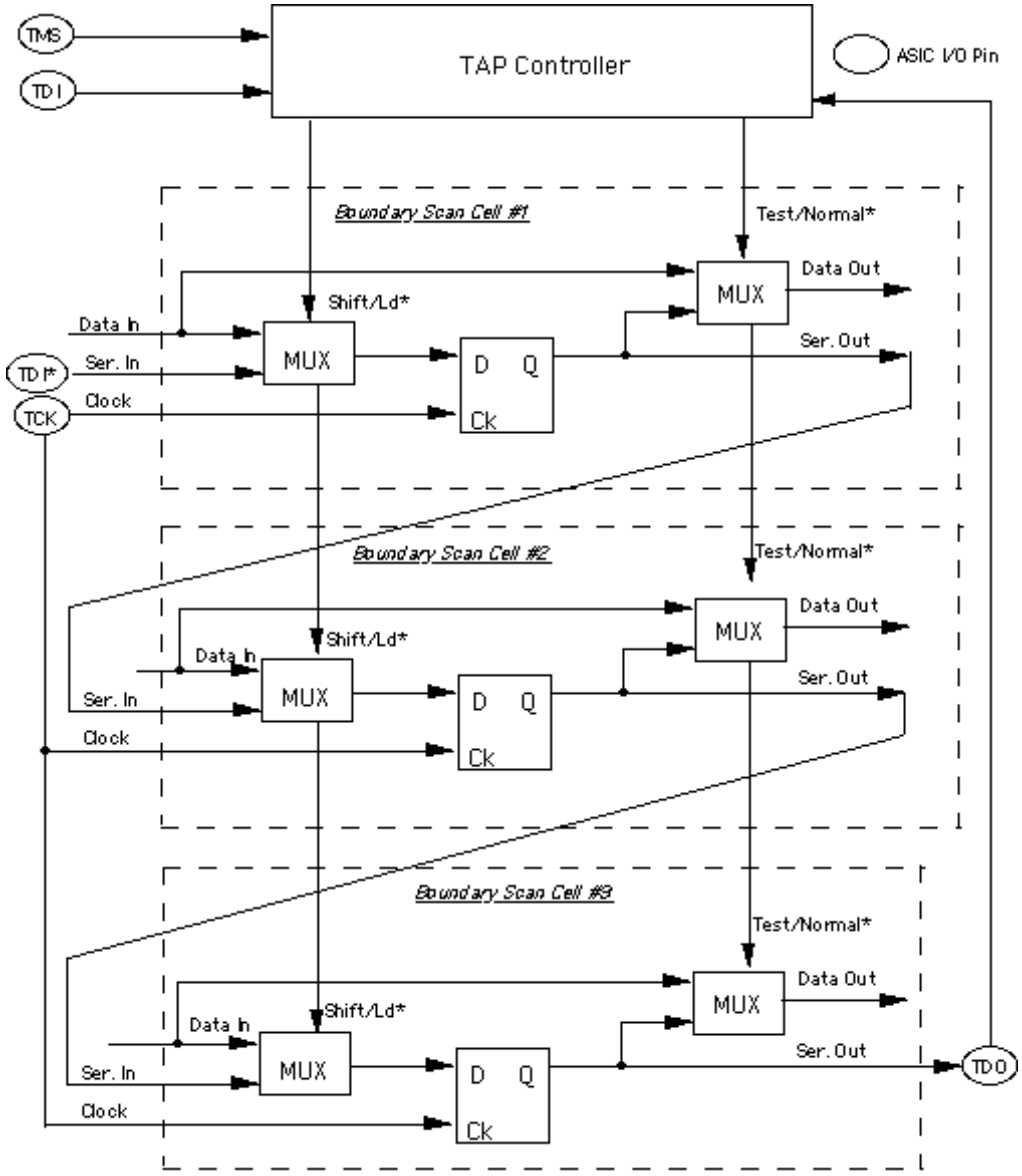


Boundary Scan Test
DR and BR Cells

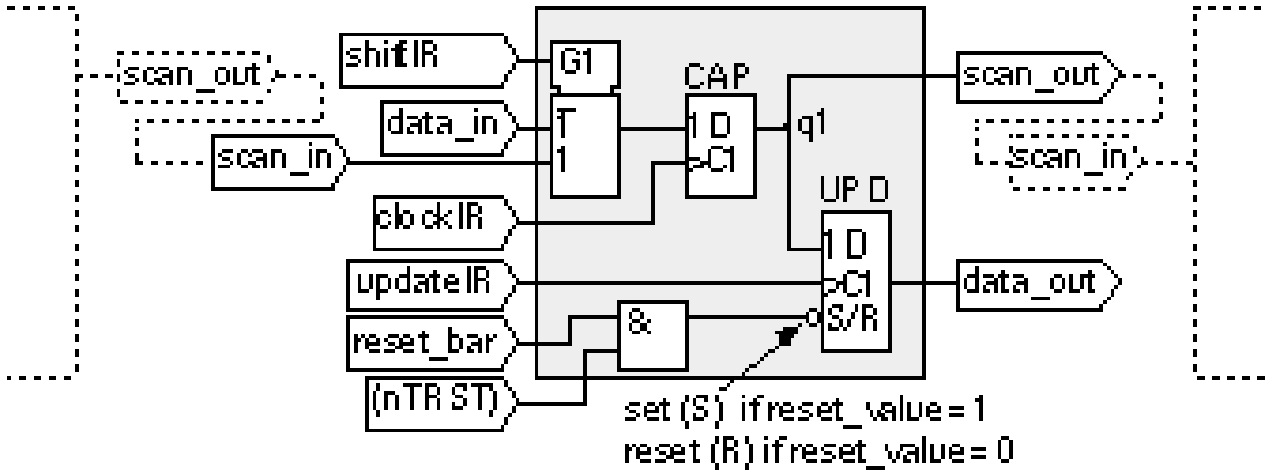




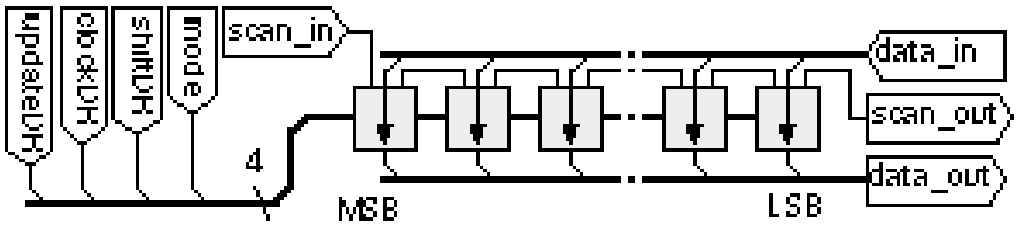
Boundary Scan Register

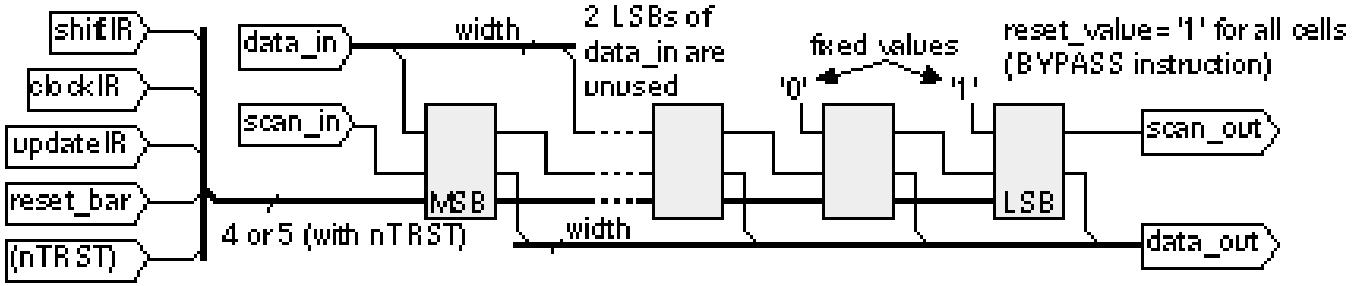


Boundary Scan Test
IR Cell

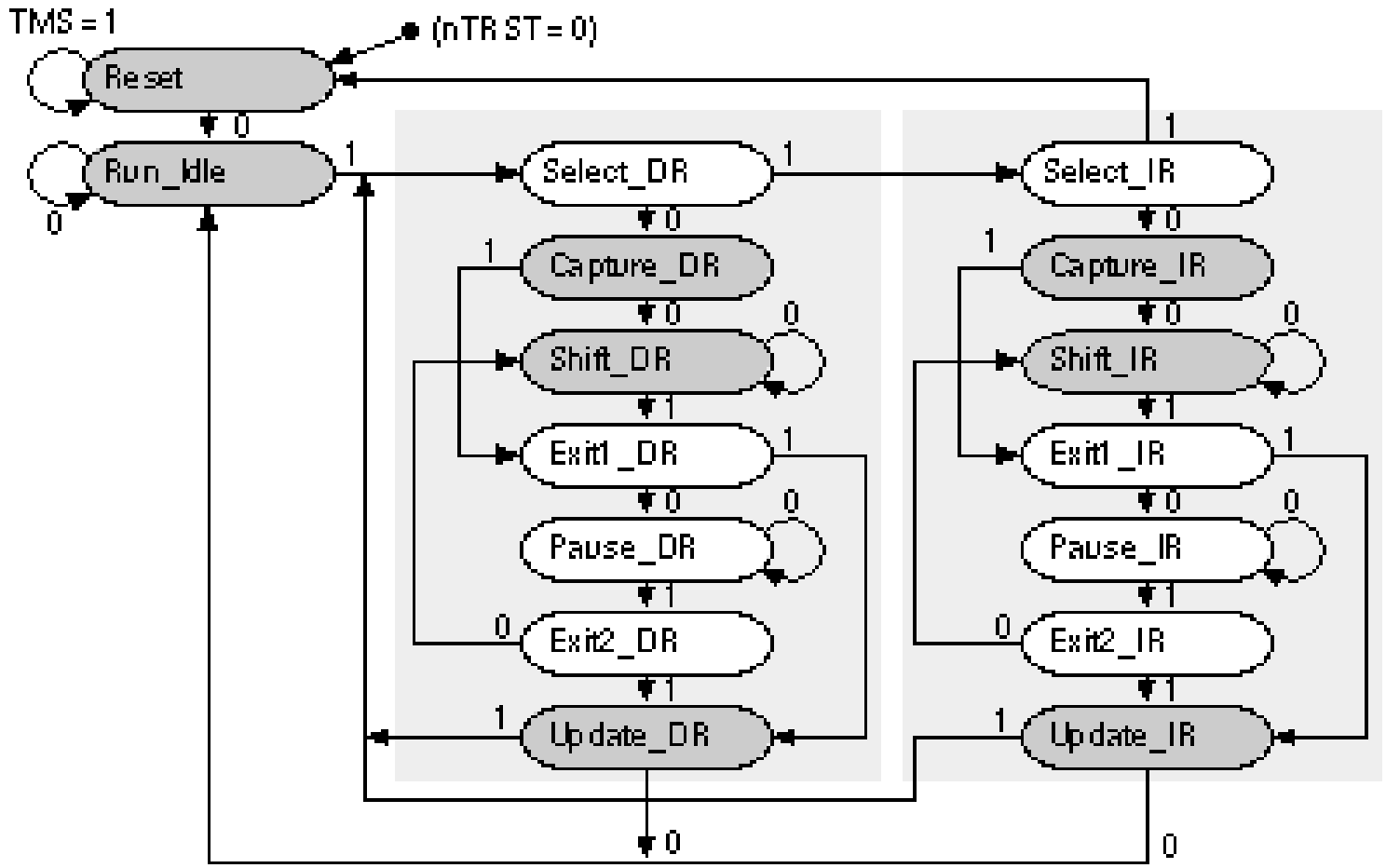


Boundary Scan Test
BSR and IR





Boundary Scan Test
TAP Controller State Diagram



MC 68040
BST Instructions

Bit 2	Bit 1	Bit 0	Instructlon Selected	Test Data Register Accessed
0	0	0	EXTEST	Boundary Scan
0	0	1	HI-Z	Bypass
0	1	0	SAMPLE/PRELOAD	Boundary Scan
0	1	1	DRVCTL.T	Boundary Scan
1	0	0	SHUTDOWN	Bypass
1	0	1	PRIVATE	Bypass
1	1	0	DRVCTL.S	Boundary Scan
1	1	1	BYPASS	Bypass

Benefits and Penalties of Boundary-Scan

- Benefits:
  - lower test generation costs
  - reduced test time
  - reduced time to market
  - simpler and less costly testers
  - compatibility with tester interfaces
  - high-density packaging devices accommodation
- Penalties
  - extra silicon due to boundary scan circuitry
  - added pins
  - additional design effort
  - degradation in performance due to gate delays through the additional circuitry
  - increased power consumption

Gate requirements for a Gate Array

Boundary-scan Design

10000 gate design in a 40-pin package

Logic Element	Gate Equivalent
Variable Size	
Boundary-scan Register (40 cells)	680 approx.
Fixed Sizes	
TAP Controller	131
Instruction Register (2 bits)	28
Bypass Register	9
Miscellaneous Logic	20 approx.
TOTAL	**868 approx.**