### Logical Effort Fast Simplified Method of Delay Calculation in CMOS Circuits

# Gate Delay

Relative and absolute delay:

### $d_{abs} = d\tau$

 $\tau$  - delay of an inverter loaded with the same inverter witout a parasitic delay

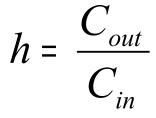
#### d=f+p

p - parasitic delay, independent of gate scaling and loadf - *stage effort*, load-dependent delay

### Stage effort

f=gh

g- *logical effort* h- *electrical effort* 



#### logical effort for different gates:

Gate type	Number of inputs						
	1	2	3	4	5	n	
Inverter	1						
NAND		4/3	5/3	6/3	7/3	(n+2)/3	
NOR		5/3	7/3	9/3	11/3	(2n+1)/3	
Multiplekser		2	2	2	2	2	
XOR		4	12	32			

### Gate Delay

d=gh+p

Gate type	Typical parasitic delay
inverter	p <sub>inv</sub>
n-input NAND	np <sub>inv</sub>
n-input NOR	np <sub>inv</sub>
n-input multiplexer	2np <sub>inv</sub>
XOR, XNOR	4p <sub>inv</sub>

Typically p<sub>inv</sub>=1.0

### Multistage Logical Networks

Path logical effort G

# $G = \prod g_i$

Path Electrical effort

$$H = \frac{C_{out}}{C_{in}}$$

## Branching effort

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}} = \frac{C_{total}}{C_{useful}}$$

 $B = \prod b_i$ 

## Path Delay

F = GBH

$$BH = \frac{C_{out}}{C_{in}} \prod b_i = \prod h_i$$
$$D = \sum p_i + \sum g_i h_i$$

# Optimal Stage Effort

$$\hat{f} = g_i h_i = F^{1/N}$$

$$\hat{D} = NF^{1/N} + P$$

### Design of a Gate Chain

#### Starting from the end of the chain:

$$h_i = \frac{F^{1/N}}{g_i}$$

$$C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$$

### **Optimum Number of Stages**

	Path effort	Optimum number of	Minimum delay	Stage effort
P <sub>inv</sub> =1.0	0	stages	1.0	
	5.00	1	<u> </u>	0-5.8
	5,83	2 3	6.8	2.4-4.7
	22.3		11.4	2.8-4.4
	82.2		16.0	2.0-4.4
	300	4	20.7	3.0-4.2
		5		3.1-4.1
	1090	6	25.3	3.2-4.0
	3920		29.8	
	14200	7	34.4	3.3-3.9
		8		3.3-3.9
	51000	9	39.0	3.3-3.9
	184000	•	43.6	