Logical Effort

Fast Simplified Method of Delay Calculation in CMOS Circuits

Gate Delay

Relative and absolute delay:

$$d_{abs}=d\tau$$

τ - delay of an inverter loaded with the same inverter witout a parasitic delay

$$d=f+p$$

p - parasitic delay, independent of gate scaling and load

f - *stage effort*, load-dependent delay

Stage effort

$$f = gh$$

g- *logical effort*

h- *electrical effort*

$$h = \frac{C_{out}}{C_{in}}$$

logical effort for different gates:

Gate type	Number of inputs					
	1	2	3	4	5	n
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n+2)/3
NOR		5/3	7/3	9/3	11/3	(2n+1)/3
Multiplekser		2	2	2	2	2
XOR		4	12	32		

Gate Delay

$$d = gh + p$$

Gate type	Typical parasitic delay
inverter	p_{inv}
n-input NAND	np_{inv}
n-input NOR	np_{inv}
n-input multiplexer	$2np_{inv}$
XOR, XNOR	$4p_{inv}$

Typically $p_{inv} = 1.0$

Multistage Logical Networks

Path logical effort G

$$G = \prod g_i$$

Path Electrical effort

$$H = \frac{C_{out}}{C_{in}}$$

Branching effort

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}} = \frac{C_{total}}{C_{useful}}$$

$$B = \prod b_i$$

Path Delay

$$F = GBH$$

$$BH = \frac{C_{out}}{C_{in}} \prod b_i = \prod h_i$$

$$D = \sum p_i + \sum g_i h_i$$

Optimal *Stage Effort*

$$\hat{f} = g_i h_i = F^{1/N}$$

$$\hat{D} = NF^{1/N} + P$$

Design of a Gate Chain

Starting from the end of the chain:

$$h_i = \frac{F^{1/N}}{g_i}$$

$$C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$$

Optimum Number of Stages

$P_{inv}=1.0$

Path effort	Optimum number of stages	Minimum delay	*Stage effort*
0		1.0	
	1		0-5.8
5,83		6.8	
	2		2.4-4.7
22.3		11.4	
	3		2.8-4.4
82.2		16.0	
	4		3.0-4.2
300		20.7	
	5		3.1-4.1
1090		25.3	
	6		3.2-4.0
3920		29.8	
	7		3.3-3.9
14200		34.4	
	8		3.3-3.9
51000		39.0	
	9		3.3-3.9
184000		43.6	