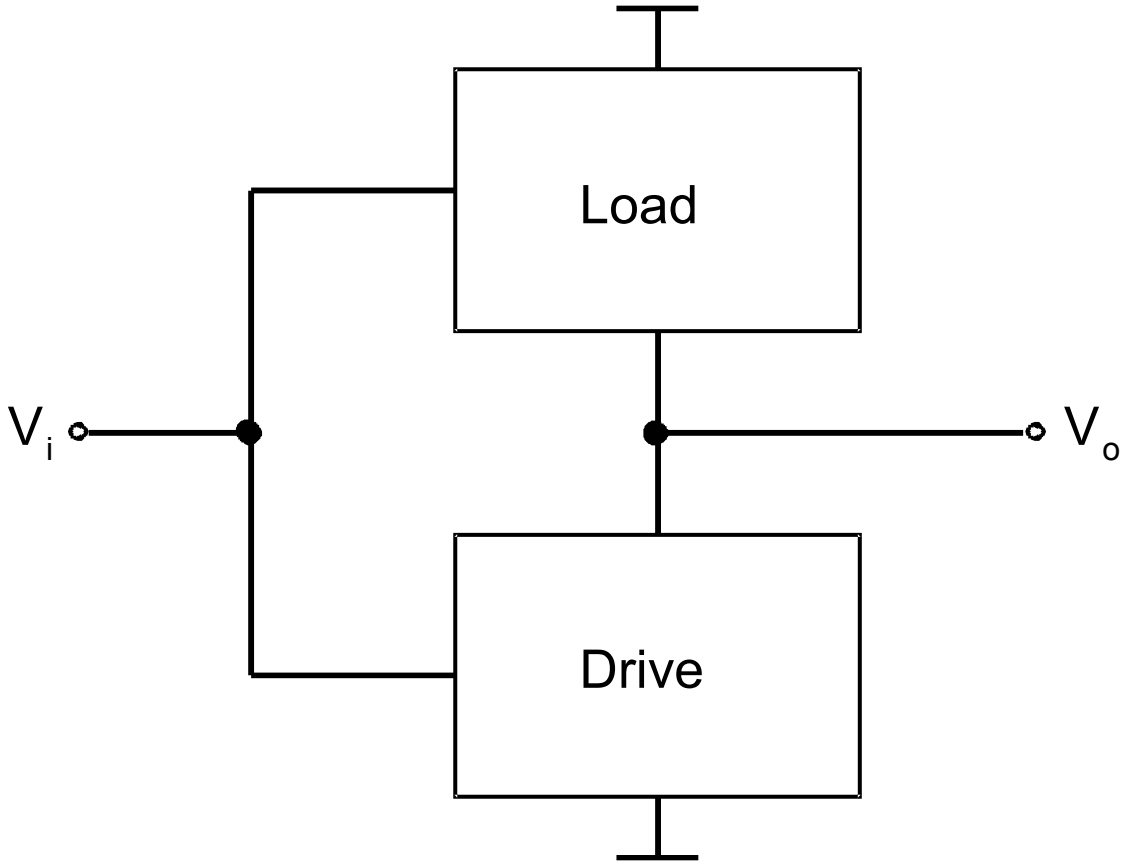
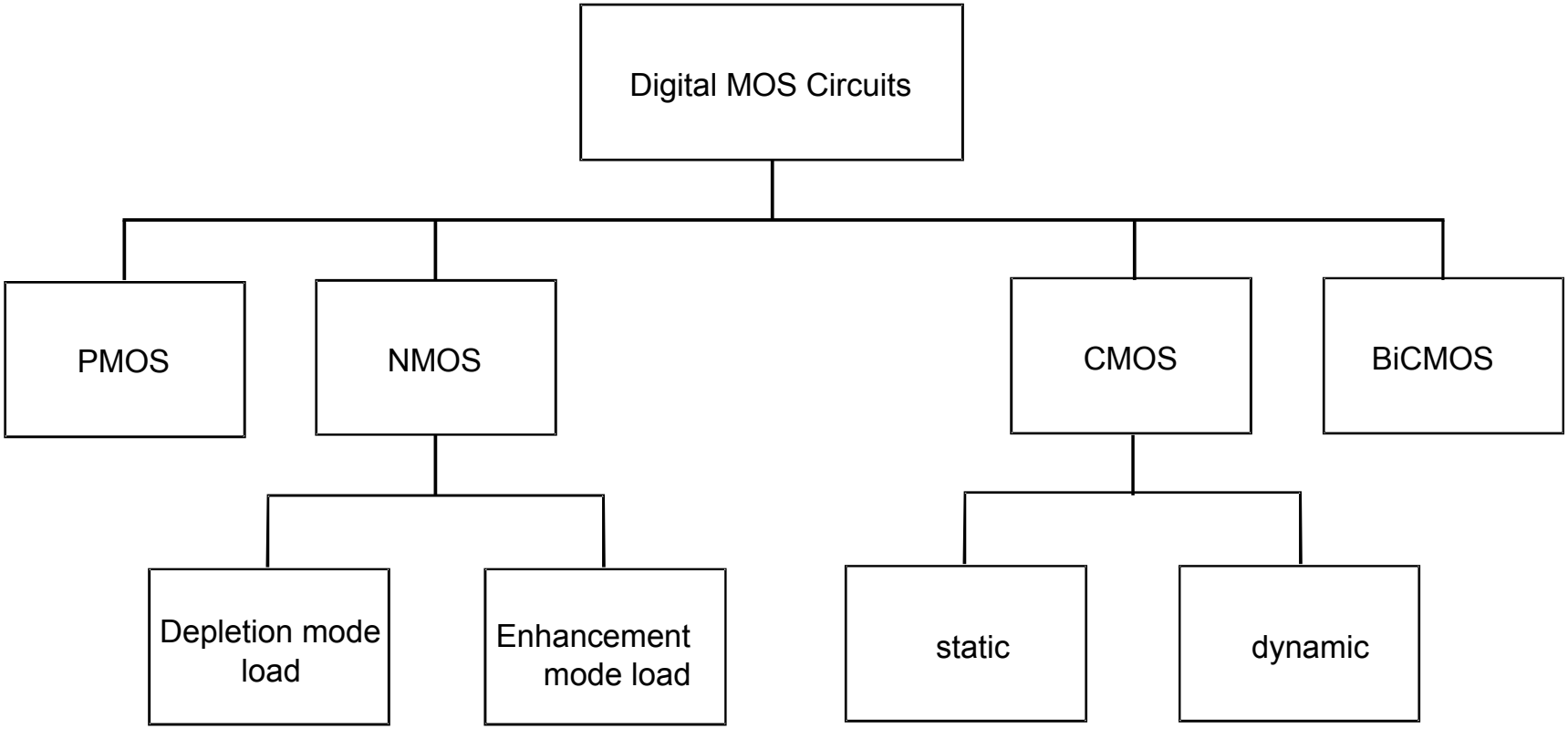
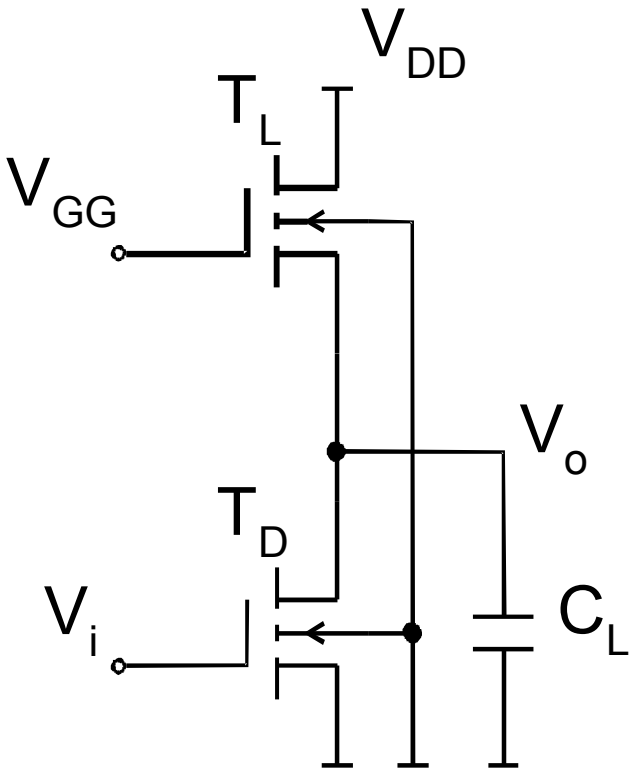
General Structure of MOS Inverter



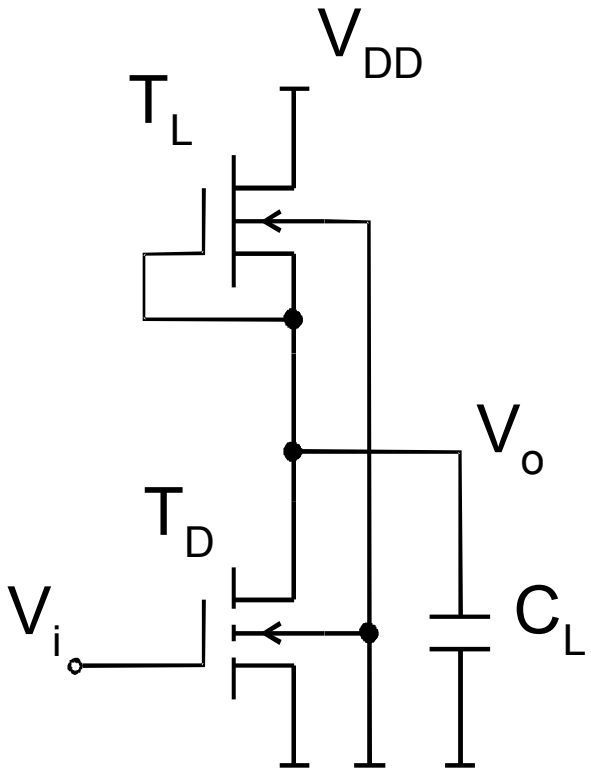
Digital MOS Circuits Families



NMOS Gates

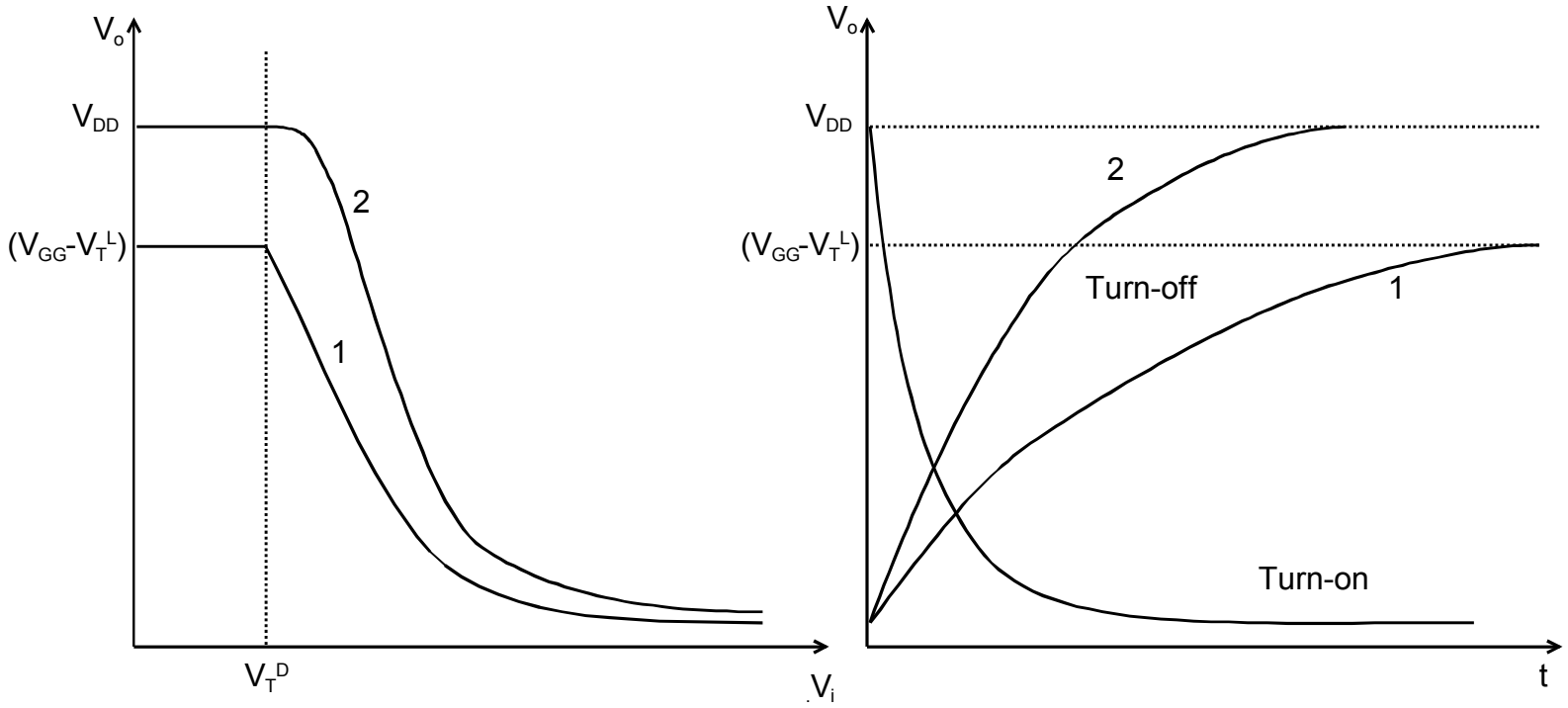


With enhancement mode load



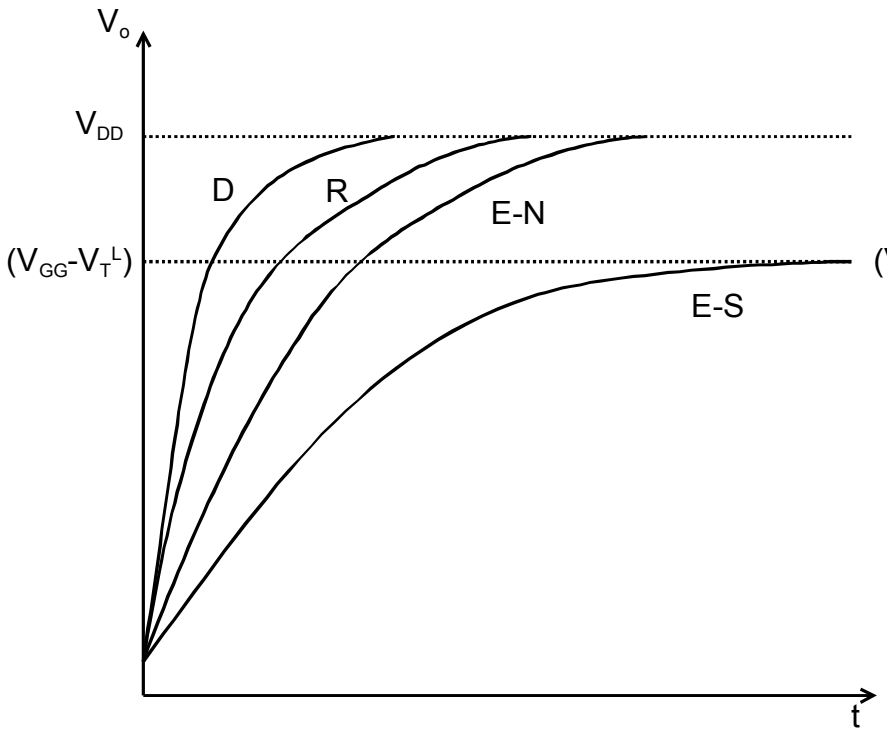
With depletion mode load

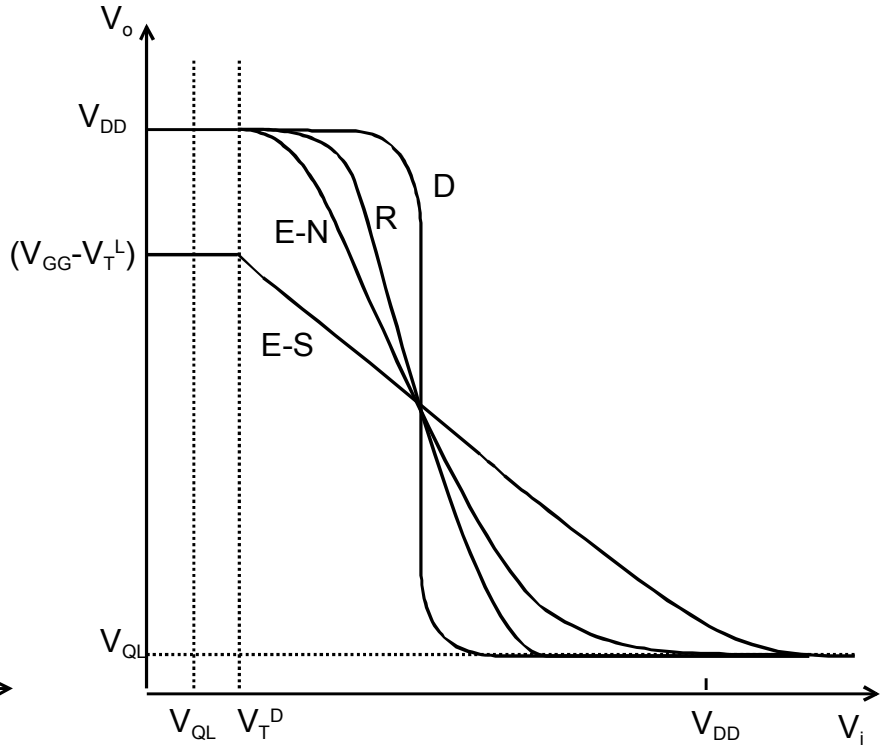
NMOS Gates with Enhancement Mode Load



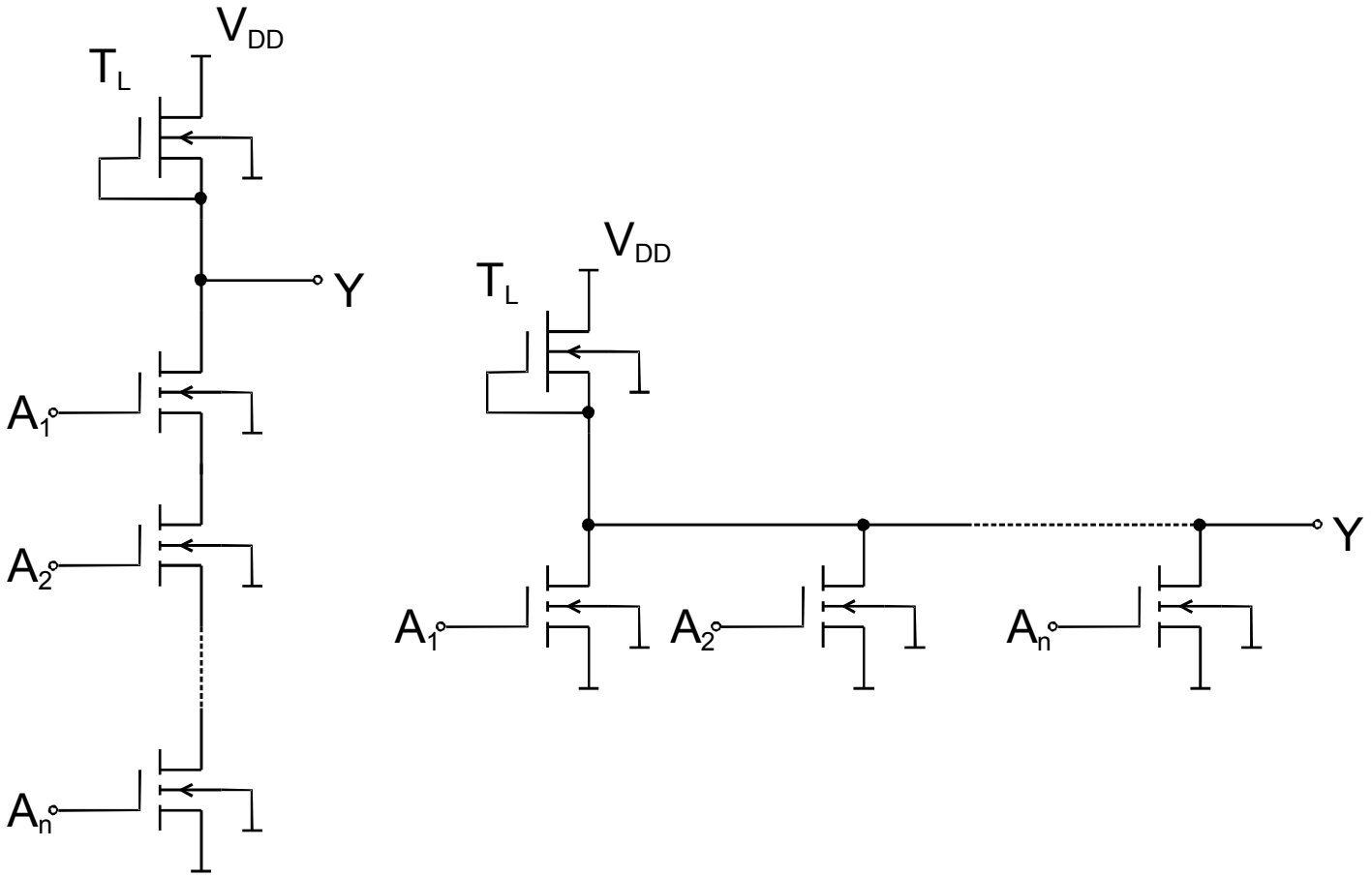
1. VGG<VDD+VTL - load transistor operates in saturation range
2. VGG≥VDD+VTL - load transistor operates in non-saturation range

Comparison of NMOS Gates

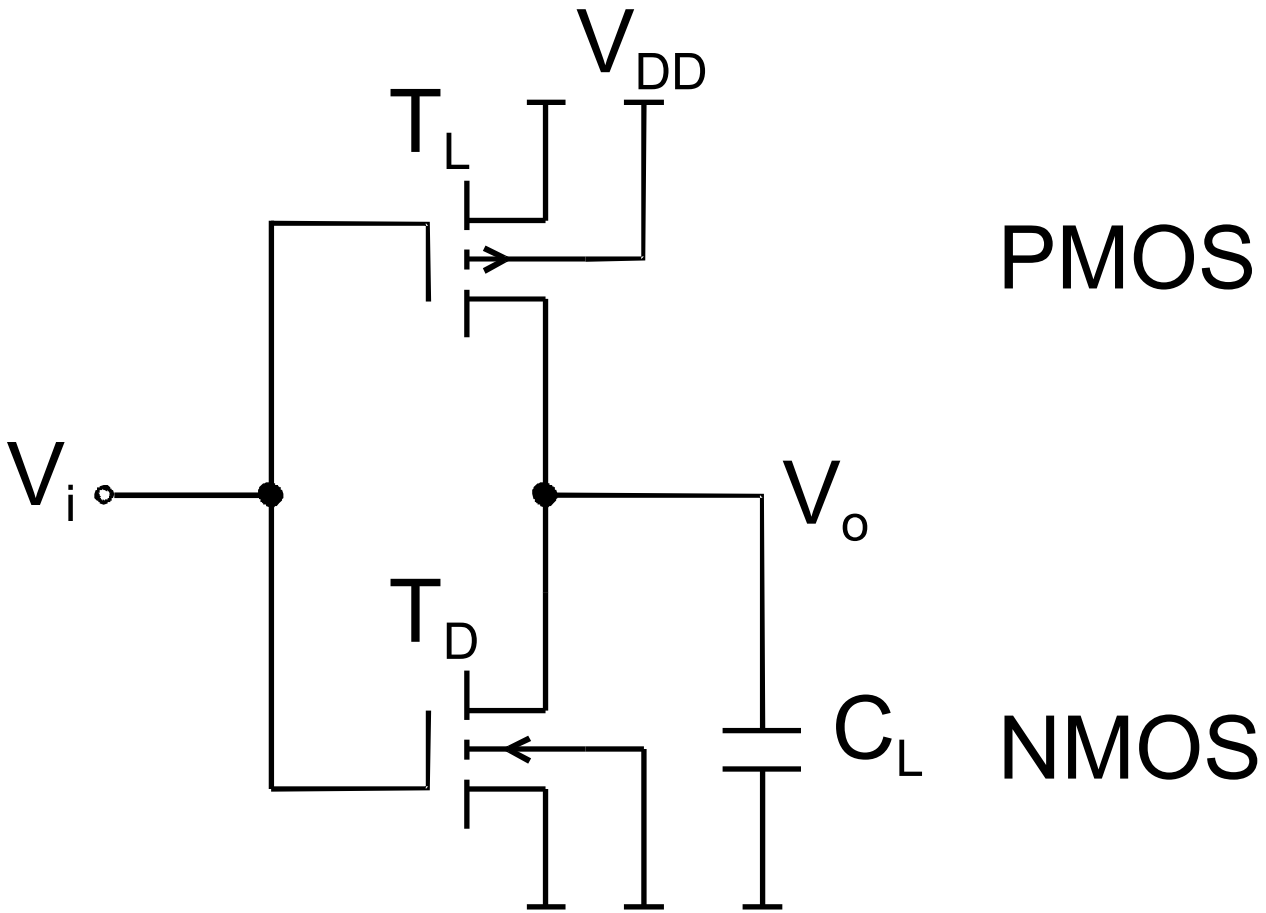




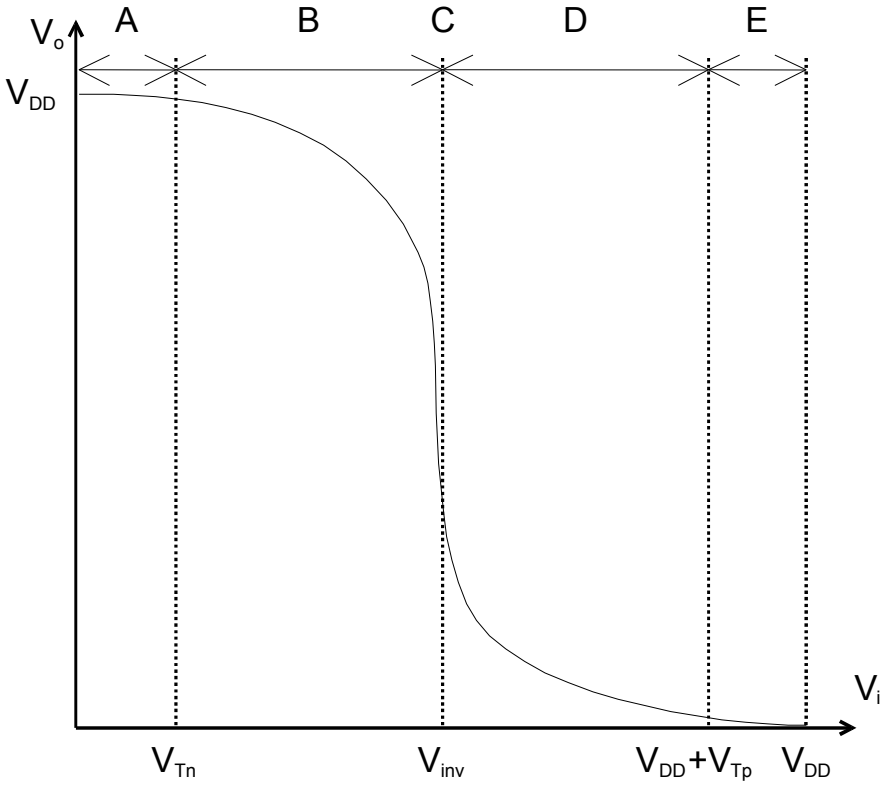
NMOS Gates
- NAND and NOR

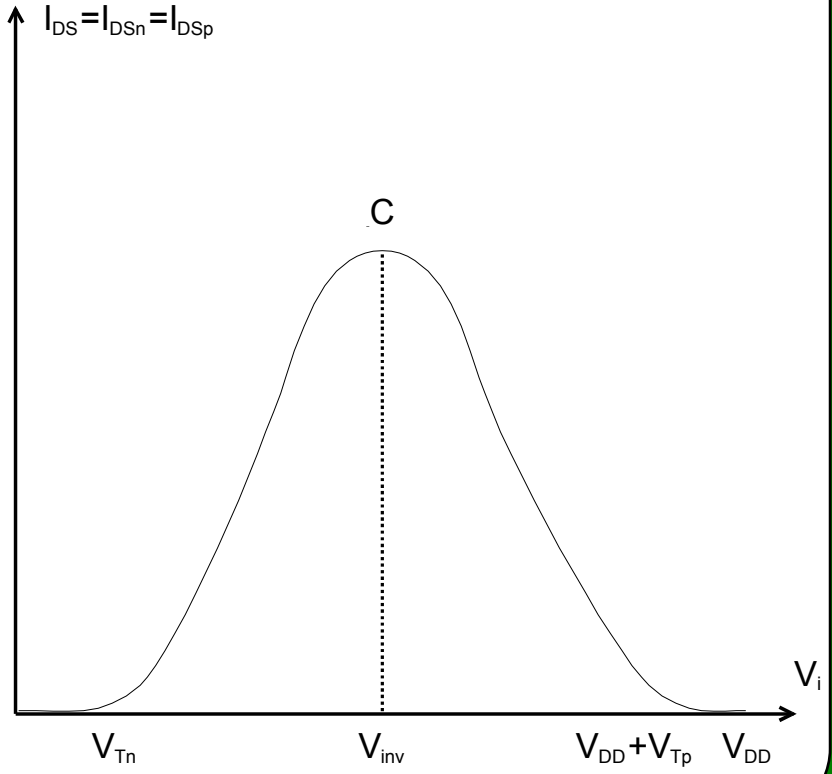


CMOS Inverter

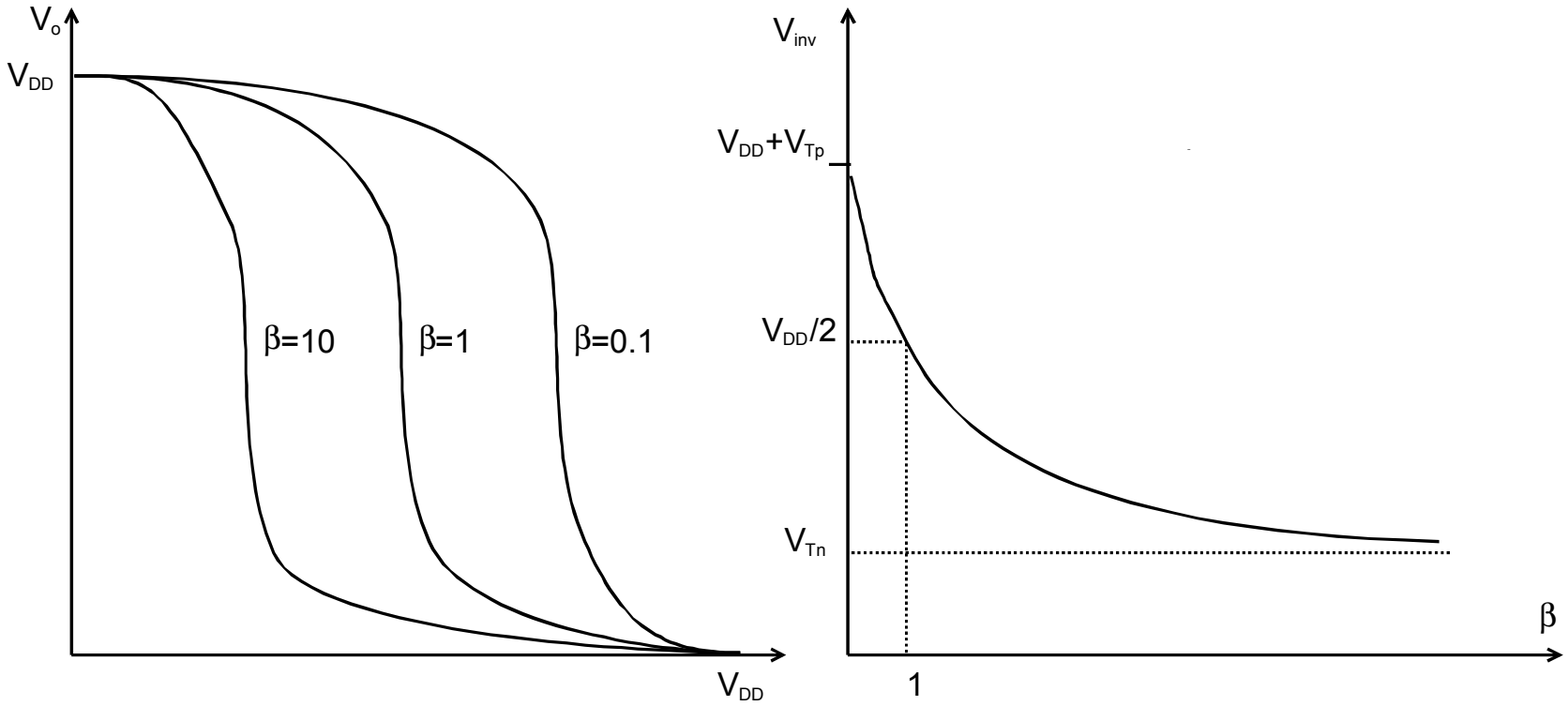


CMOS Inverter Characteristics

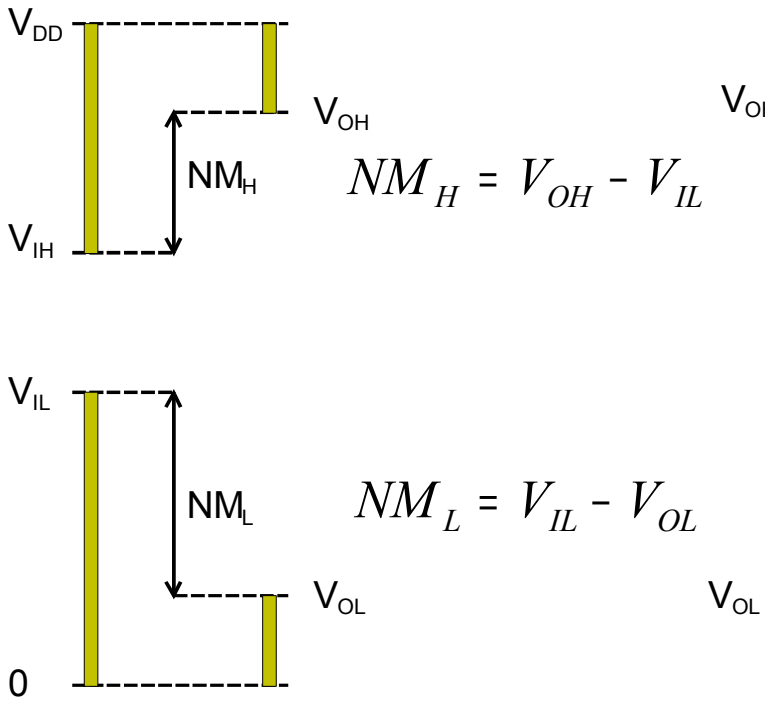




Influence of β on Transfer Characteristic of CMOS Inverter

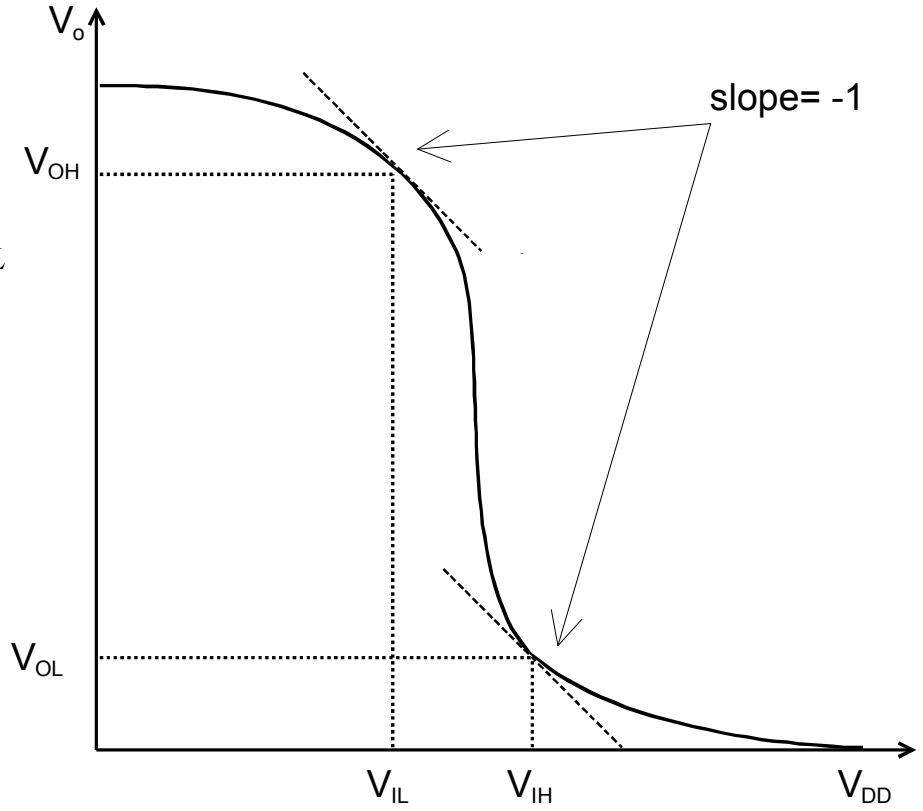


Definition of Noise Margin

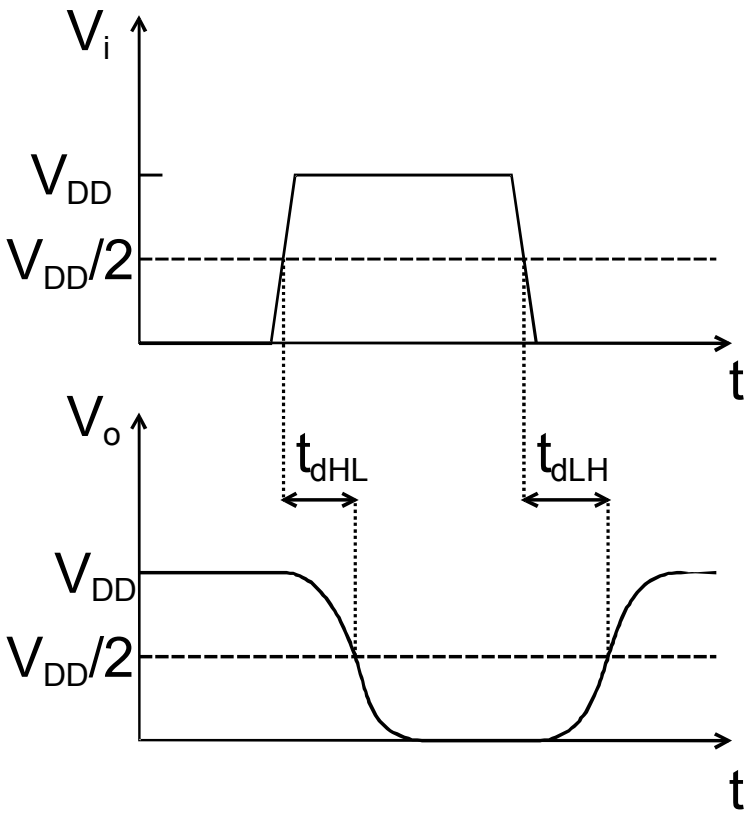


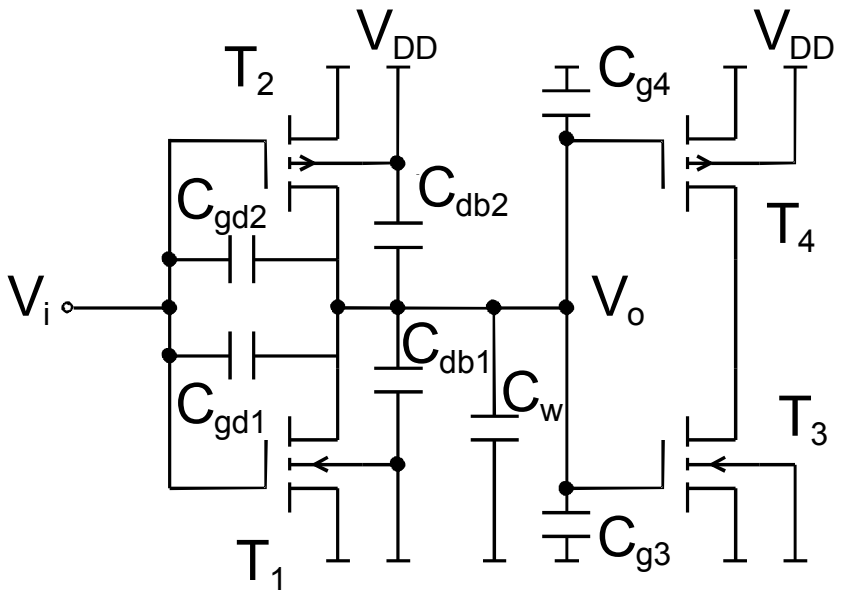
$$NM_H = V_{OH} - V_{IL}$$

$$NM_L = V_{IL} - V_{OL}$$

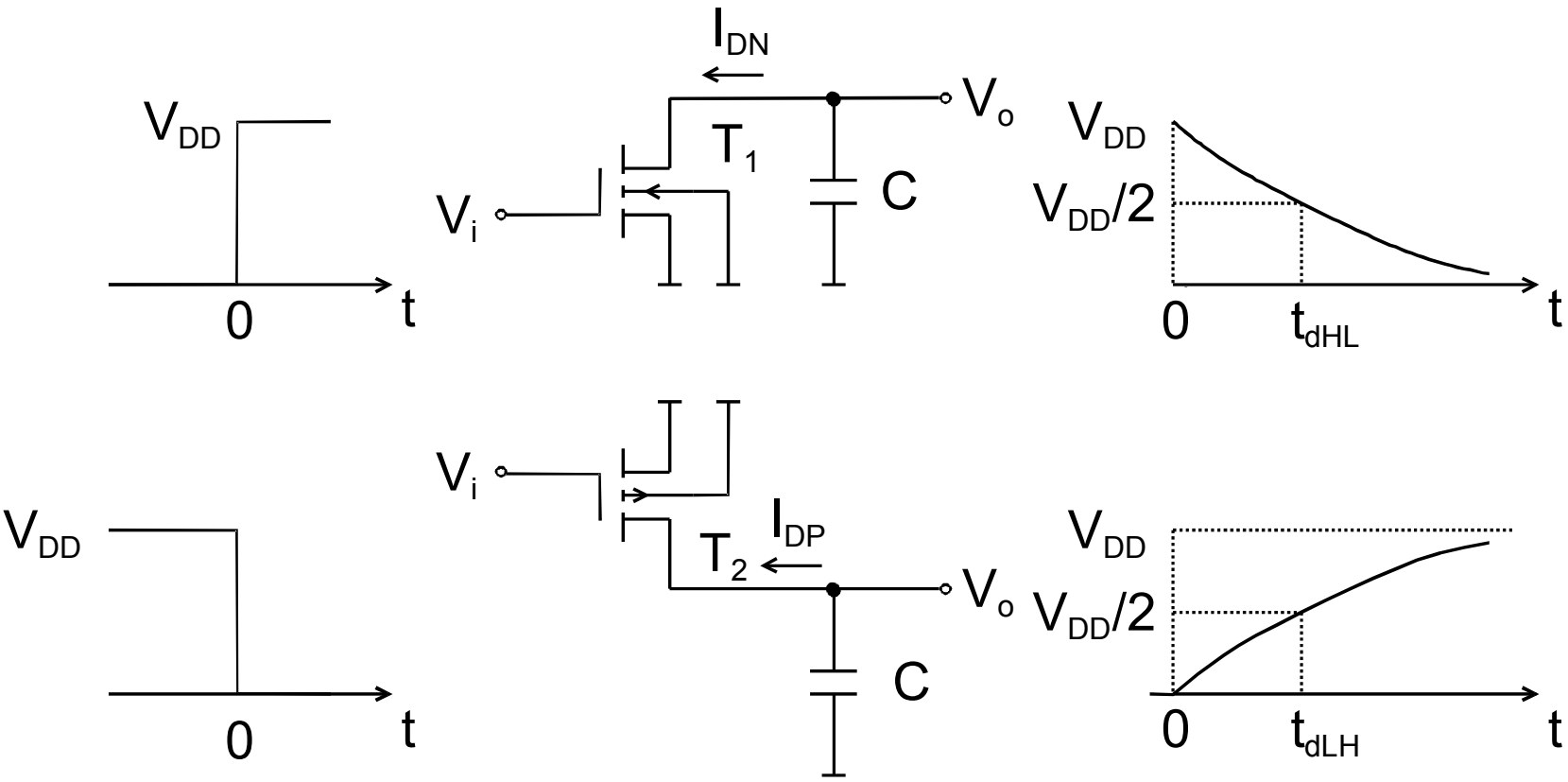


CMOS Inverter Delay

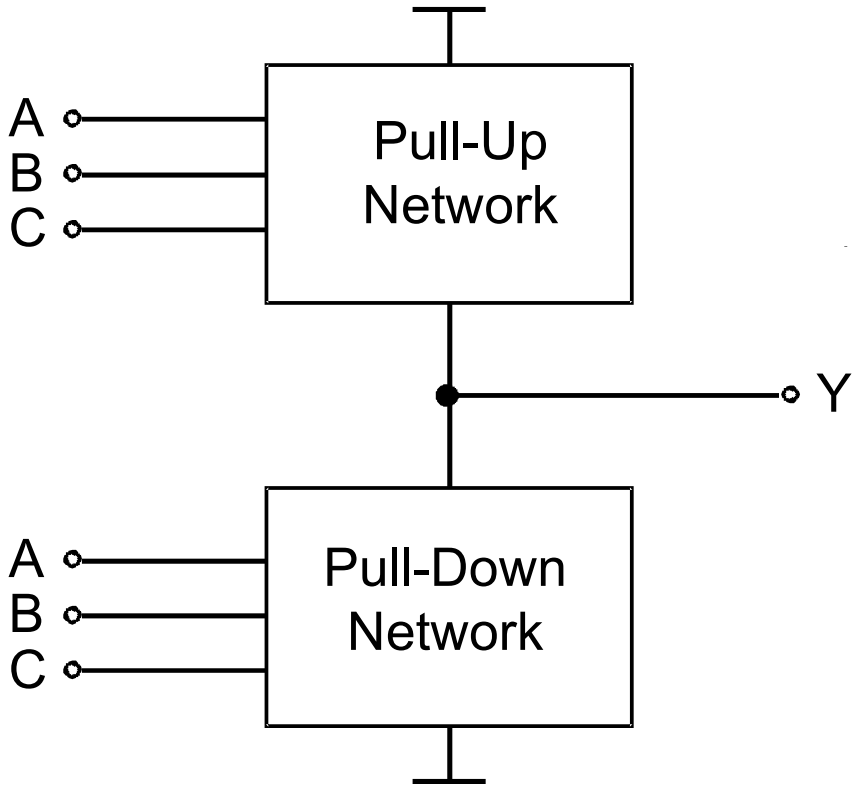




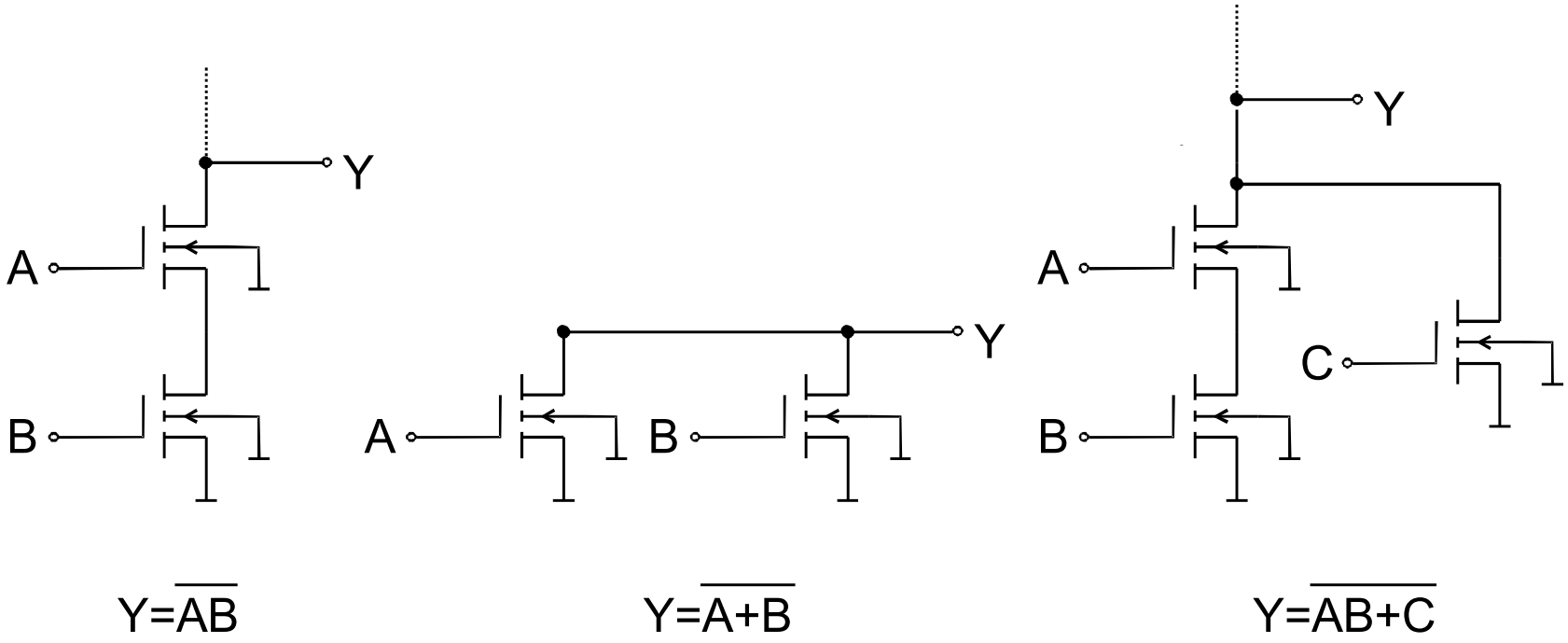
Calculation of t_{dHL} and t_{dLH}



General Structure of CMOS Gate

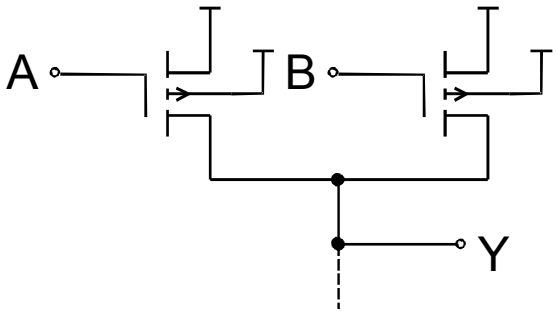


CMOS Pull-Down Networks

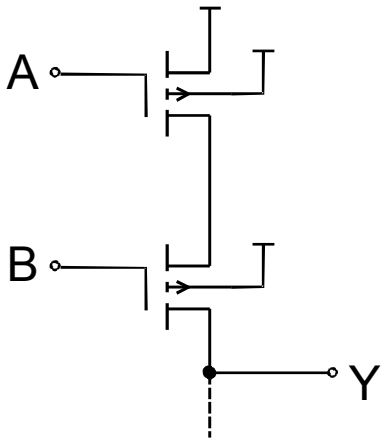


$Y=\overline{AB}$ $Y=\overline{A+B}$ $Y=\overline{AB+C}$

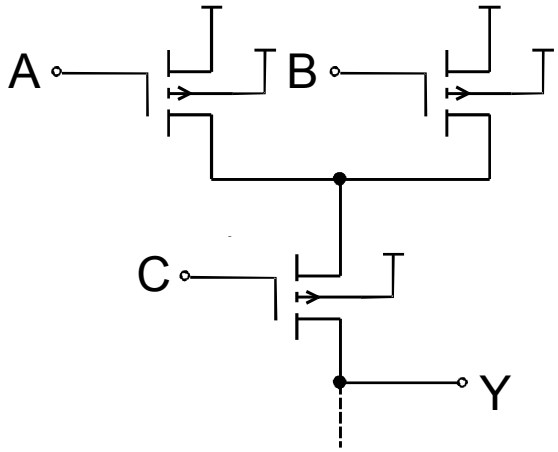
CMOS Pull-Up Networks



$Y=\overline{AB}$

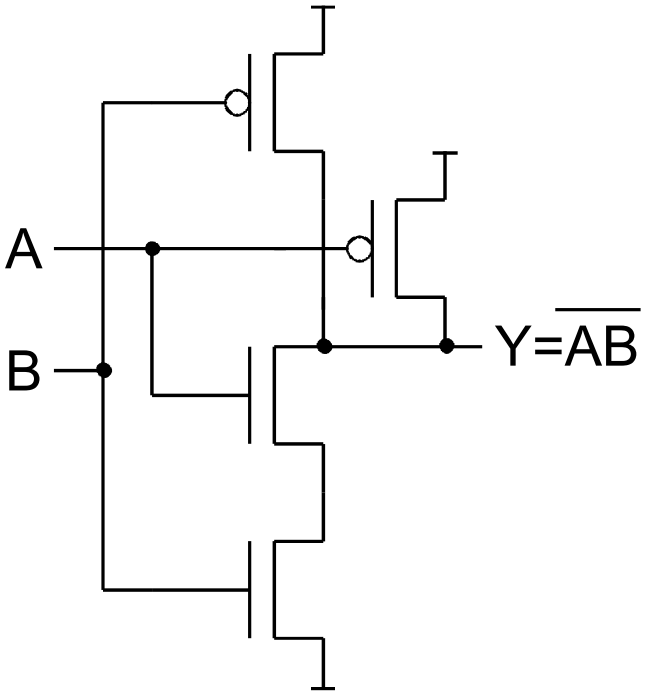


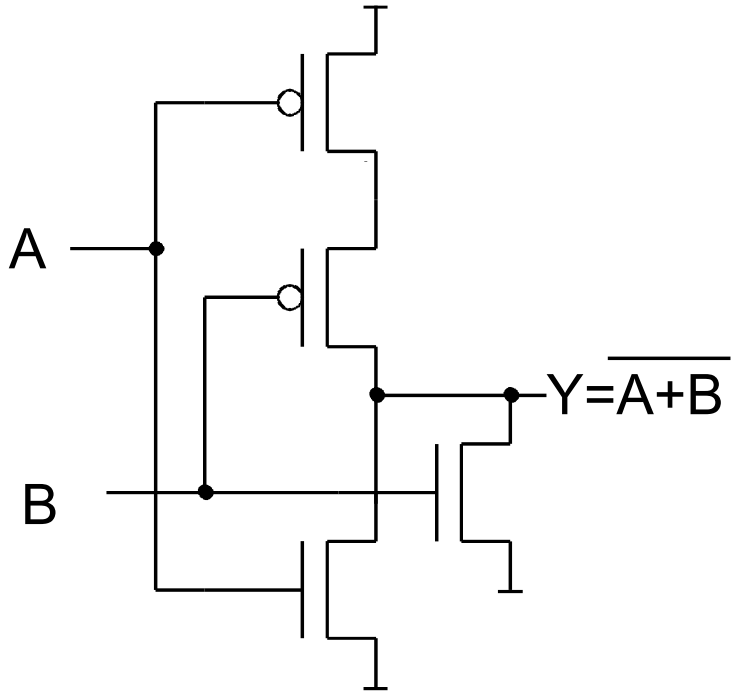
$Y=\overline{A+B}$



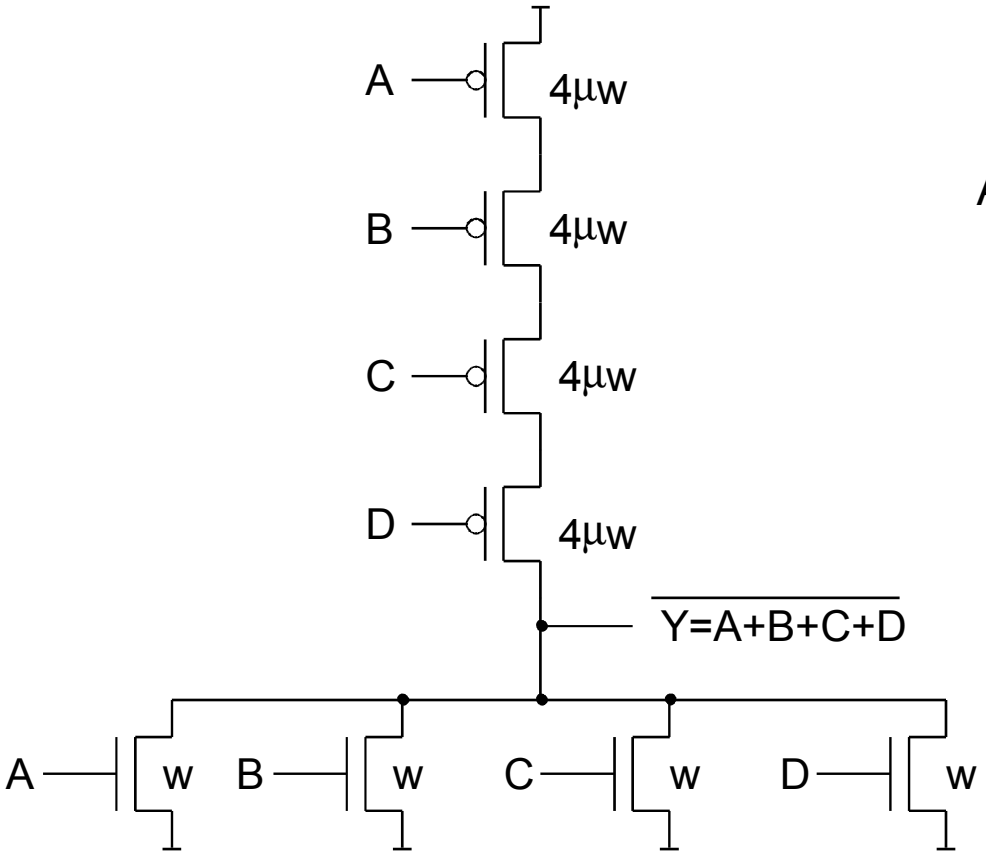
$Y=\overline{AB+C}$

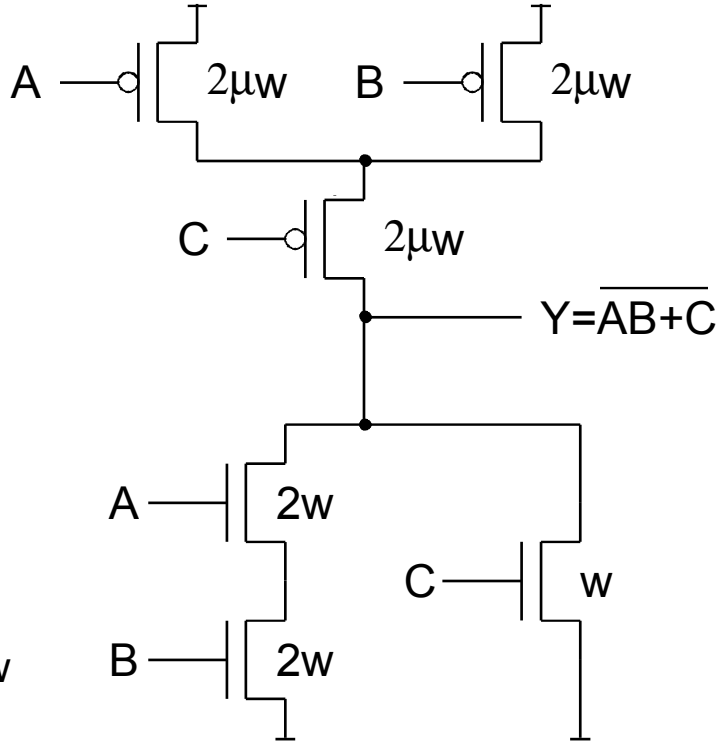
CMOS Gates: NAND and NOR



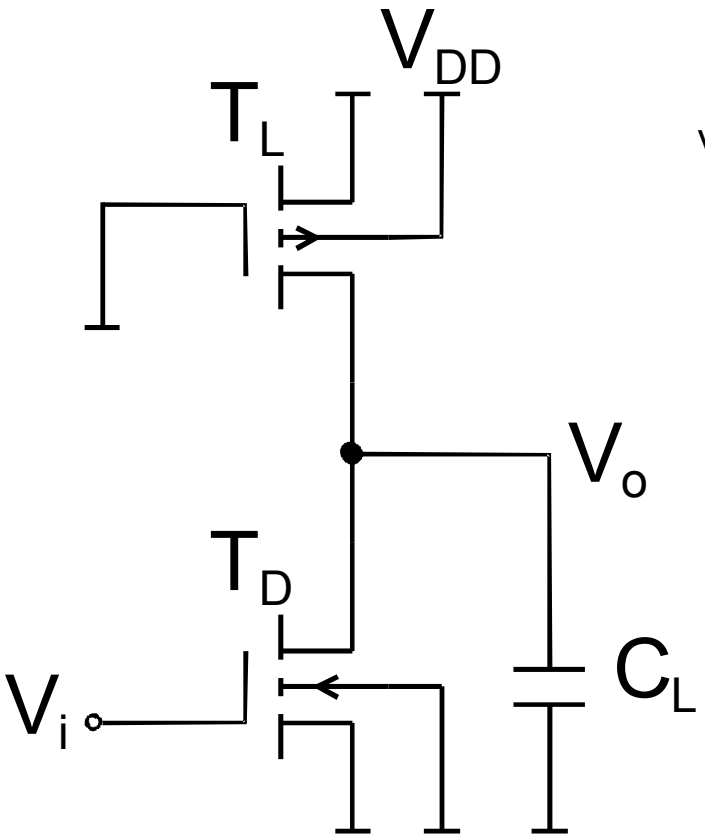


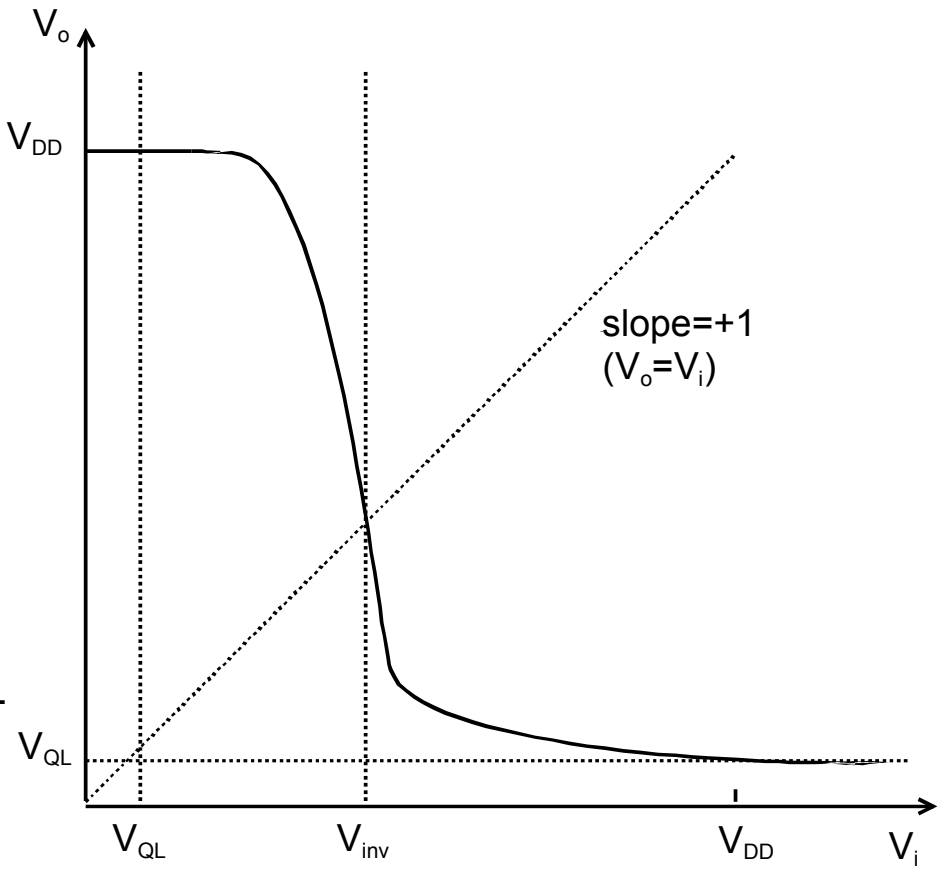
Transistor Widths in CMOS Gates



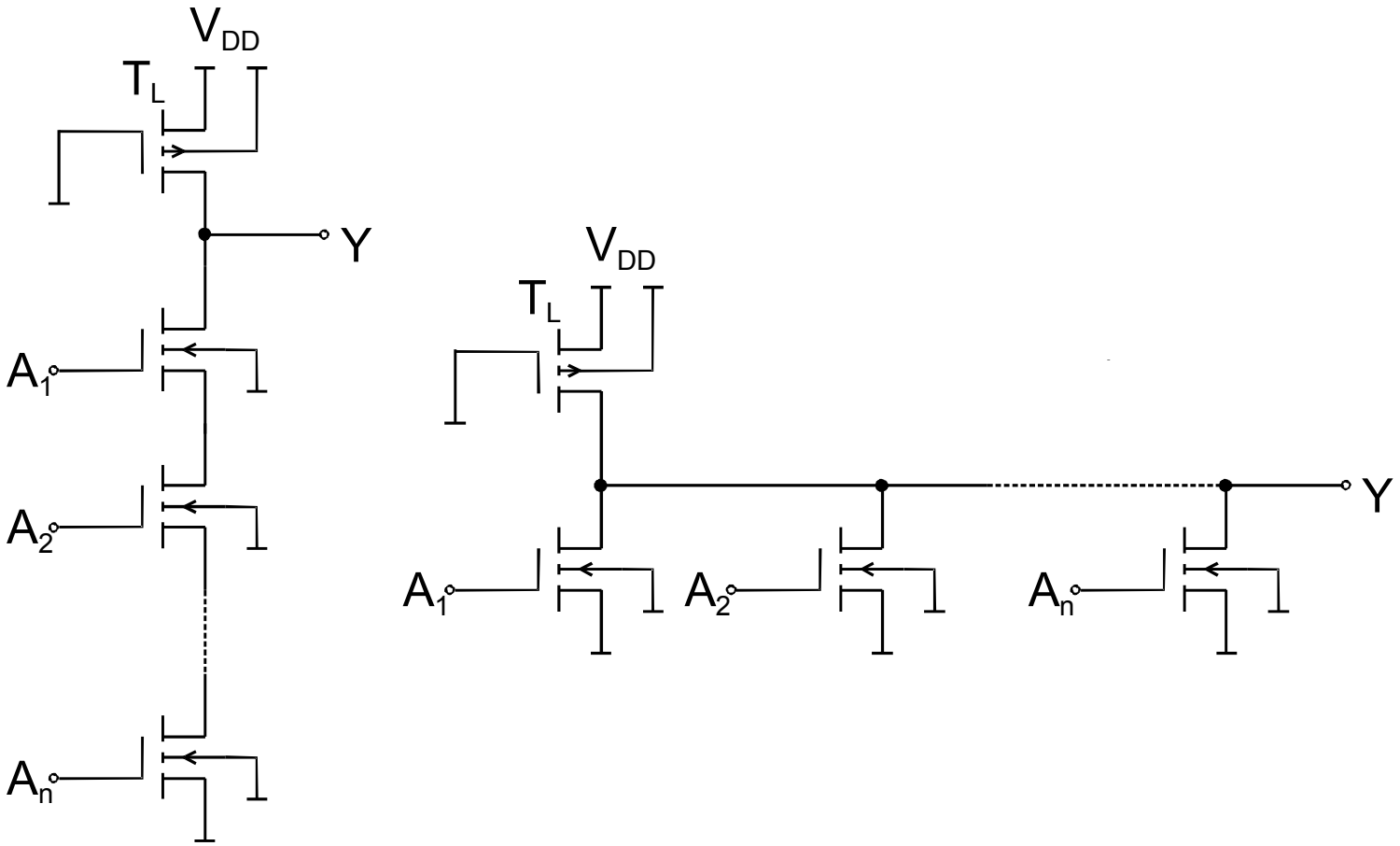


Pseudo-NMOS Inverter

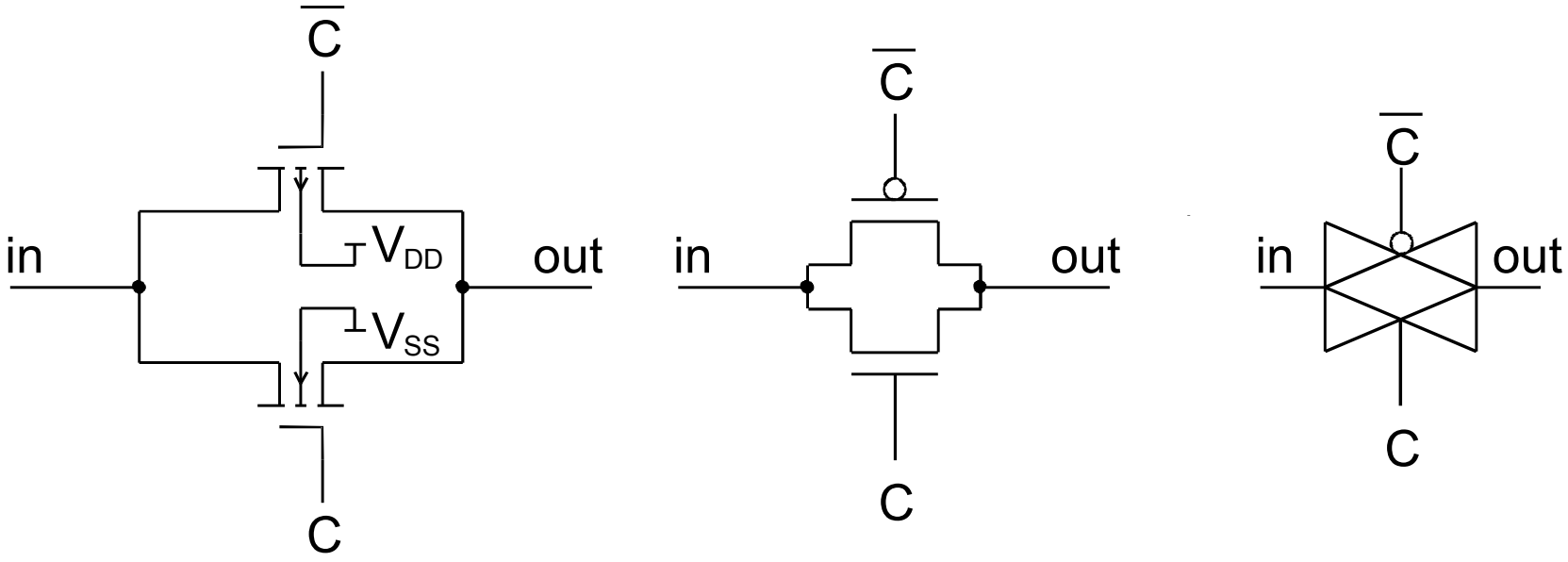




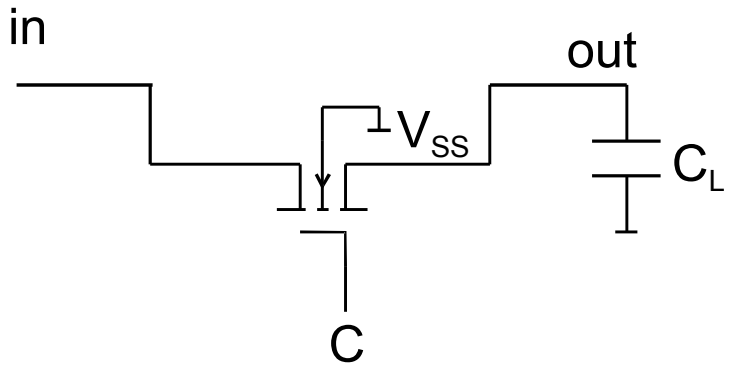
Pseudo-NMOS NAND and NOR Gates

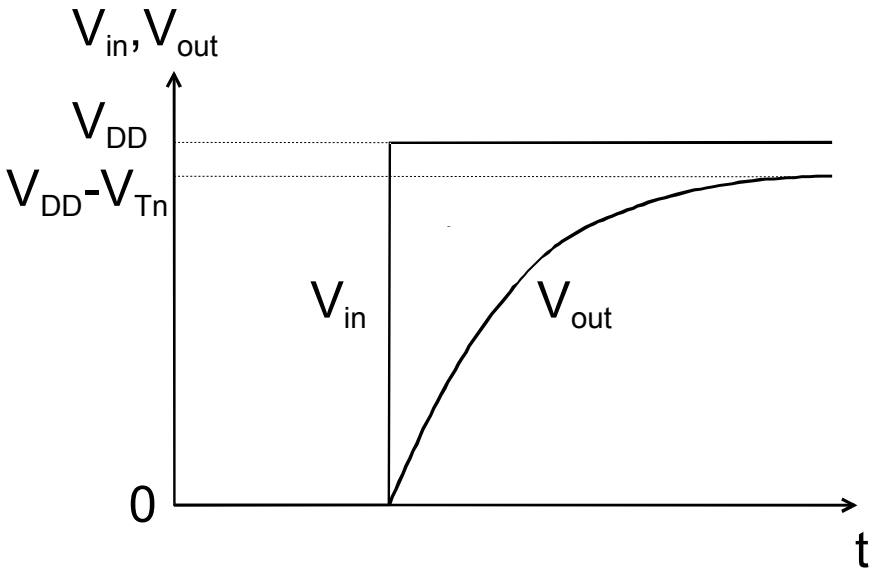


CMOS Transmission Gate

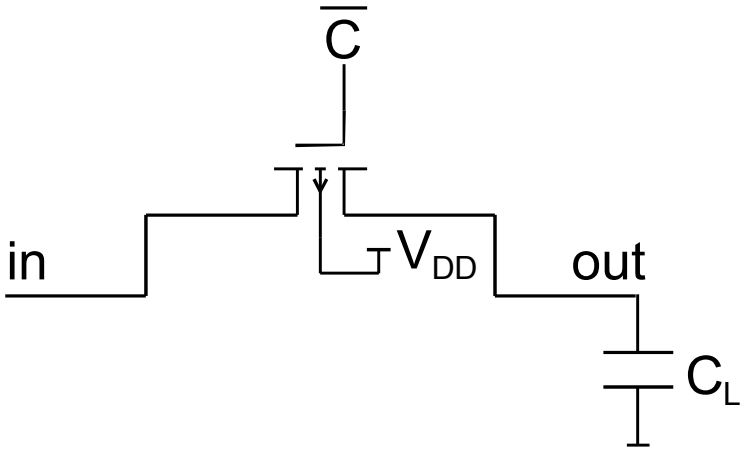


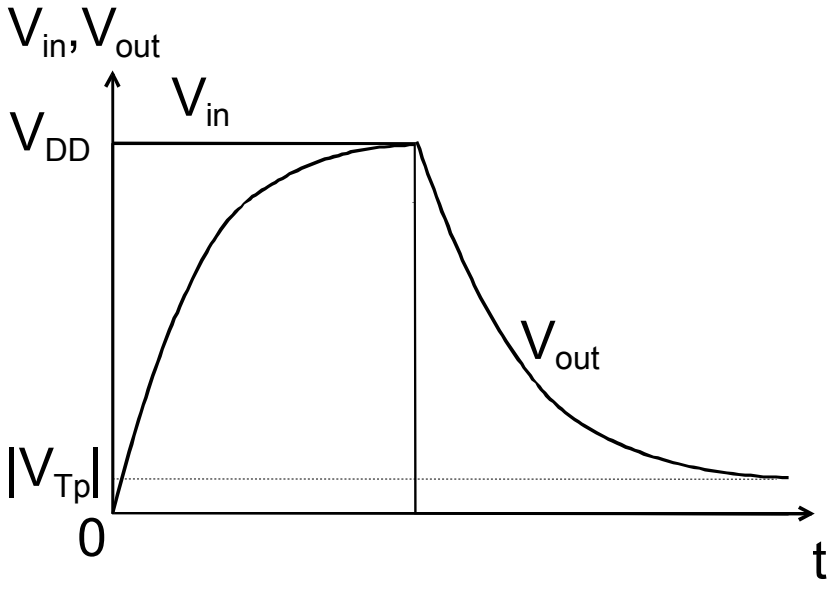
NMOS as A Switch



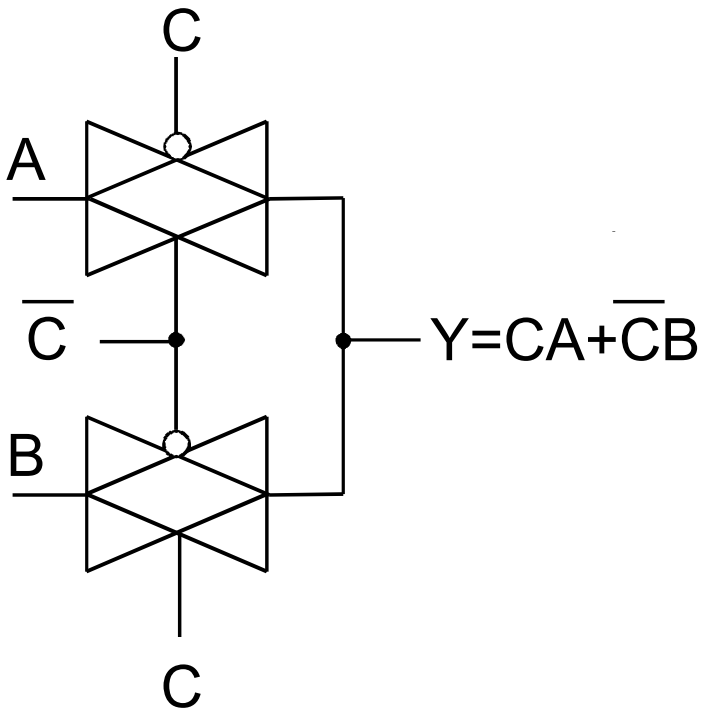


PMOS as A Switch

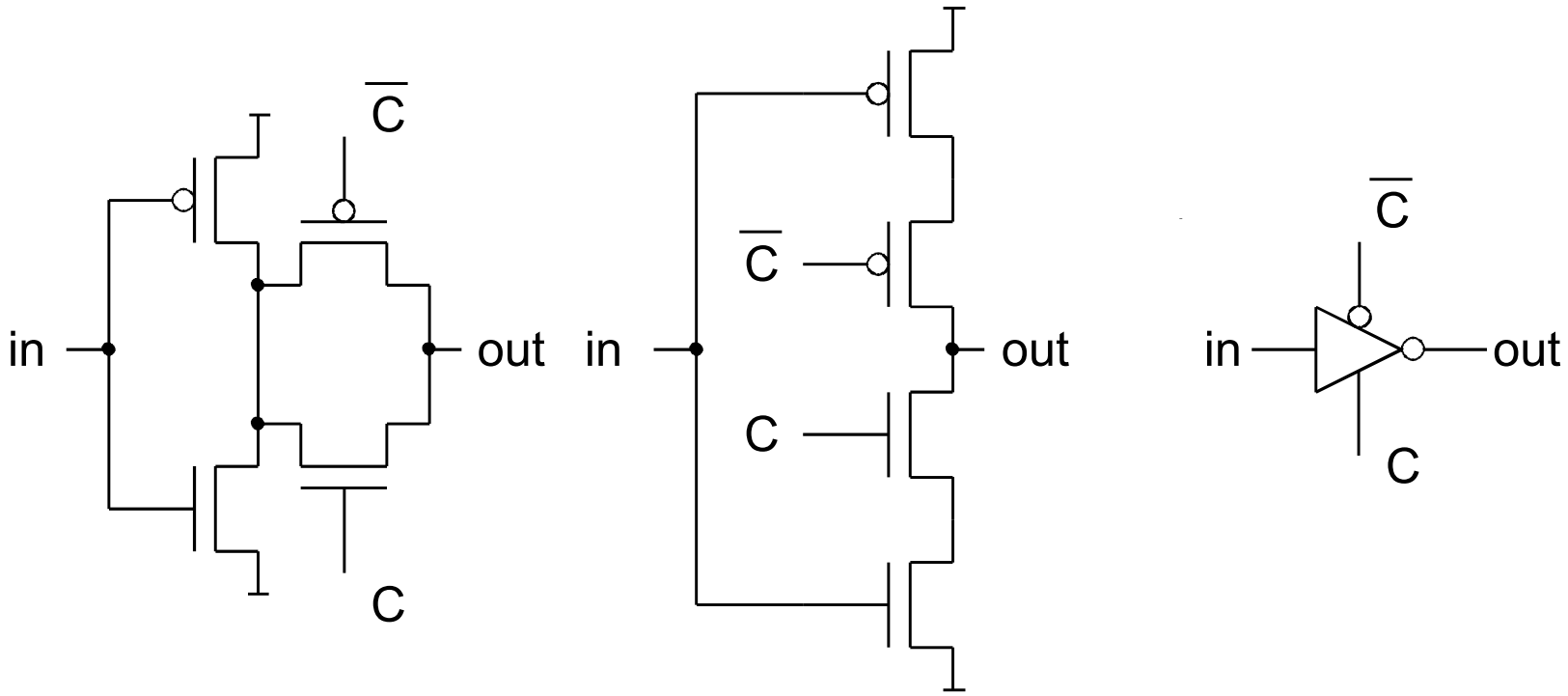




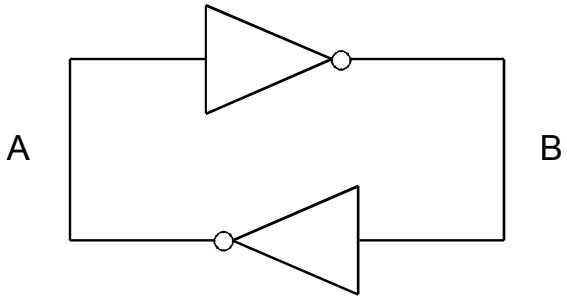
Two-Input Multiplexer

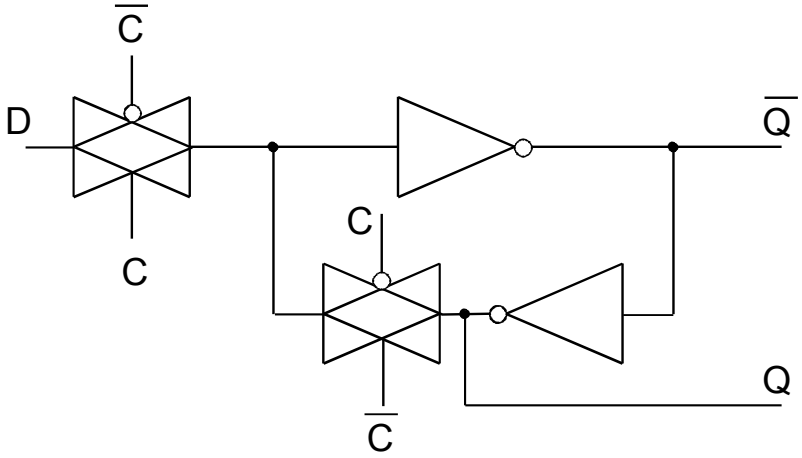


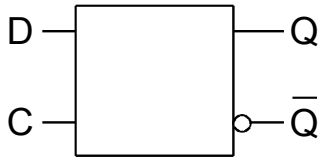
Three-State Inverter

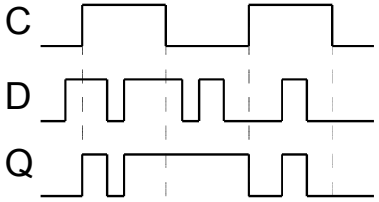


D latch

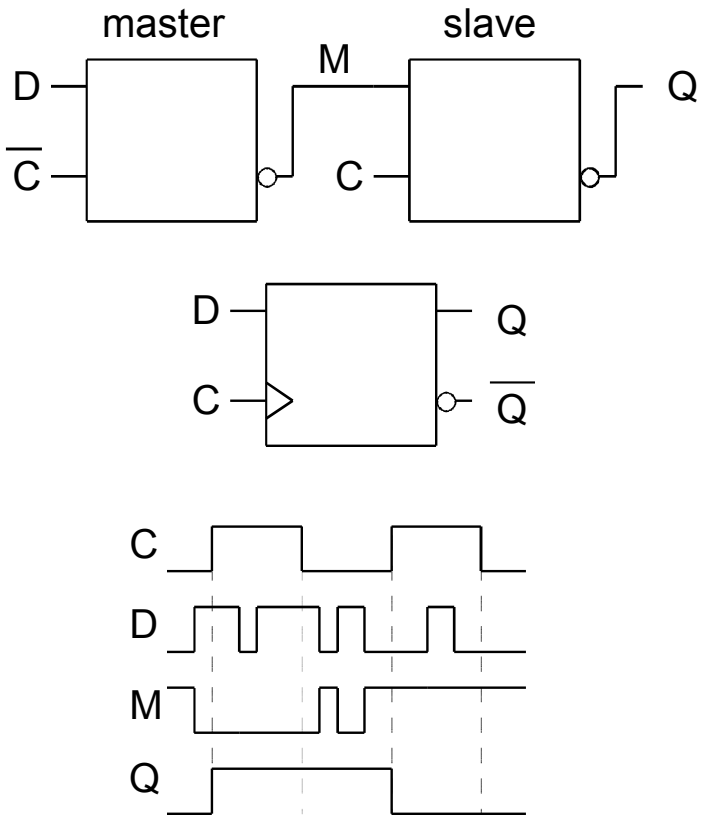




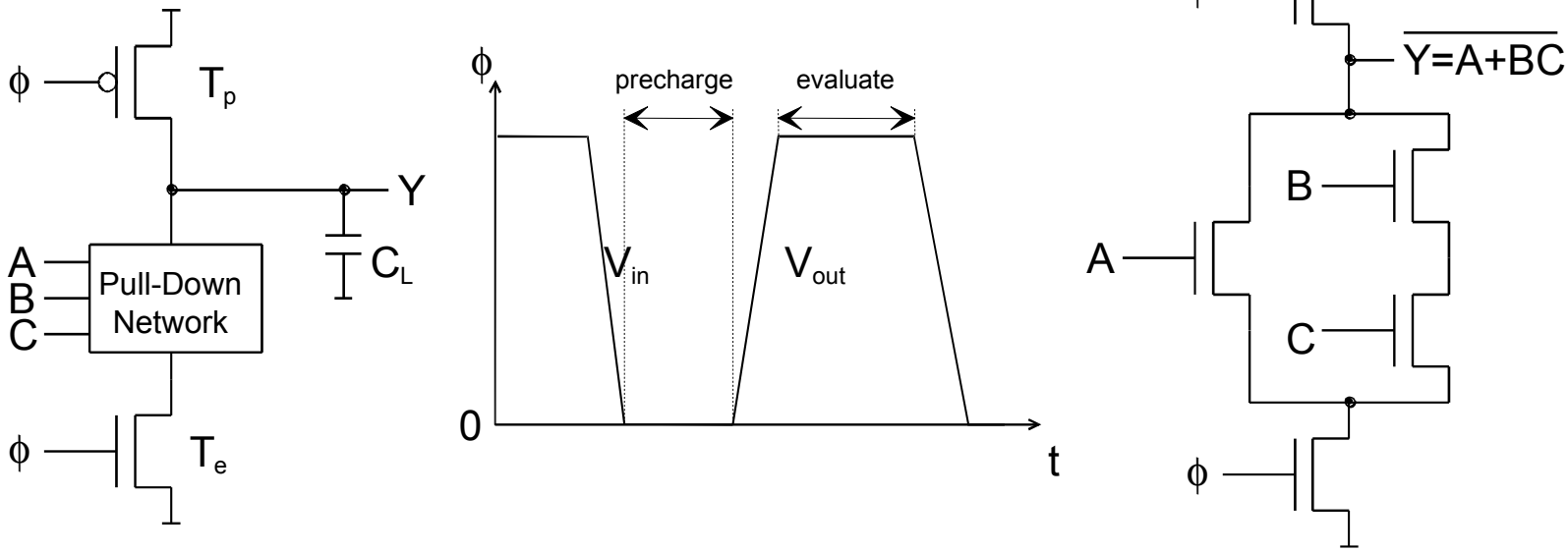




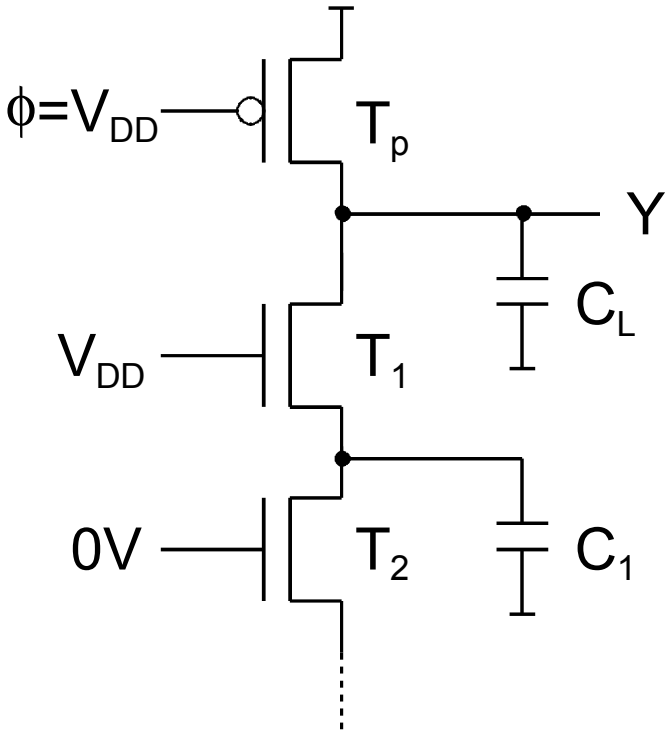
D Flip-Flop



Dynamic Gates



"Charge sharing"



Cascading of Dynamic Gates