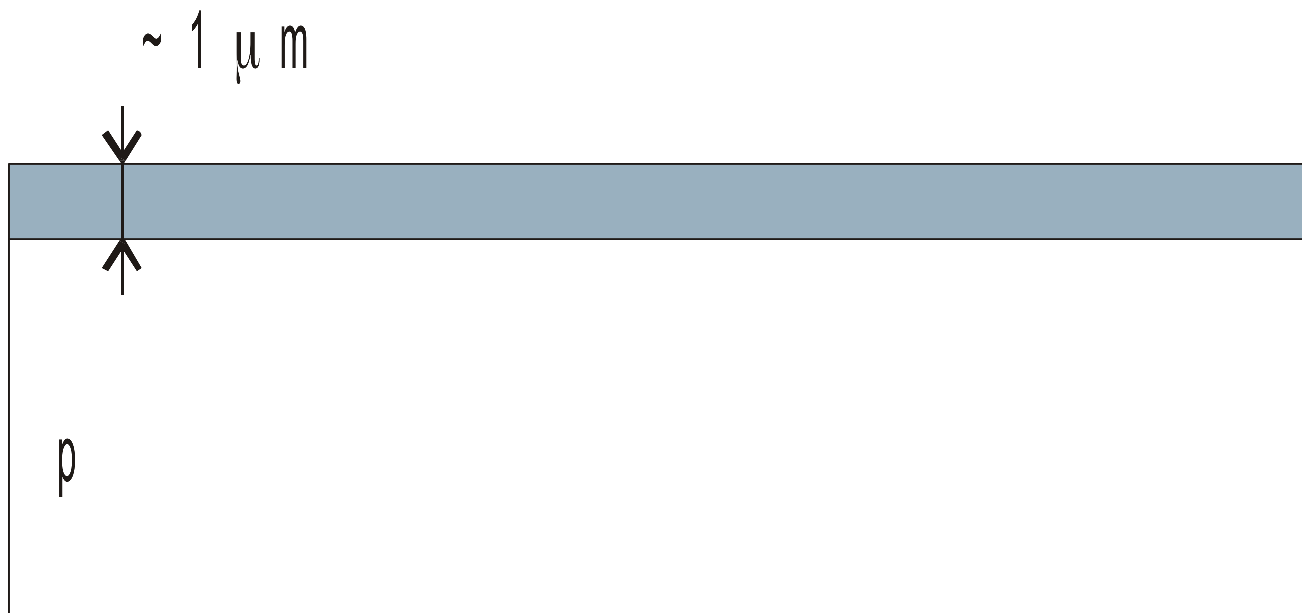
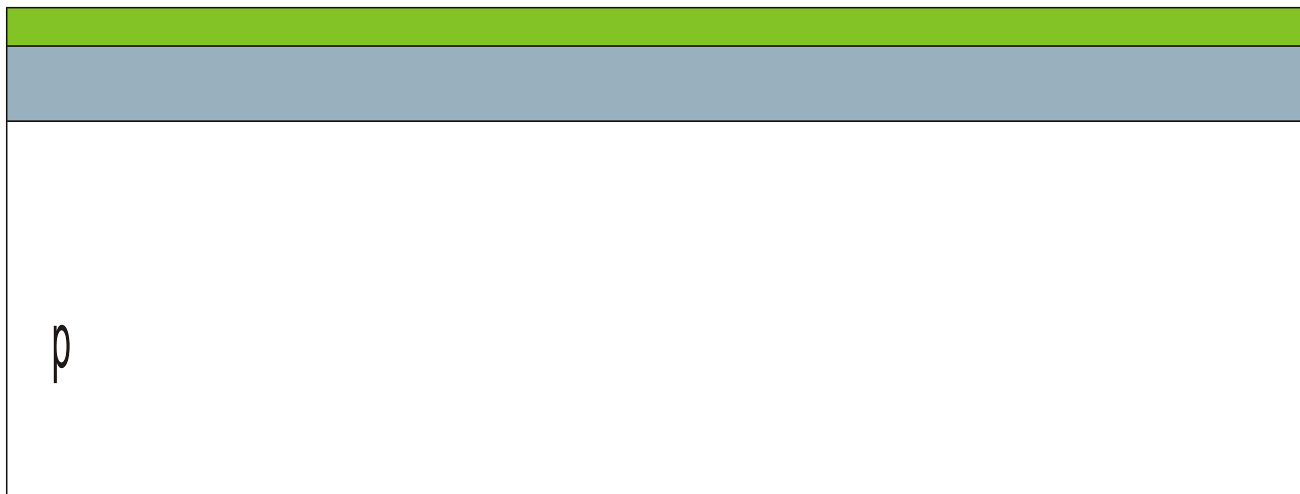
N-well CMOS Process

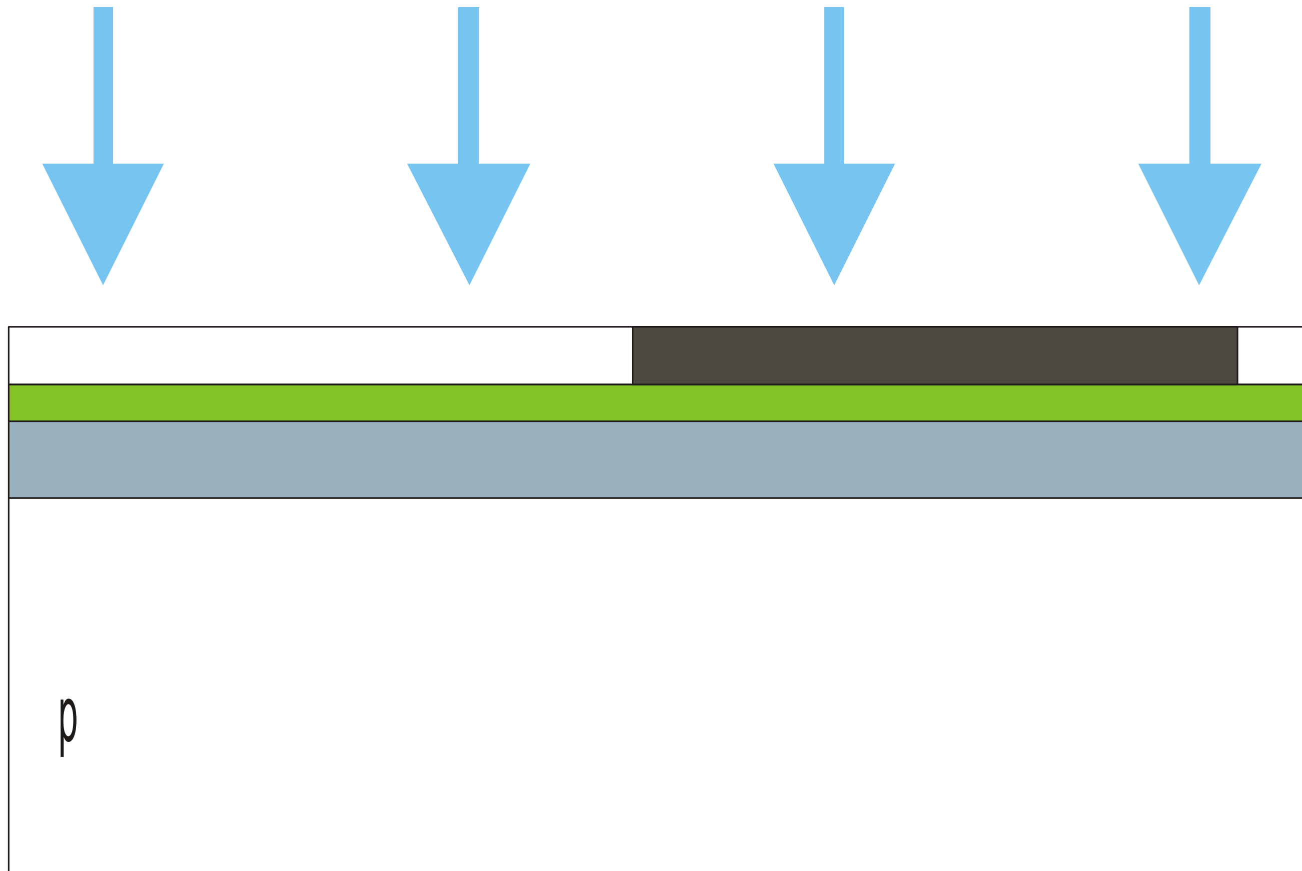
Substrate Oxidation



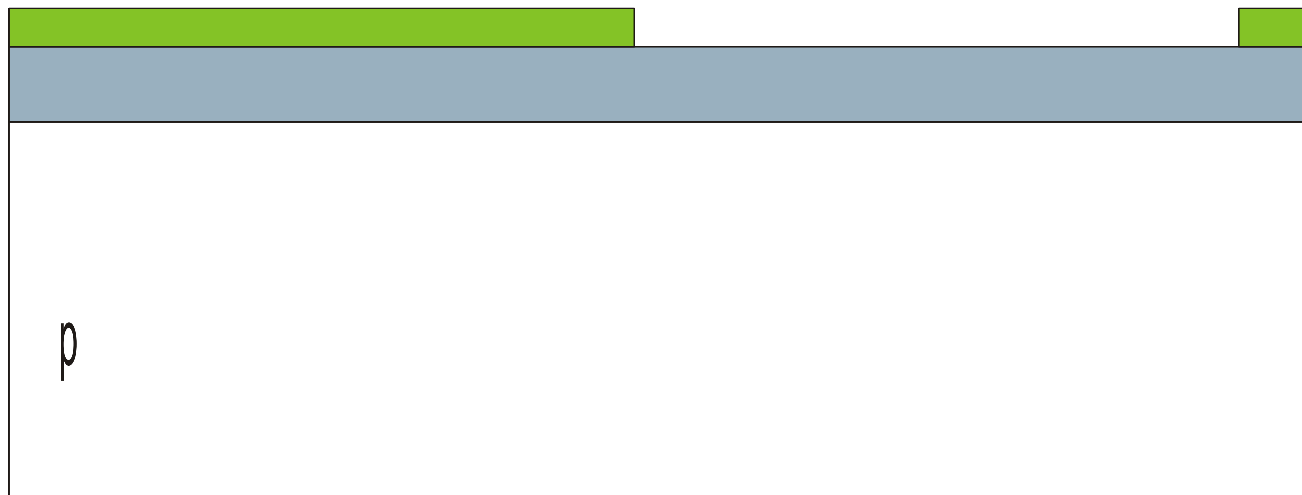
Deposition of Photoresist



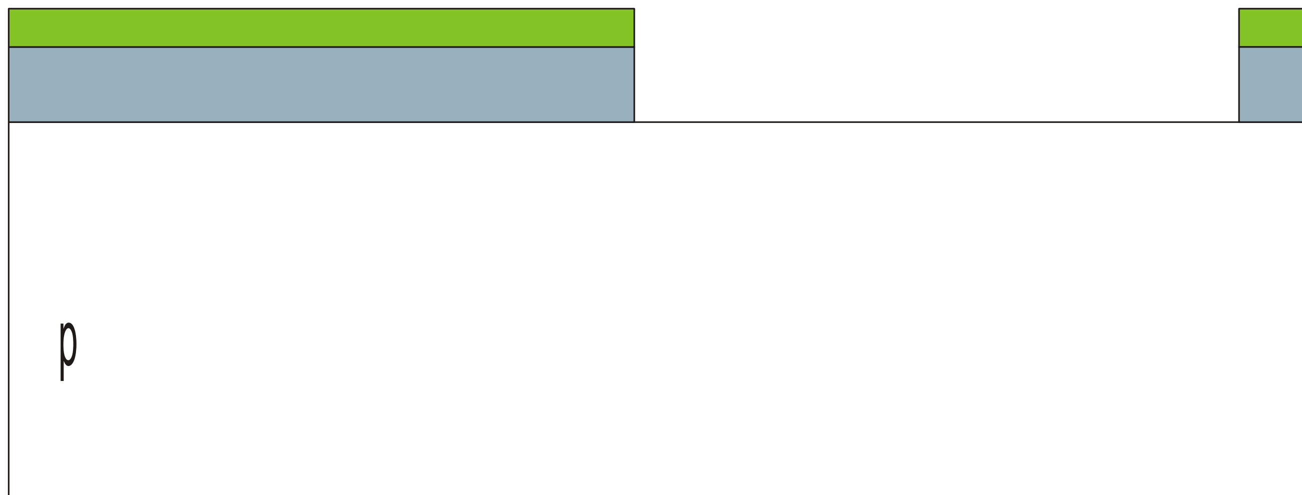
Masking and Projection



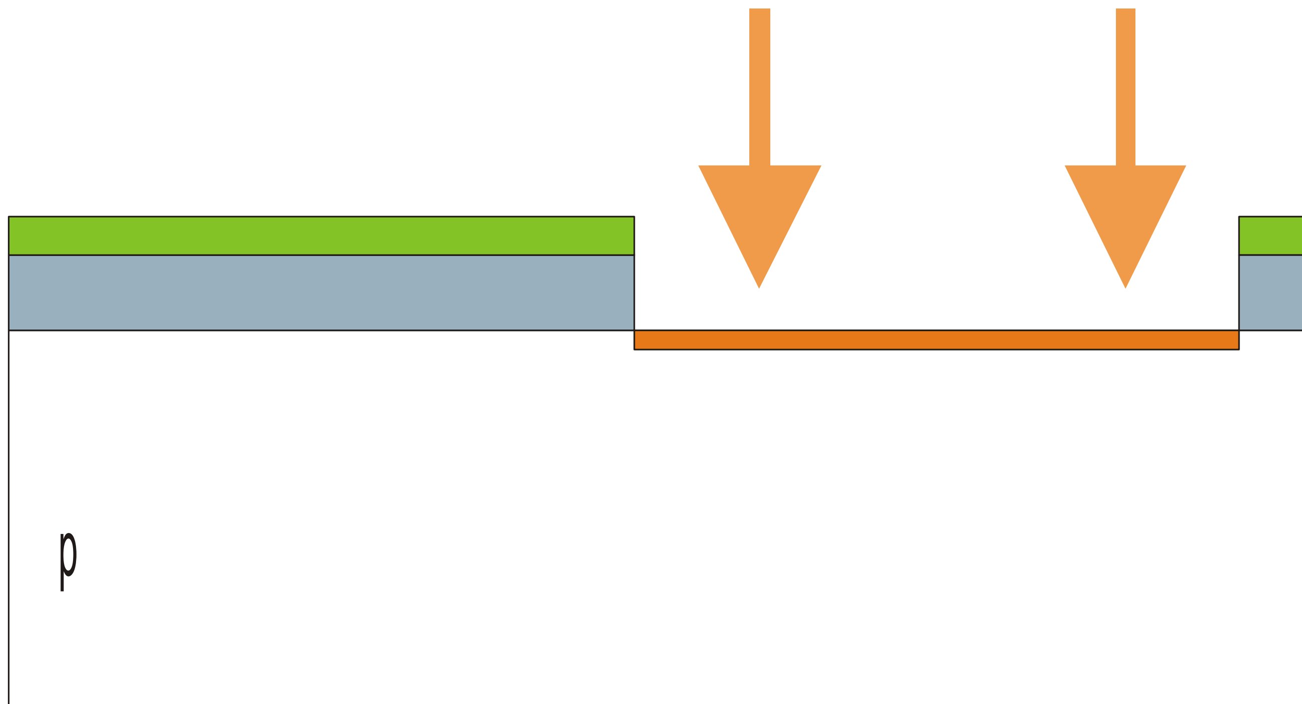
Developing of Photoresist



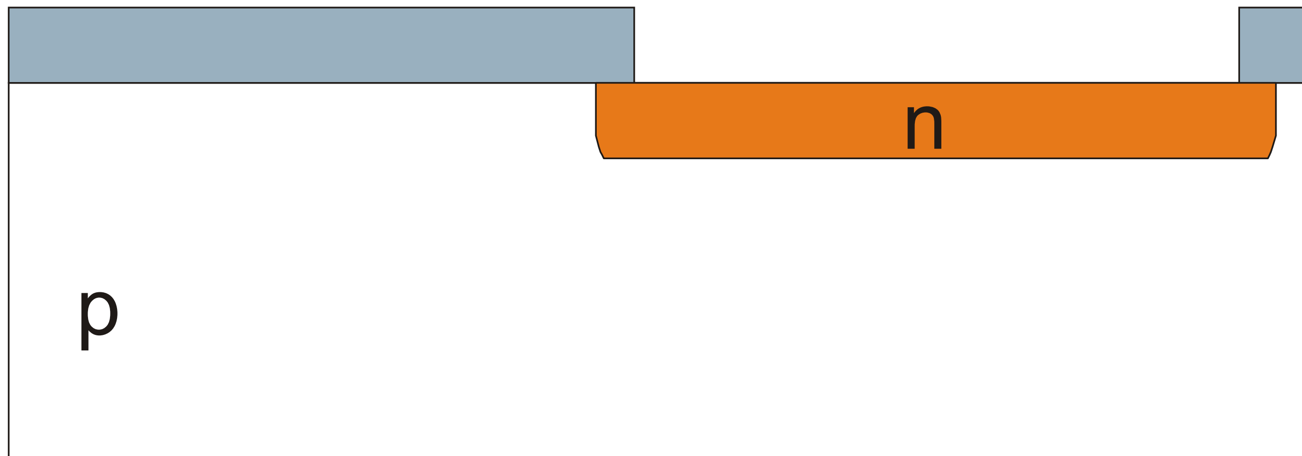
Oxide Etch



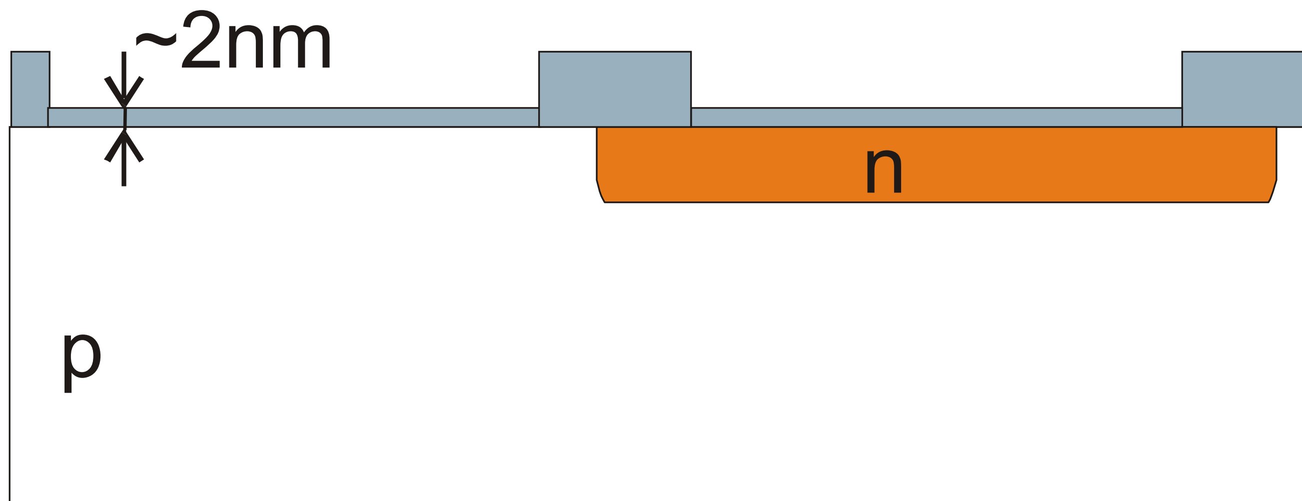
Ion Implantation



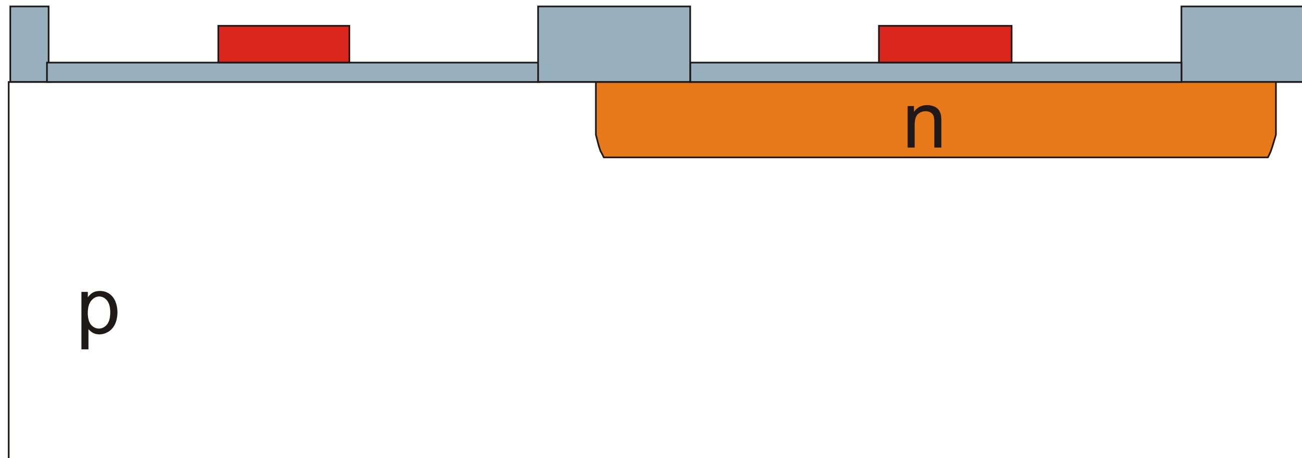
Annealling / Rediffusion



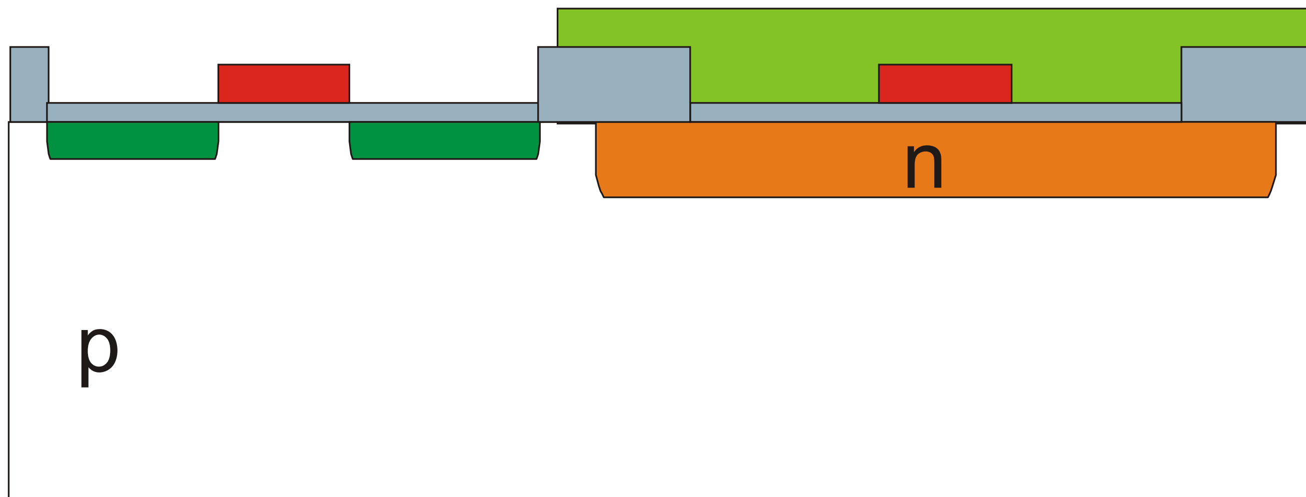
Gate Oxide



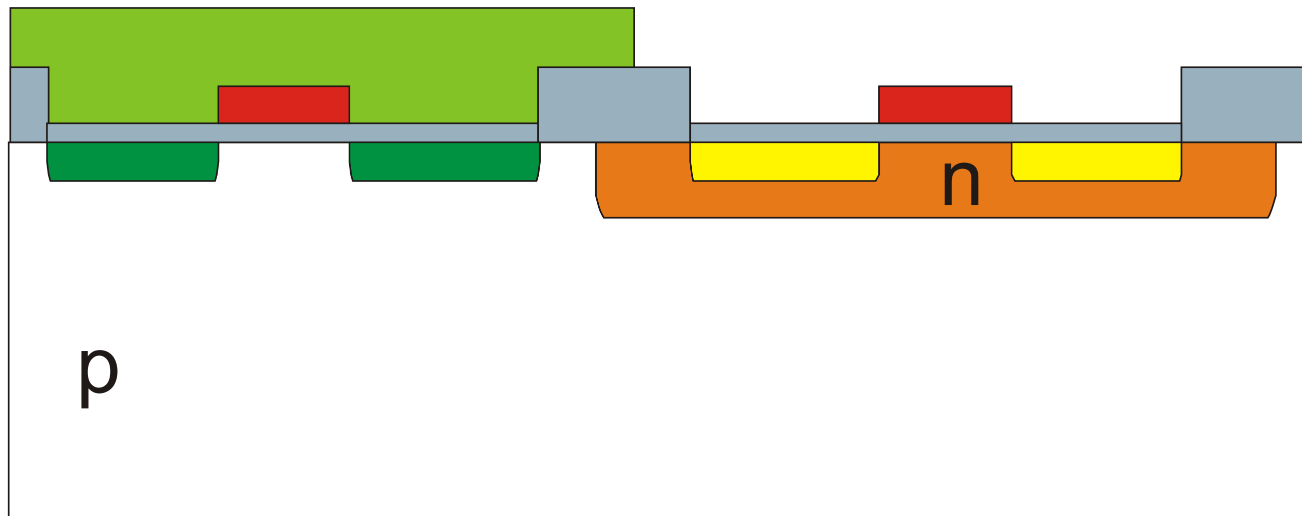
Deposition, Masking and Etching of Polysilicon



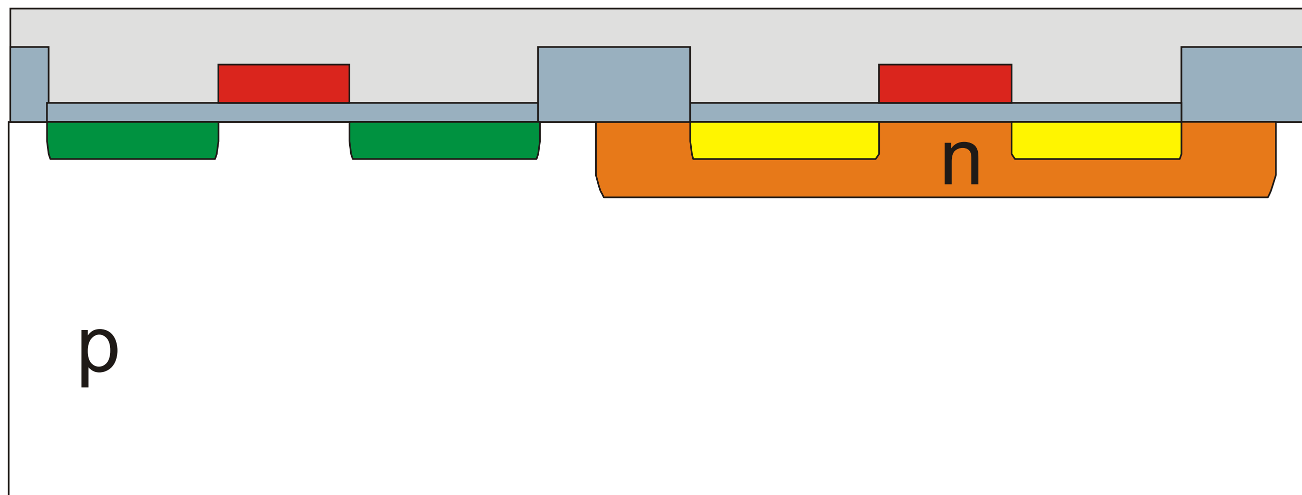
NMOS Manufacturing



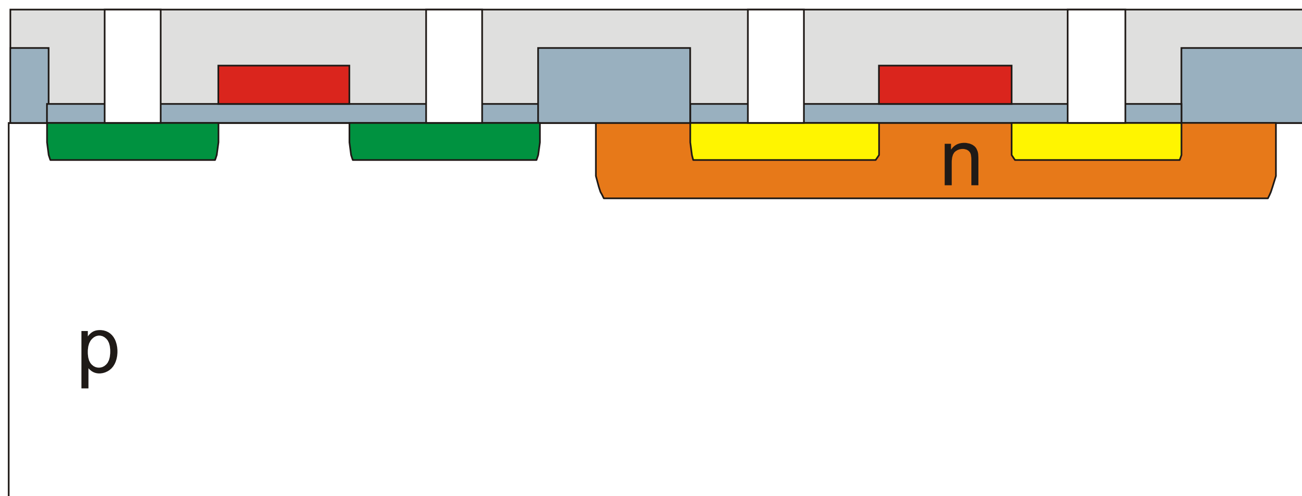
PMOS Manufacturing



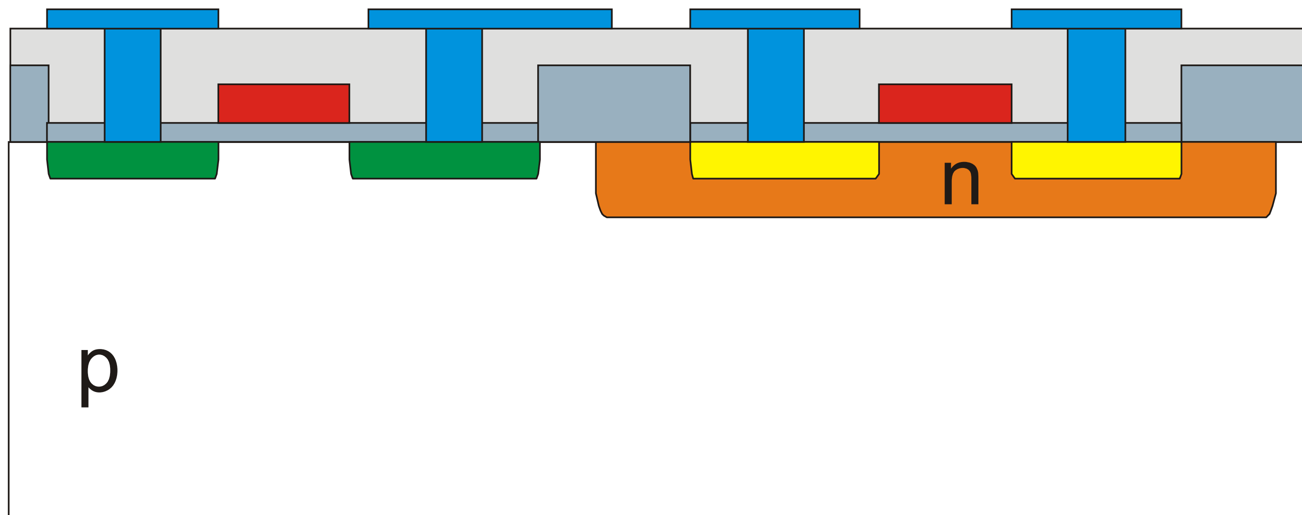
First Insulating Layer



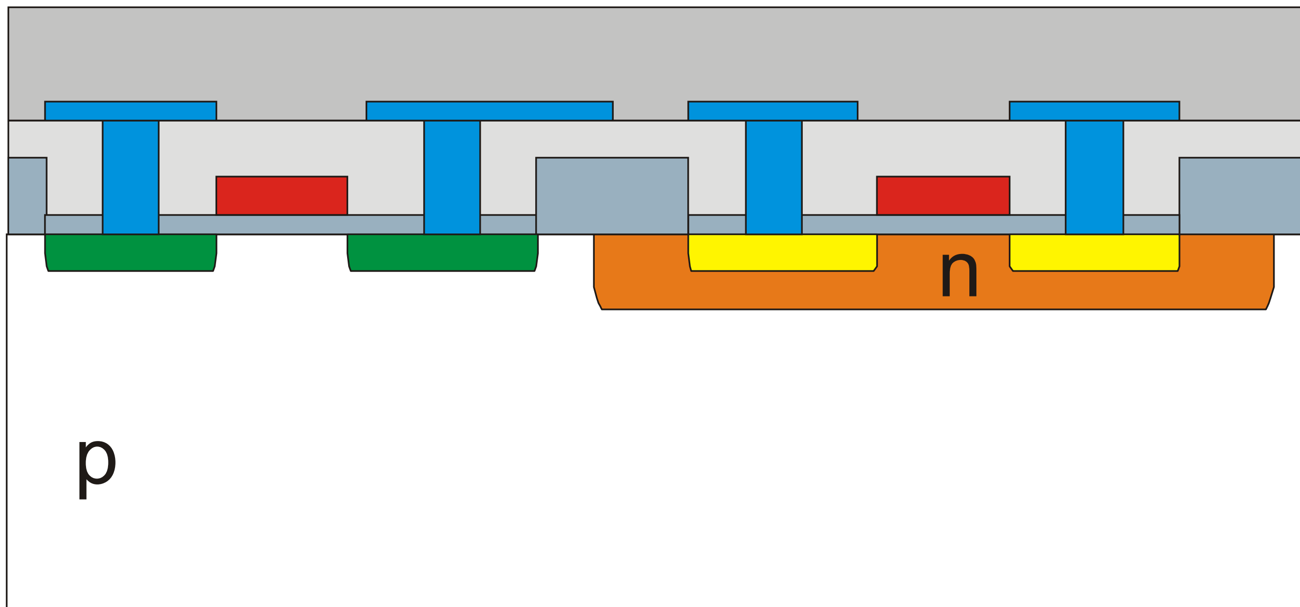
Contact Etch



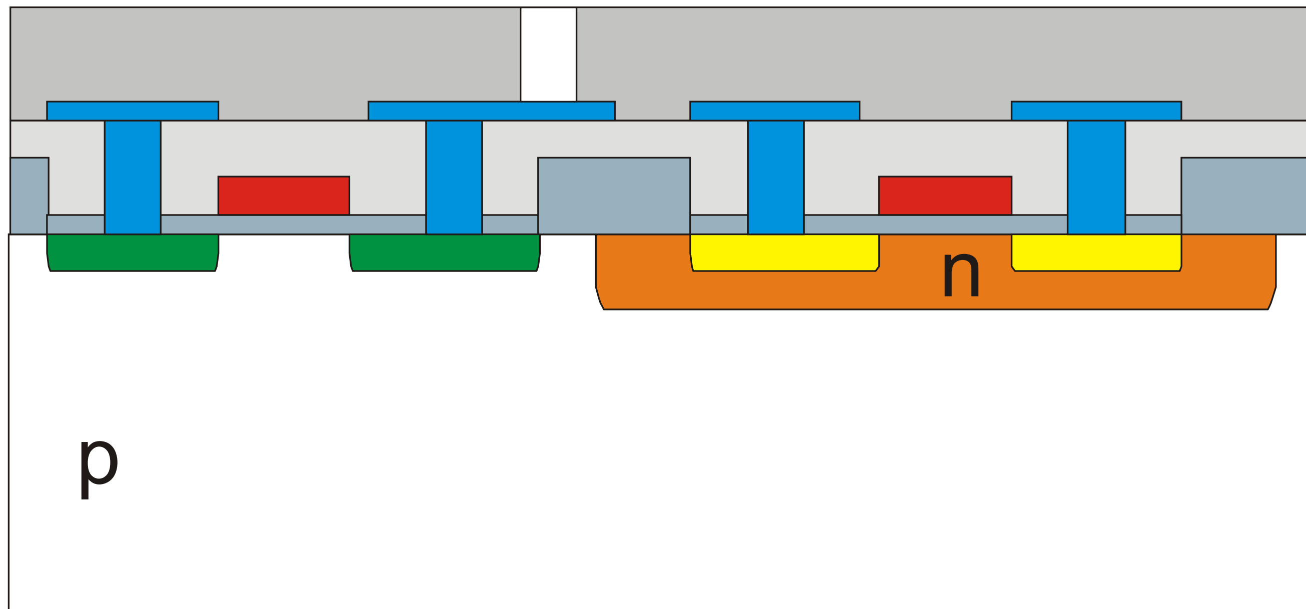
Contacts and Metallization I



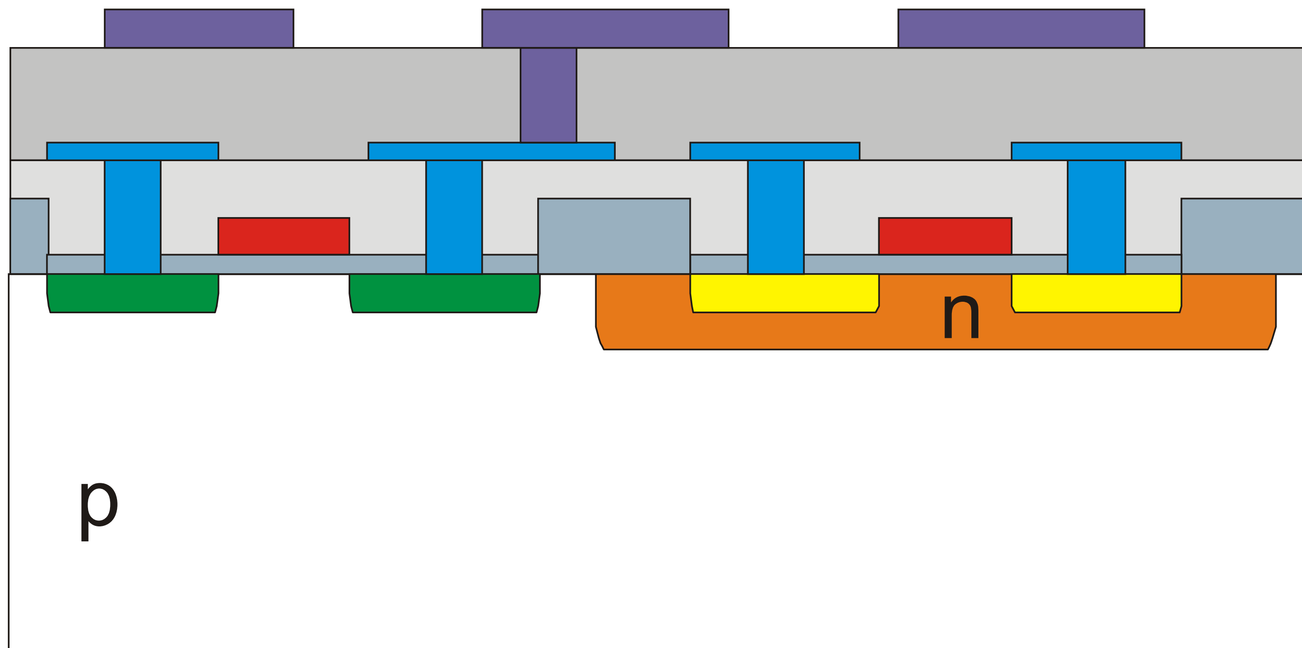
Second Insulating Layer



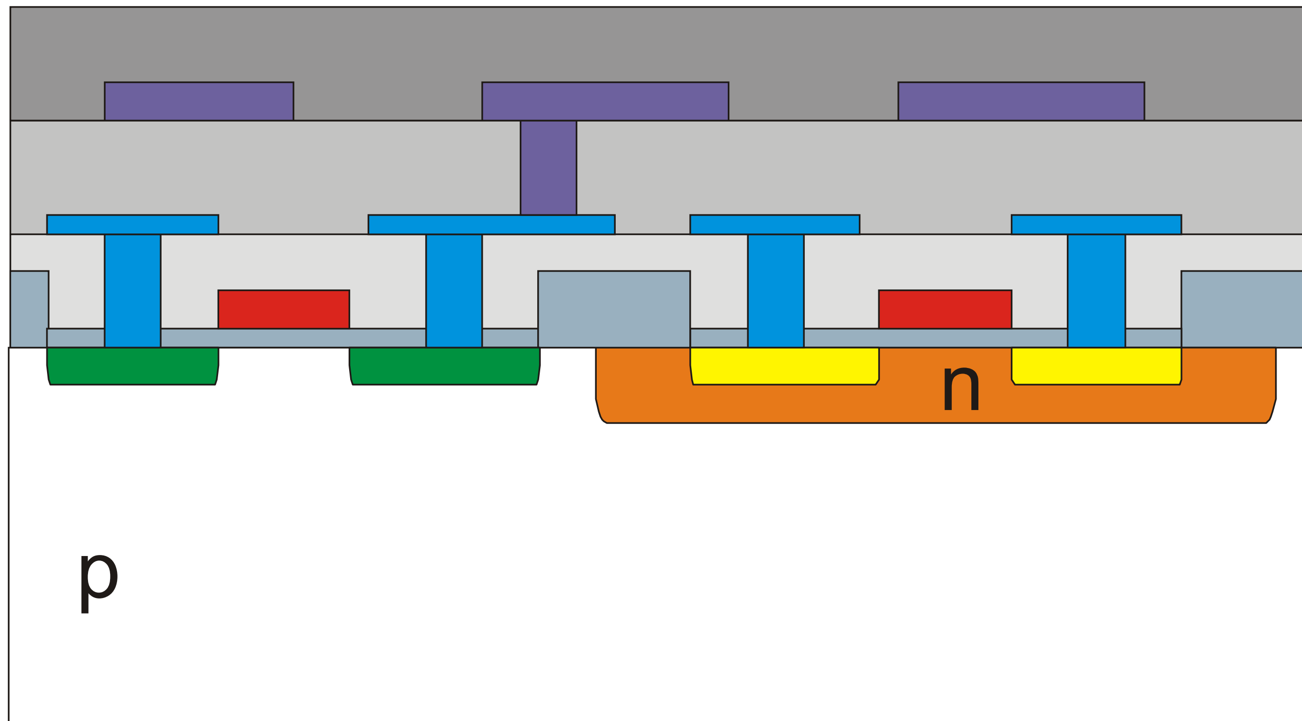
VIA Etch



Vias and Metallization II

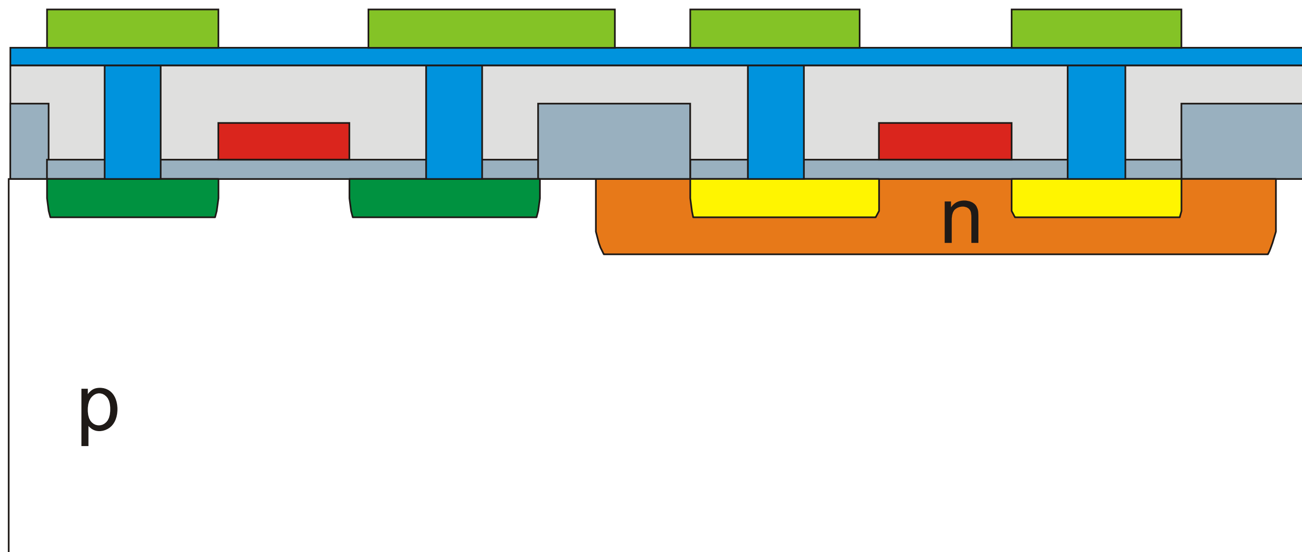


Final Passivation

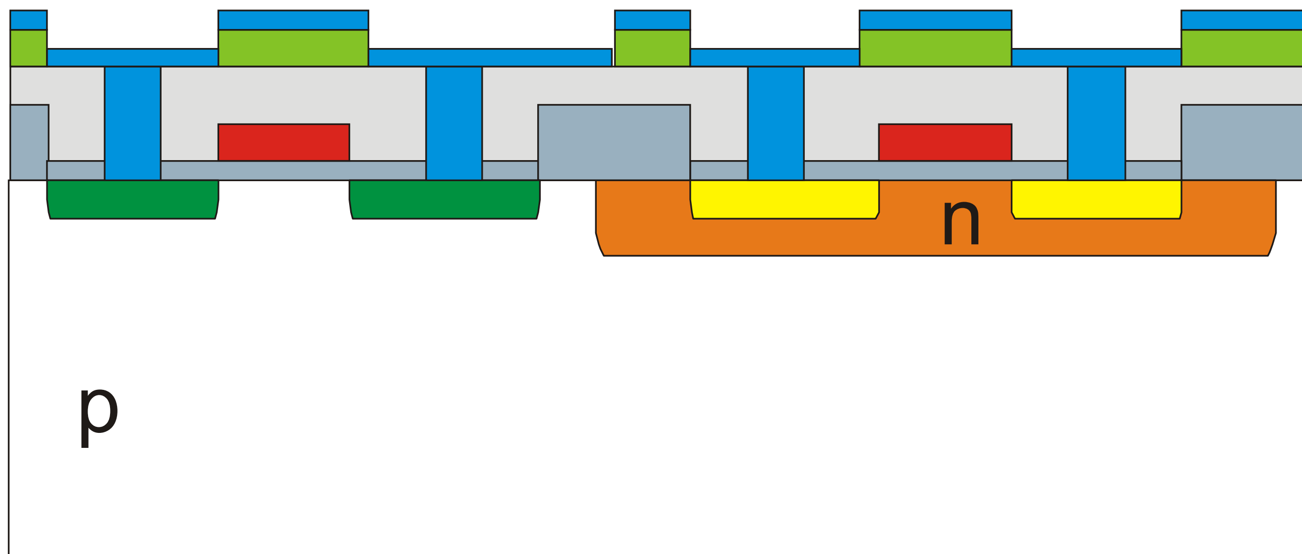


Deposition of Metallic Layers

Etching Away of Excessive Metal



Lift-off

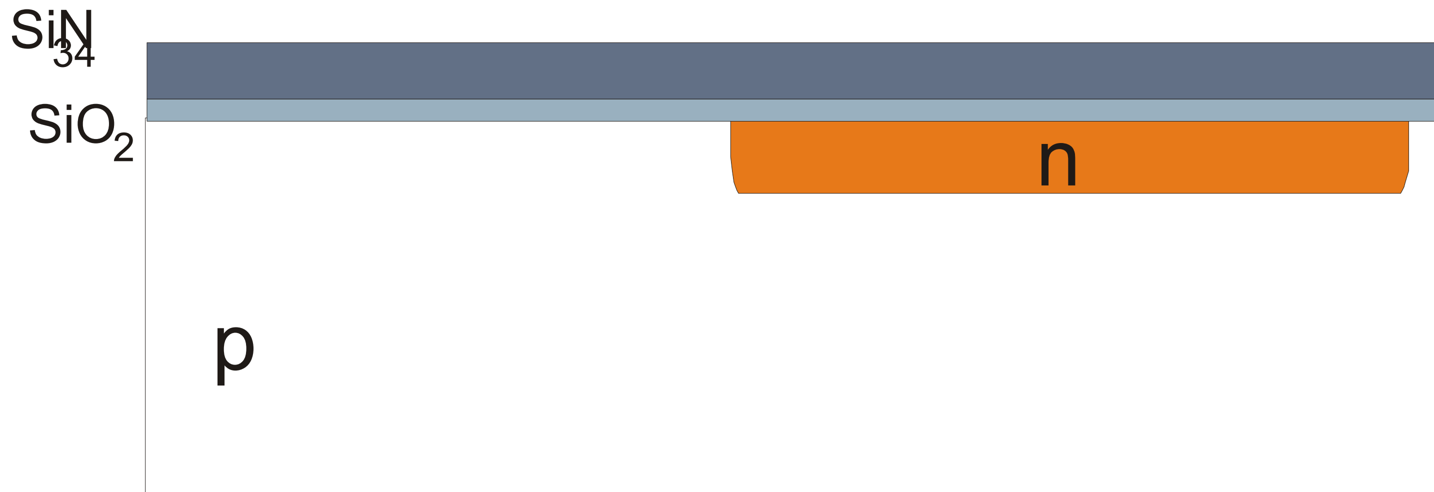


Metal-Semiconductor Contacts

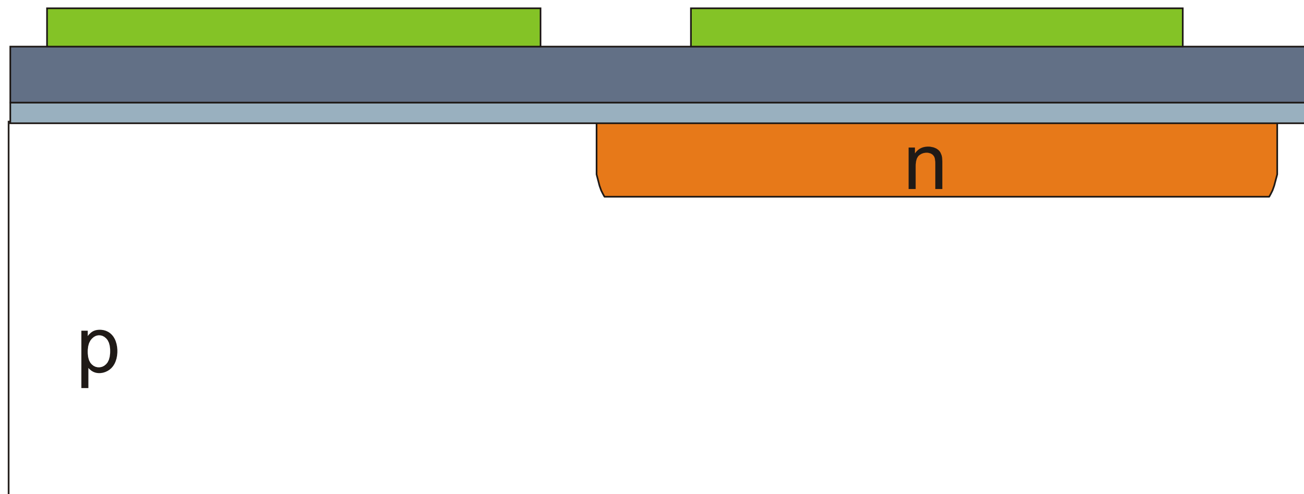
- Drain and source pins
- Substrate and well bias
- Always to heavily doped semiconductor
  - low ohmic resistance
  - no Schottky junction

LOCOS Technology

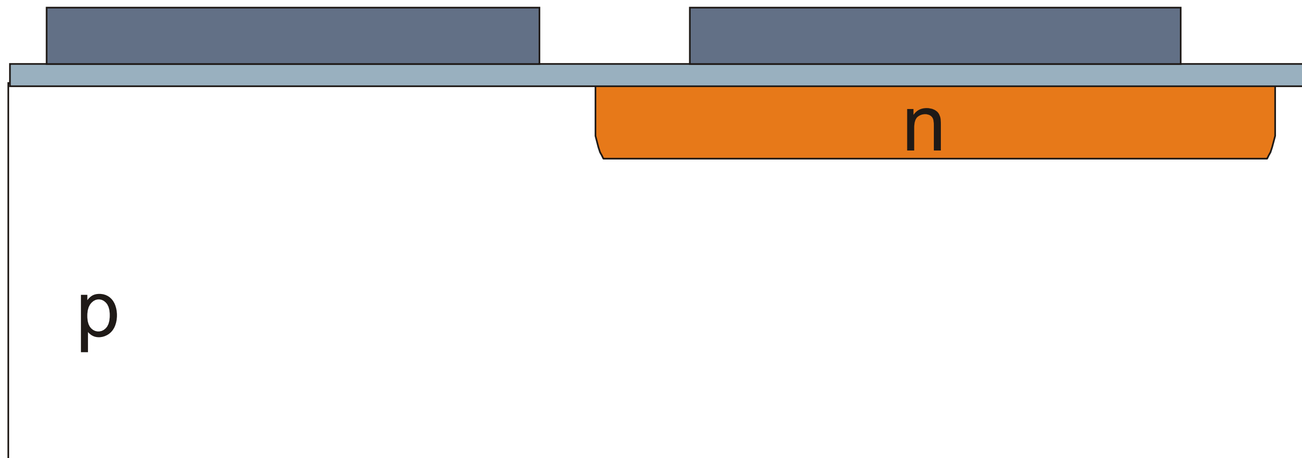
Deposition of Silicon Dioxide and Silicon Nitride



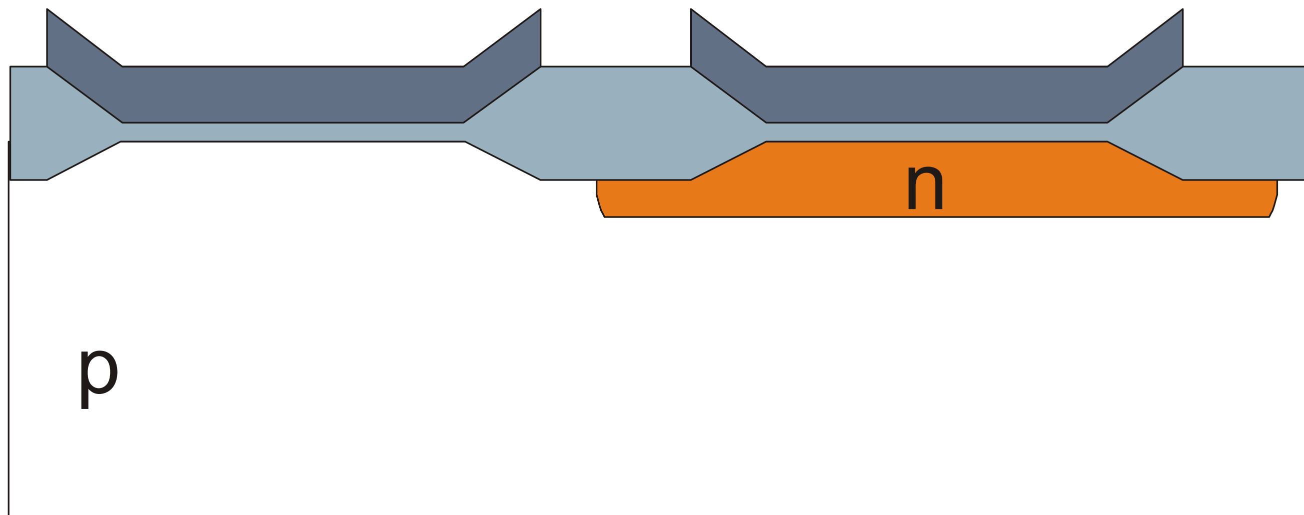
Deposition, Masking and Etching of Photoresist



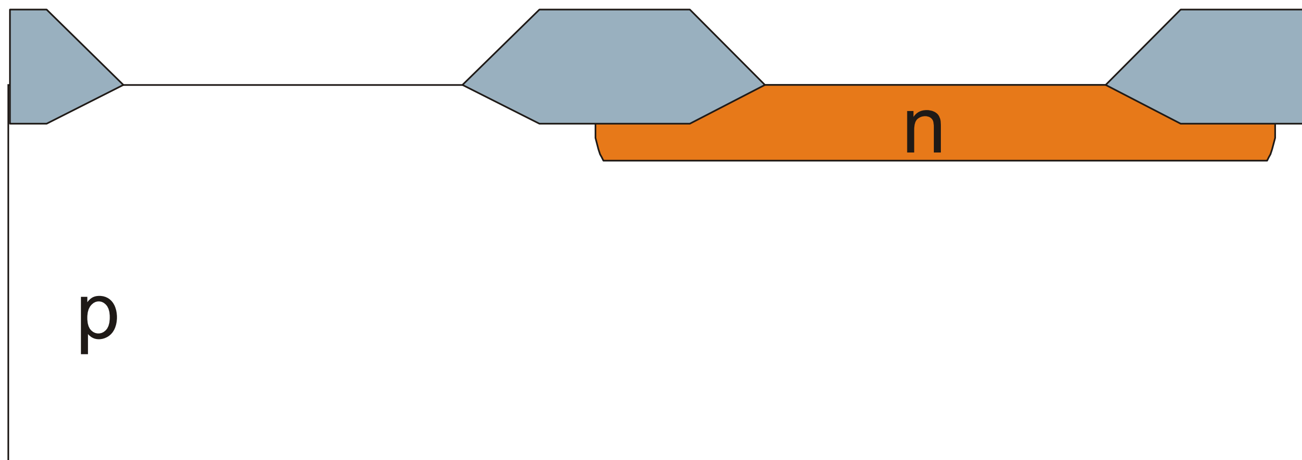
Etching of Nitride and Removal of Photoresist



Field Oxide Manufacturing



Removal of Nitride and Thin Oxide



Shallow Trench Isolation (STI)

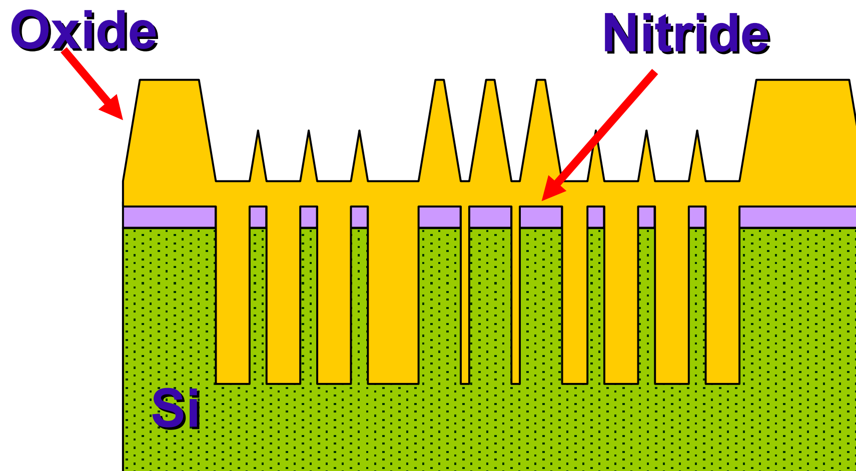
LOCOS Shortcomings

- In submicron technologies (below 250 nm) LOCOS isolation takes too much space
- The mechanical stress appearing at thin/thick oxide border increase the gate leakage current

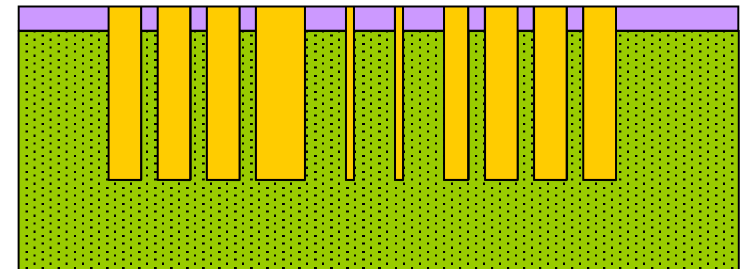
Shallow Trench Isolation

- Curently the most commonf form of isolation
- Trenches in substrate filled with oxide surrond the devices and isolate them from the surroundings
- Process steps:
  - Diffusion areas covered with nitride
  - Trenches etched and filled with CVD oxide
  - CMP (Chemical and Mechanical Polishing) removes the unneeded oxide

Shallow Trench Isolation



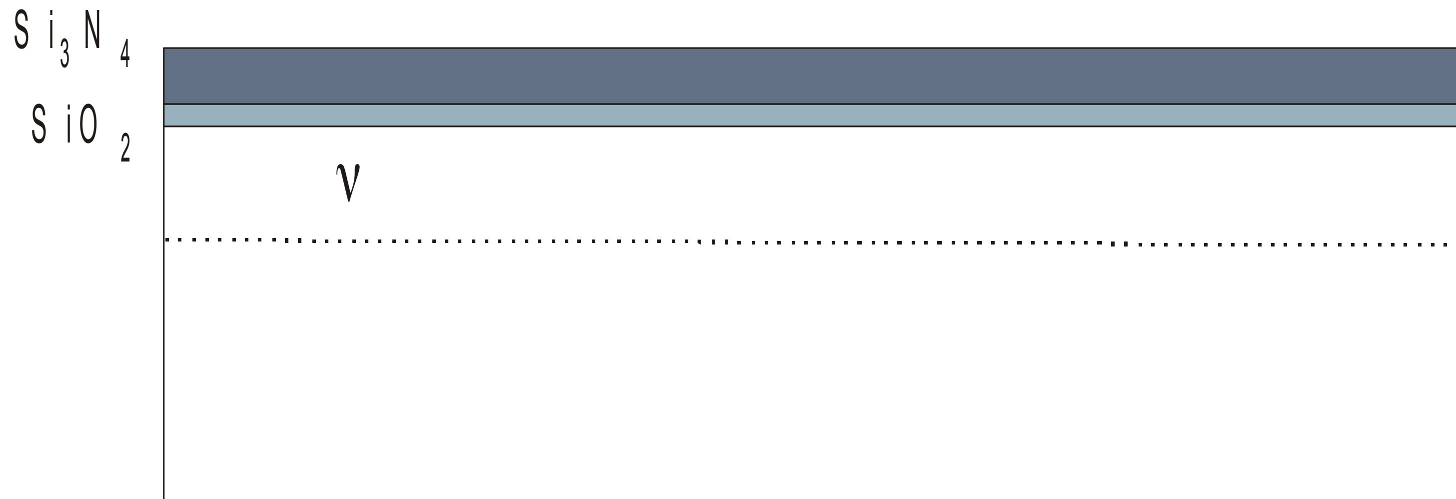
Before CMP



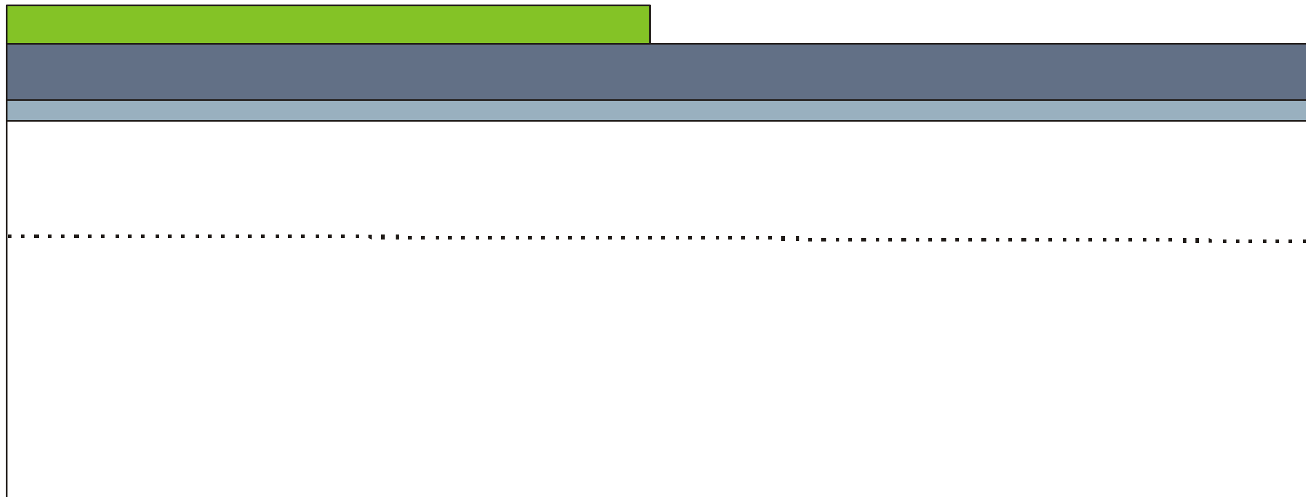
After Perfect CMP

Twin-Well (Twin-Tub) Technology

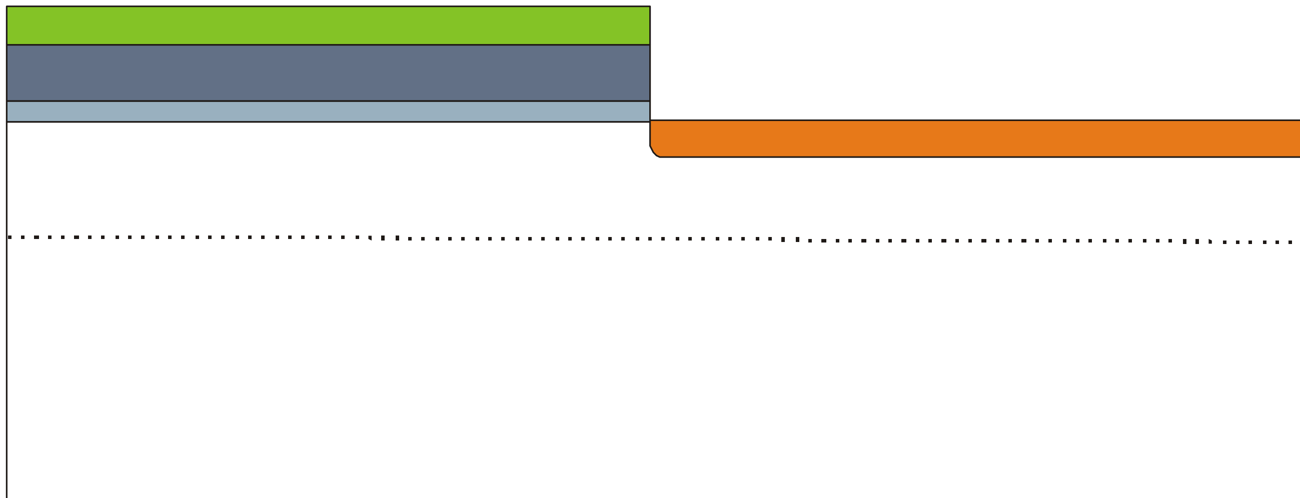
Epitaxial Layer Covered by Oxide and Nitride



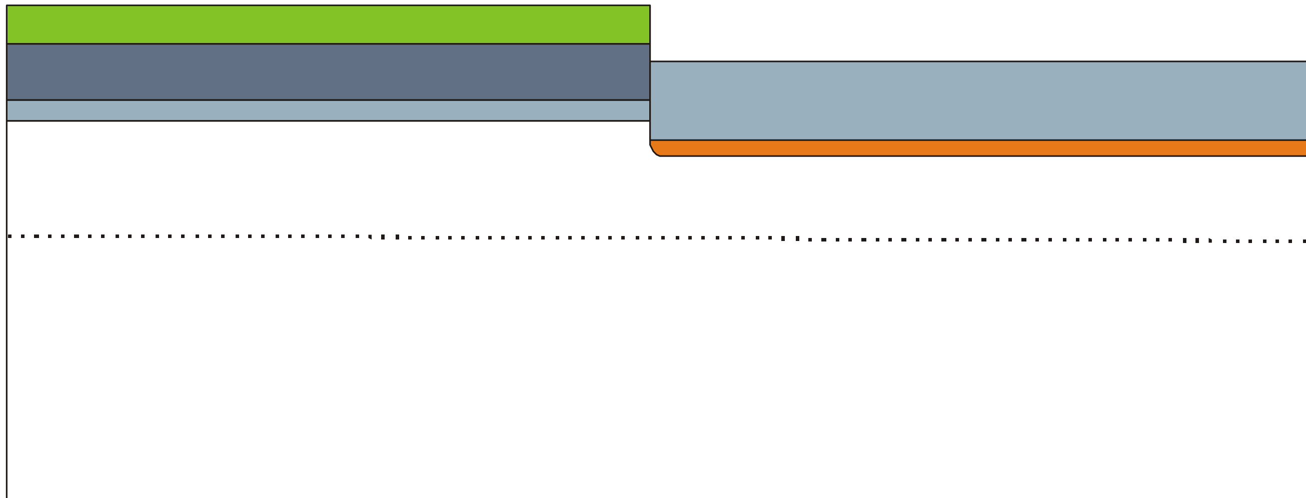
Photoresist Deposition, Projection, Developing and Removal



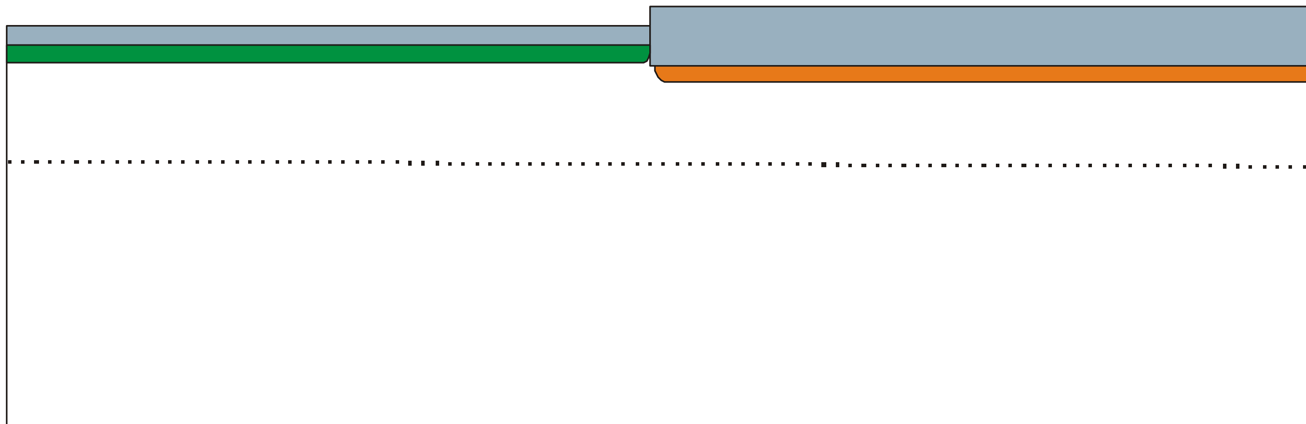
N-Well Implantation



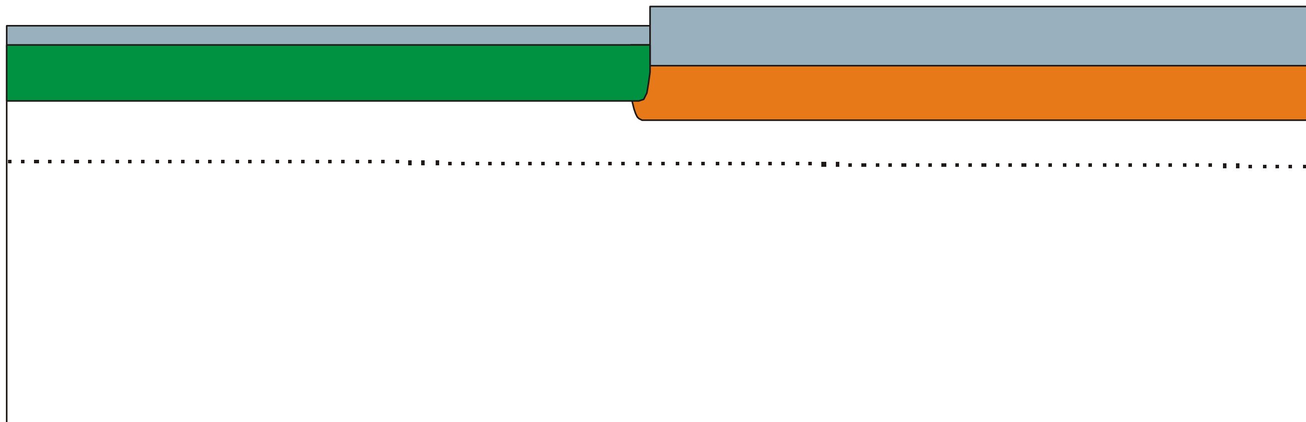
Thick Oxide



P-Well Implantation

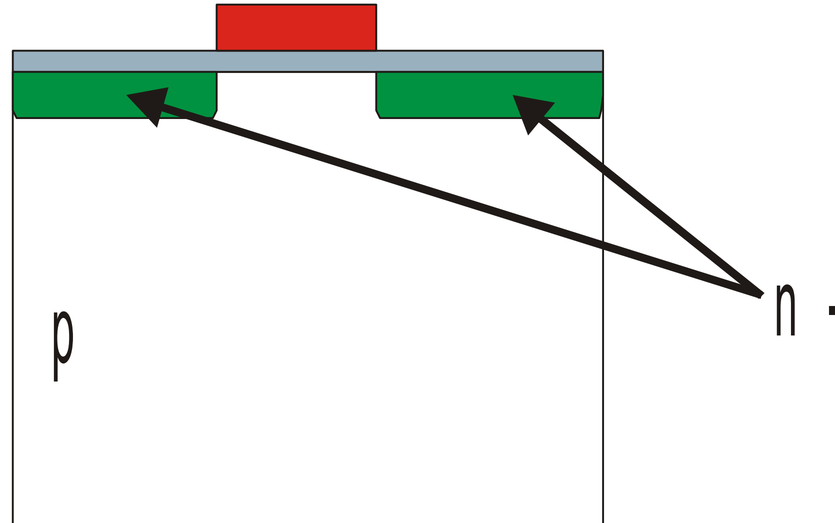


Annealing / Rediffusion

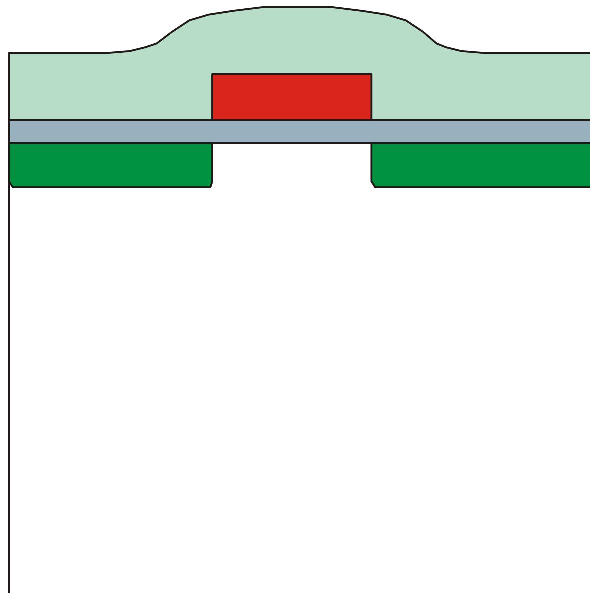


Lightly Doped Drain (LDD) Transistor

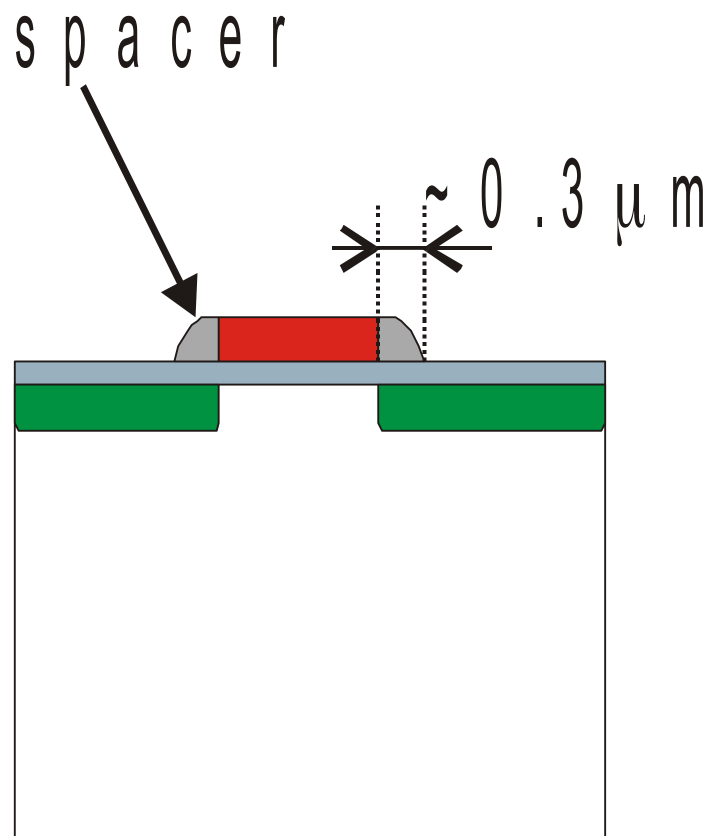
Implantation of Lightly Doped Drain and Source Areas



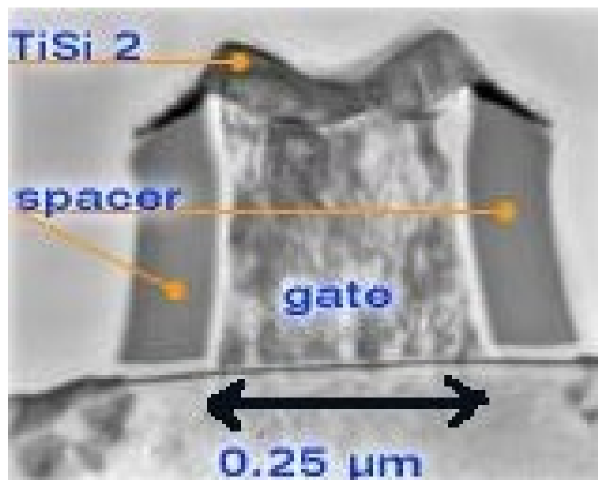
CVD of SiO_2

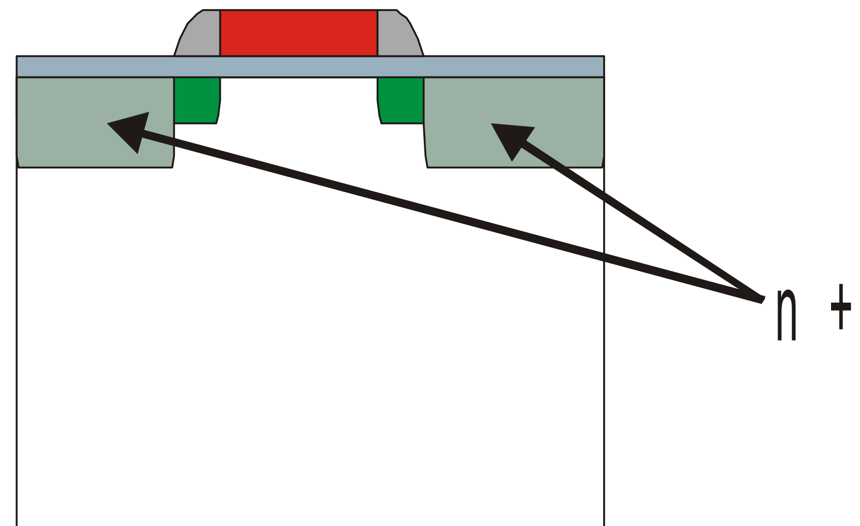


SiO_2 Etch



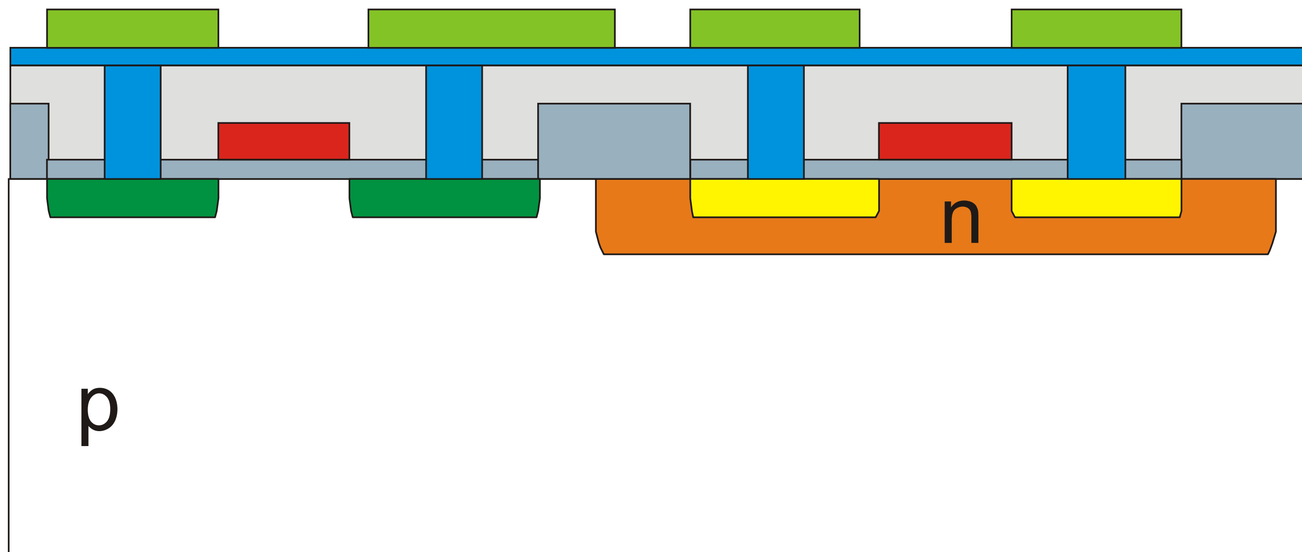
Drain and Source Implantation



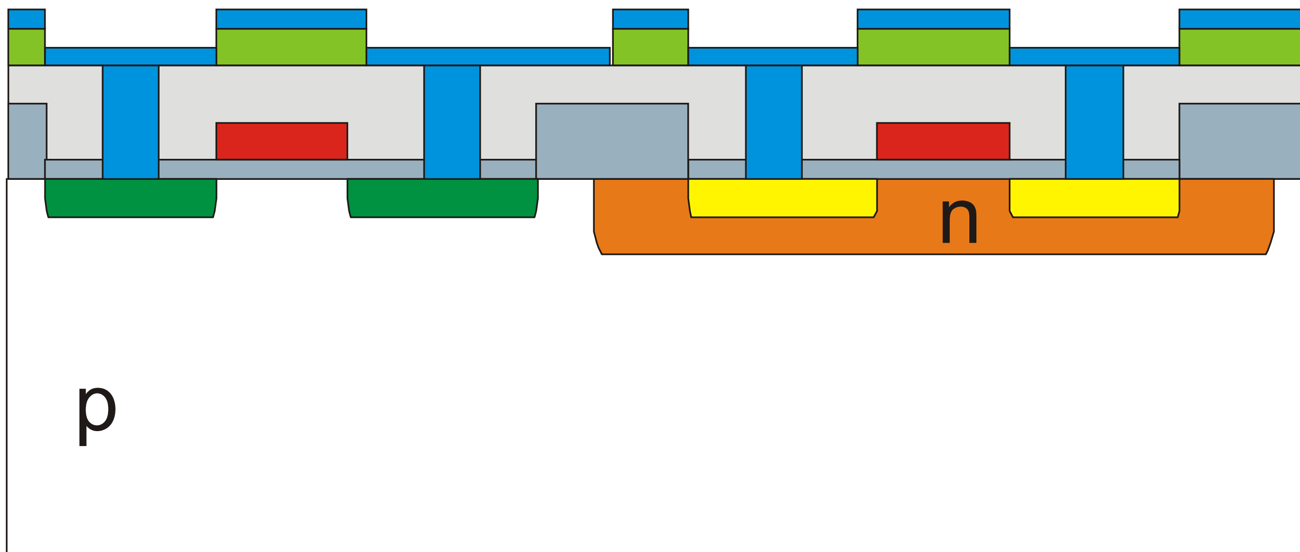


Interconnection Manufacturing

Etching of Surplus Metal



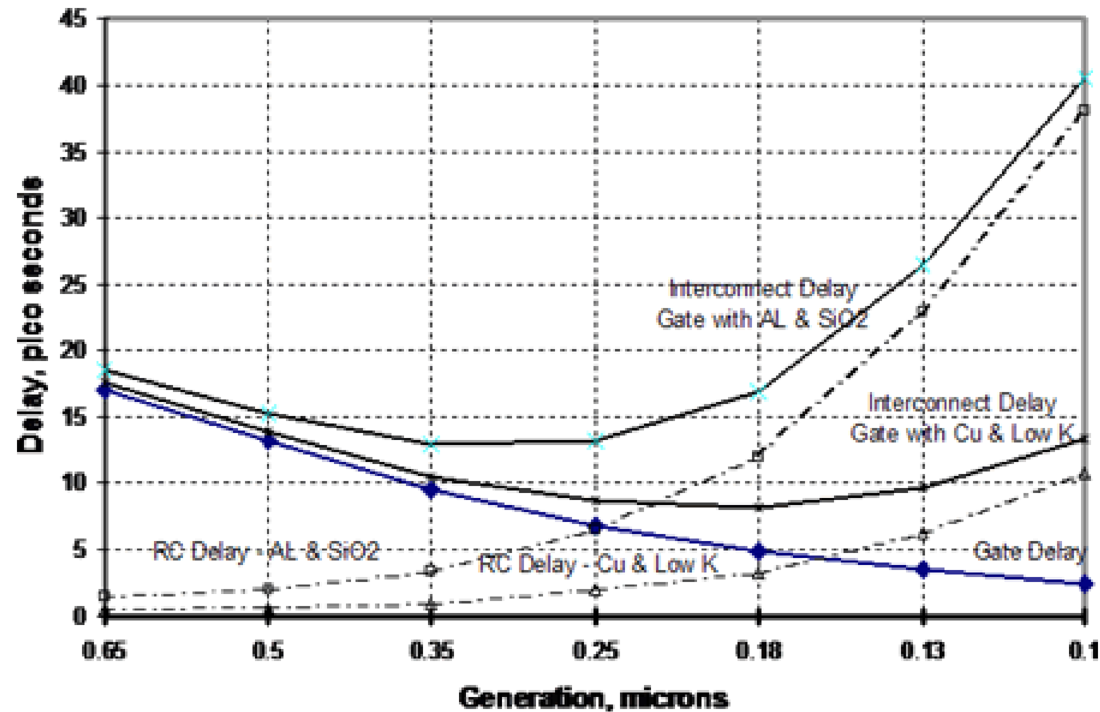
Lift-off



Copper in Interconnection

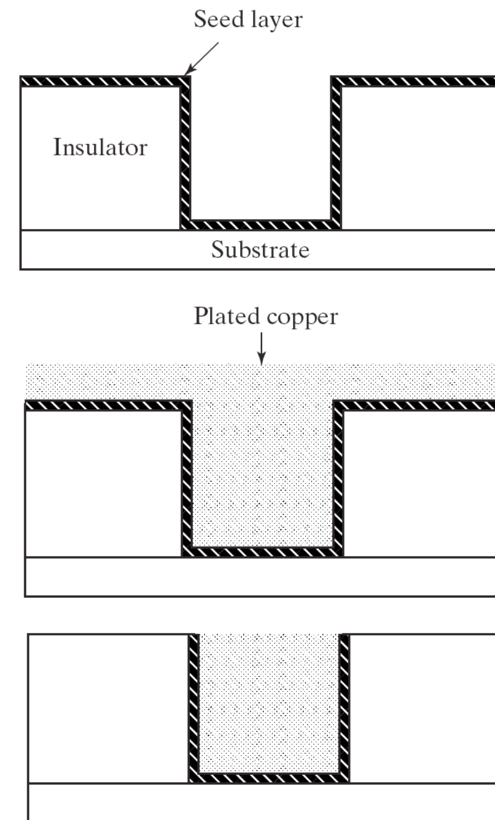
- Conductivity of Cu 50% greater, than Al
- Gives better results as the material for interconnections
- Disadvantages
  - Hard to dry-etch, different methods of manufacturing needed
  - Quickly diffuses in silicon

Interconnection Delay Components



The Damascene Process

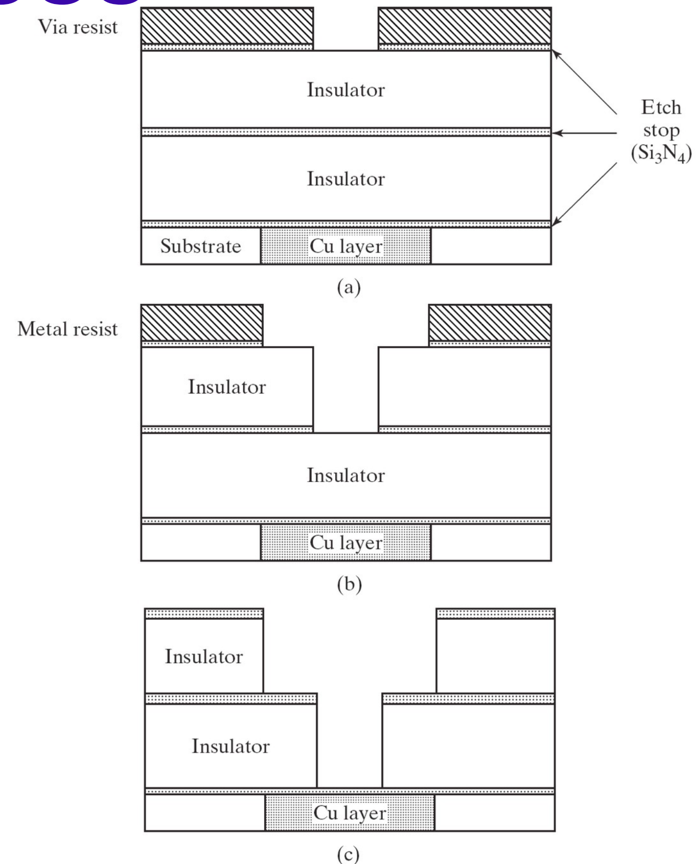
- Process steps:
  - Deposition of insulation
  - Etching of trenches
  - Seed layer deposition (PVD)
  - Electroplating with copper
  - CMP



(b) Copper Damascene process

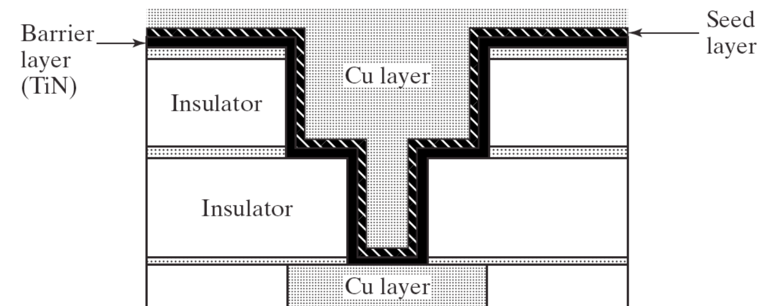
The Double Damascene Process

- Process steps:
  - Deposition of two insulation layers separated by nitride (etch stop)
  - Via mask and etching including the buried nitride layer
  - Metal mask and etching through two insulator layers

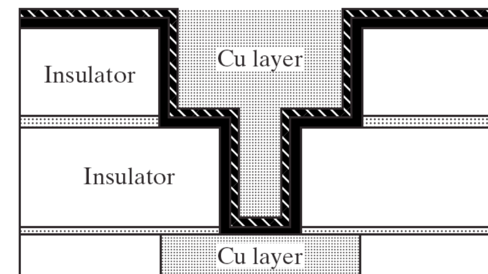


The Double Damascene Process (contd.)

- Then:
  - Deposition of barrier layer (TiN)
  - Deposition of metal (PVD)
  - Electroplating
  - CMP

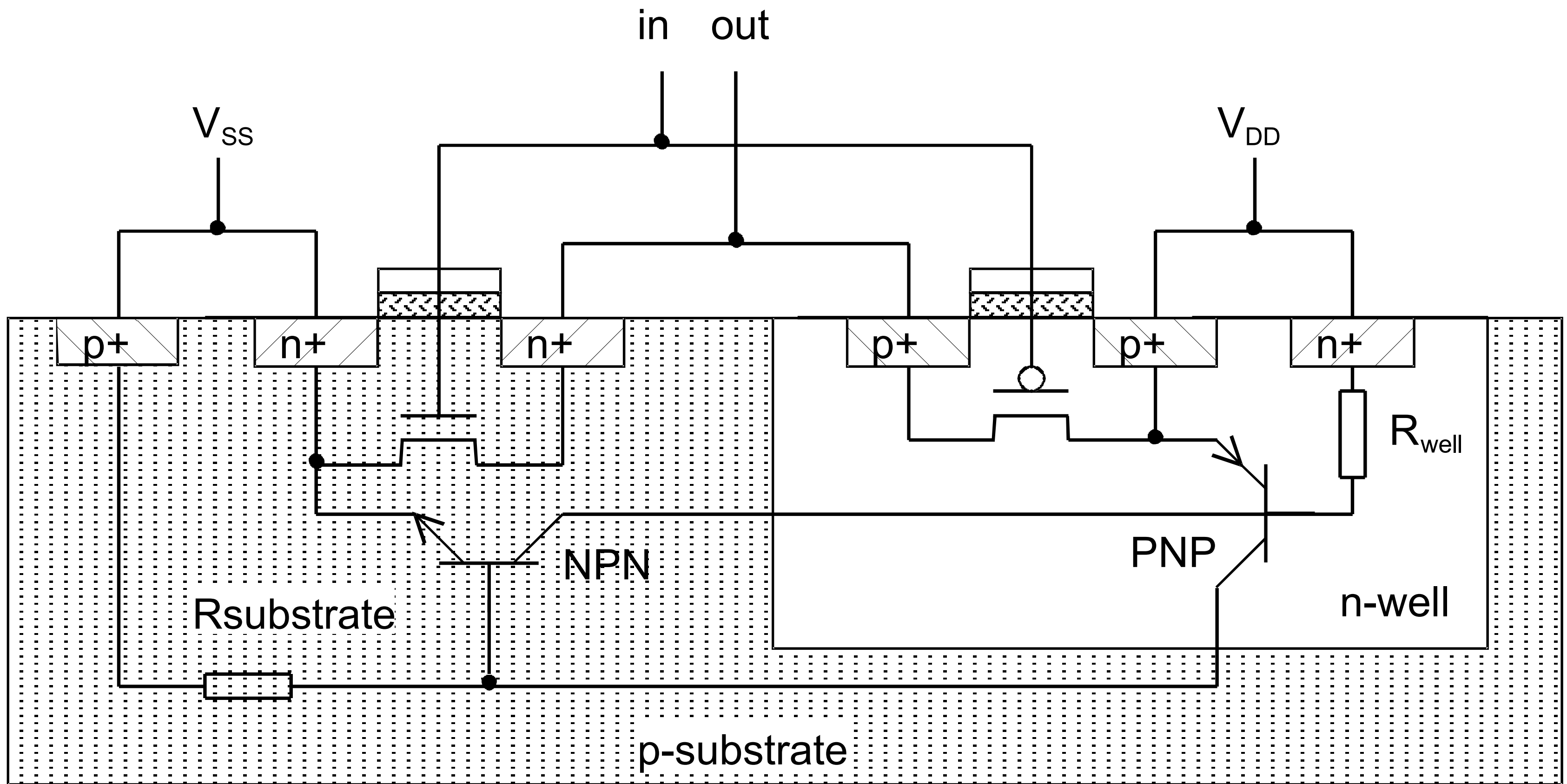


(d)

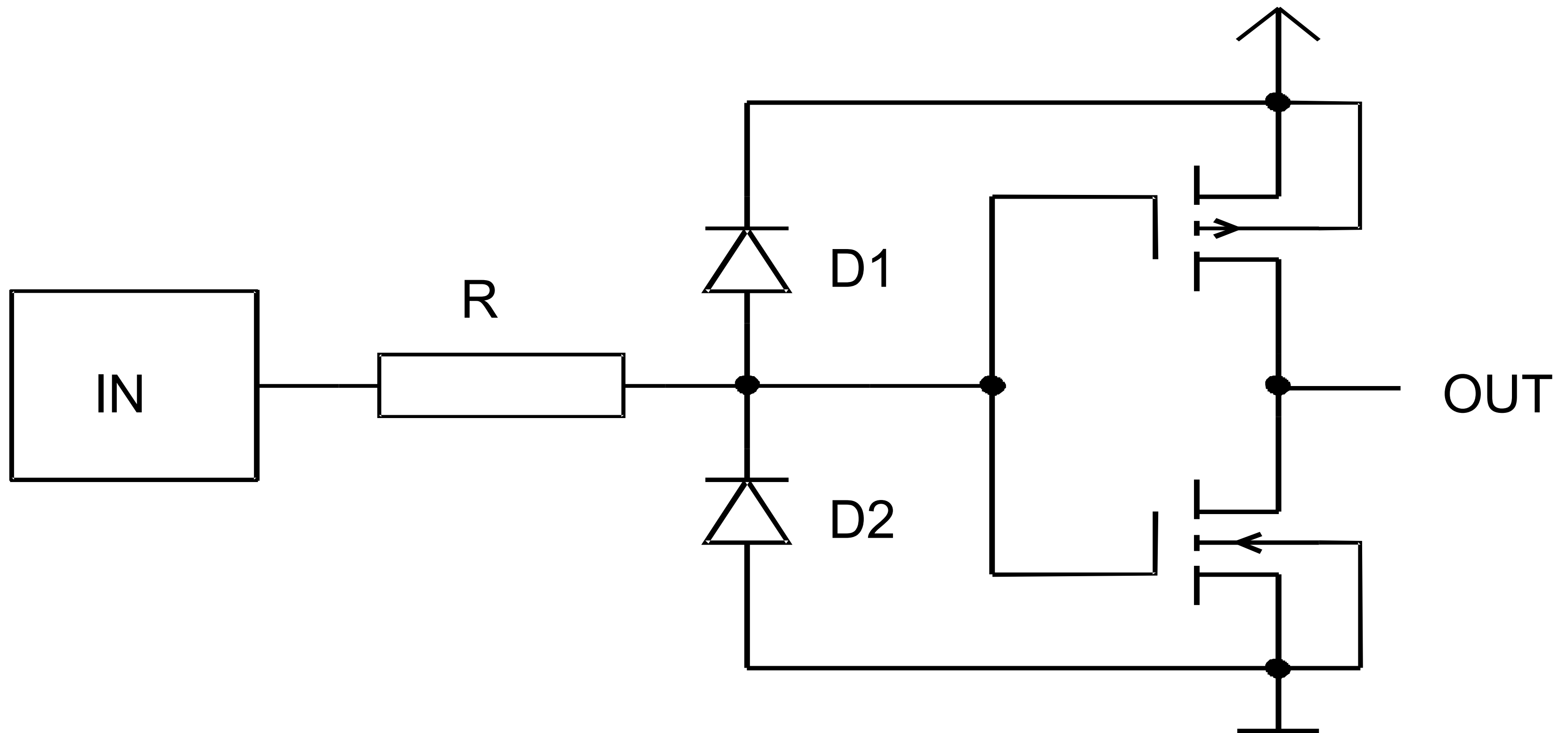


(e)

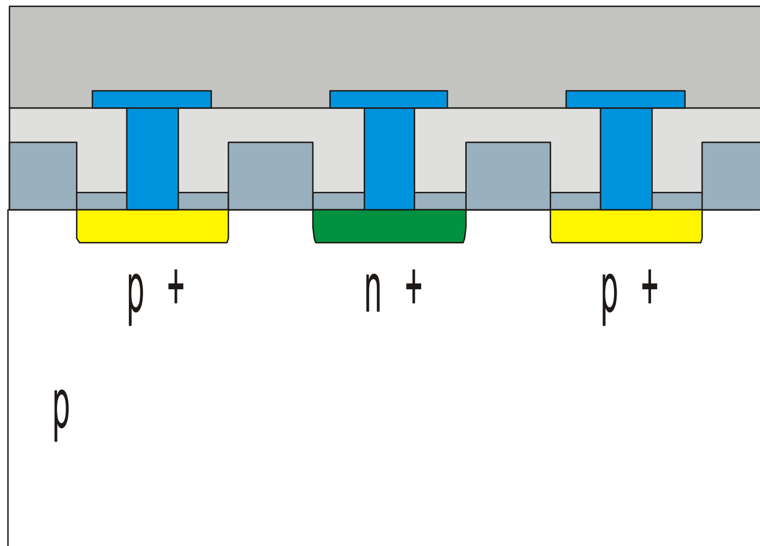
Latch-up

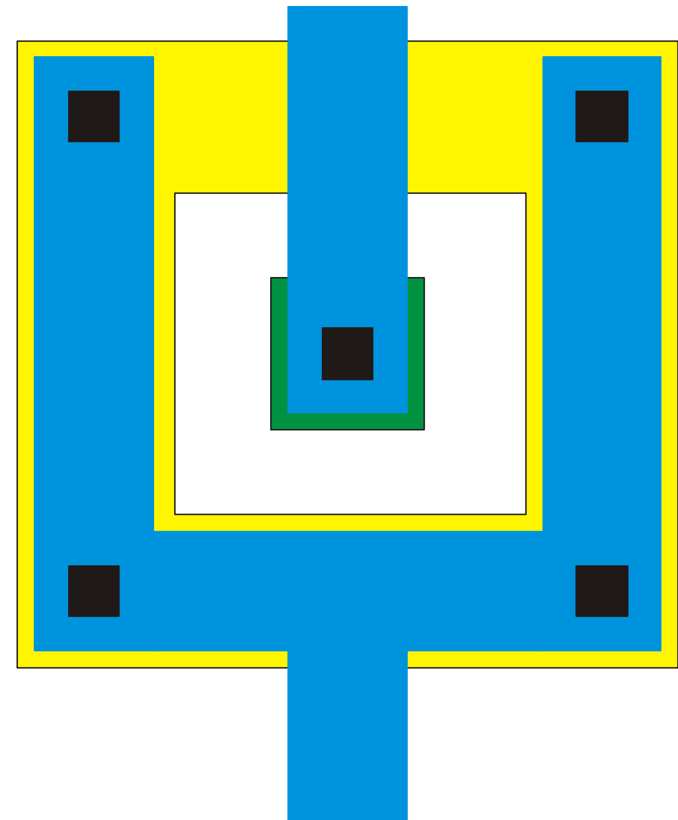


Input Protection Circuit

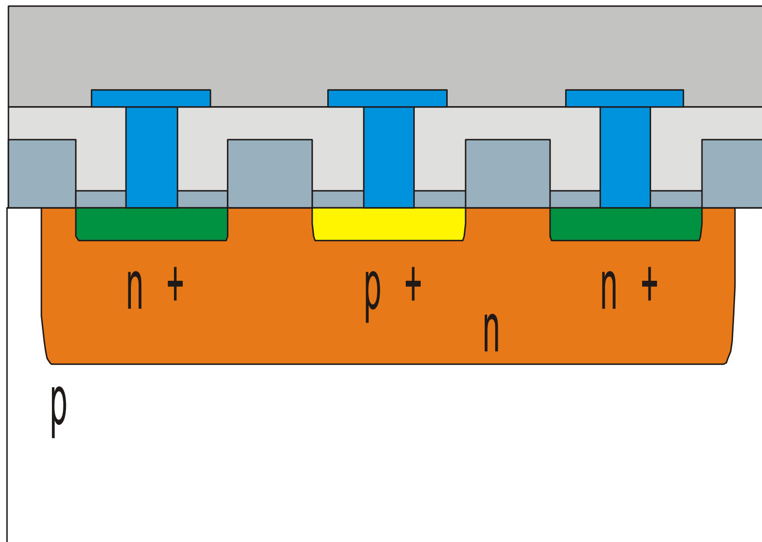


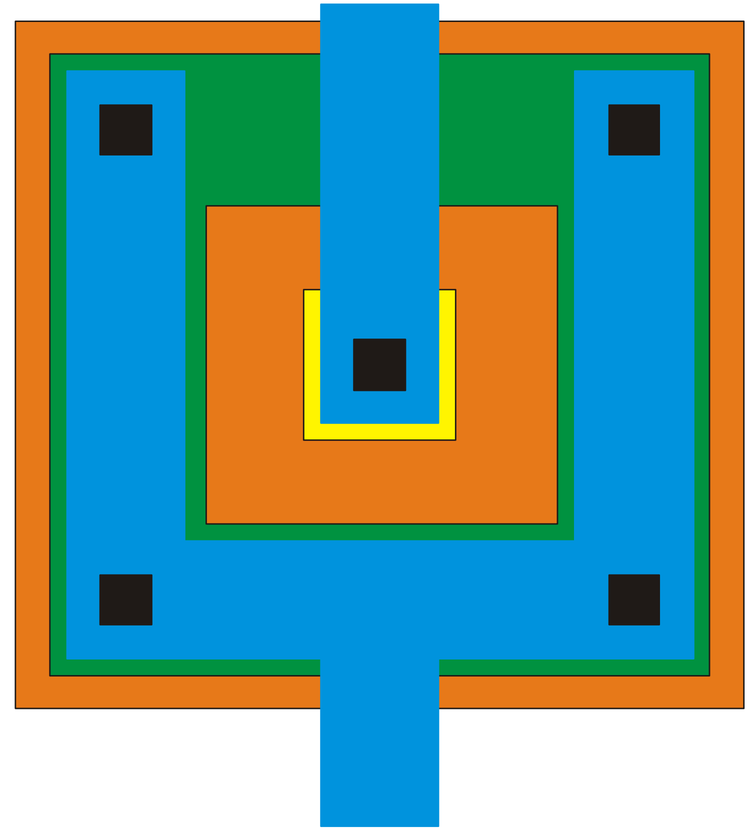
n+/p Diode



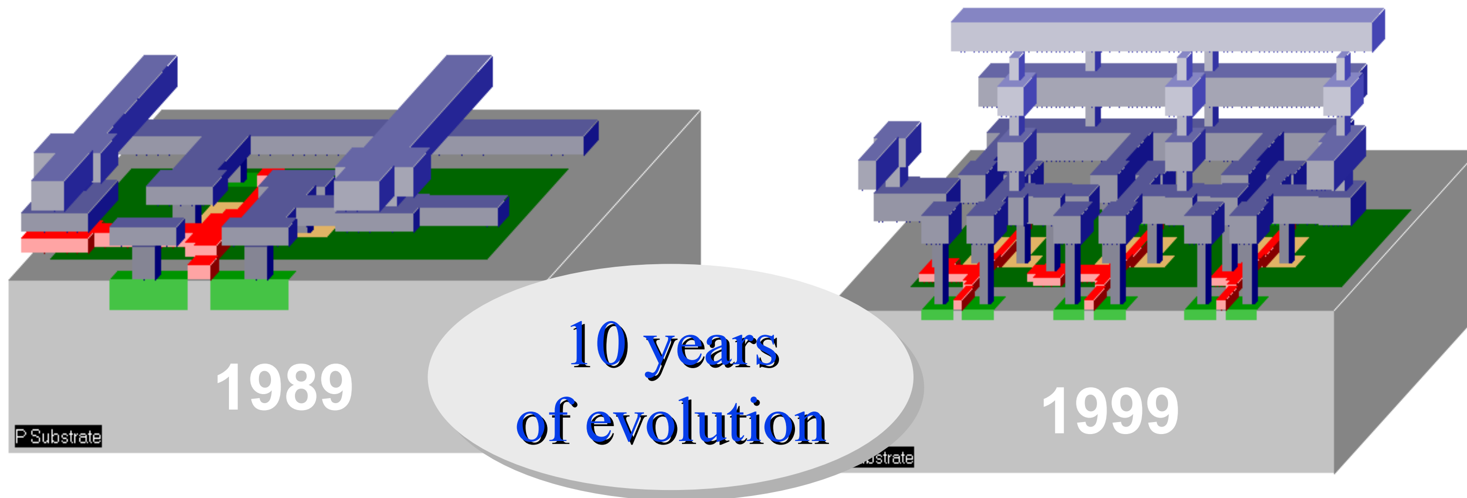


p+/n Diode





Technological Advances



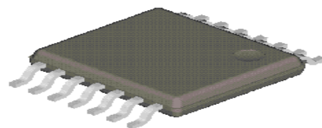
0.7μm technology

- 0.7μm, 2 metal levels
- over 100,000 transistors/die
- clock frequency: 50MHz

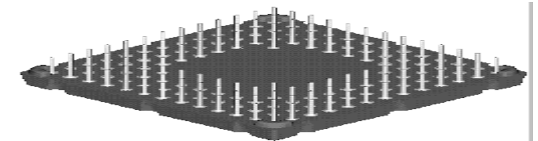
0.18μm technology

- 0.18μm, 6 metal levels
- over 10,000,000 transistors/die
- clock frequency: 500MHz

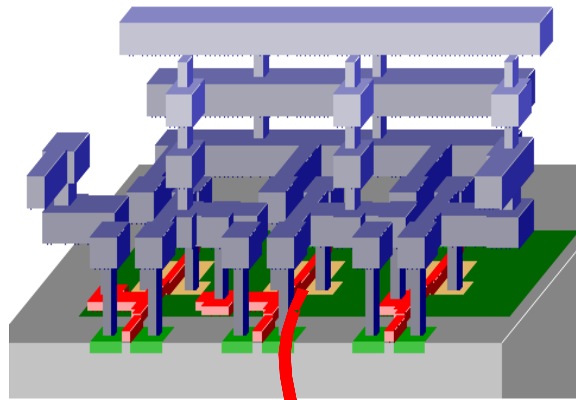
40 pins



512 pins

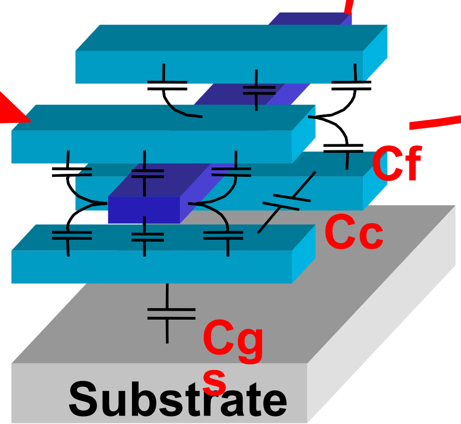


Interconnection modelling

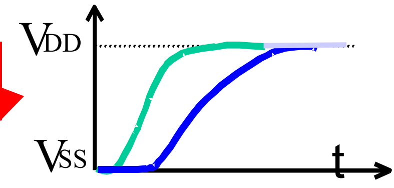


Extraction

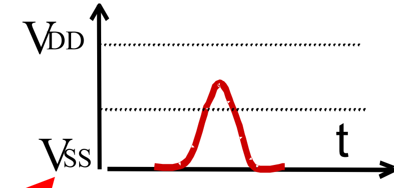
resistance
capacitance
inductance



Simulation



Propagation delay

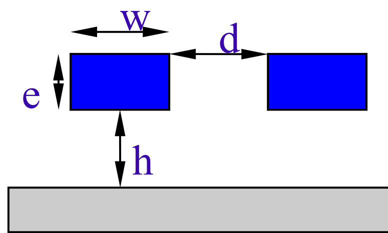


Crosstalk noise

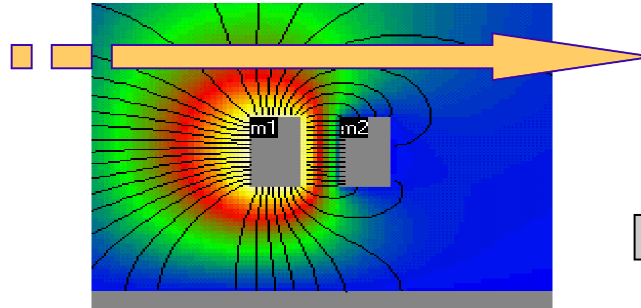
Mathematical models

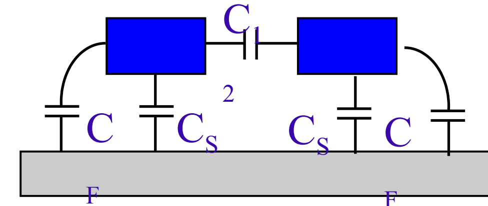
Interconnection modelling

- **Field approach**



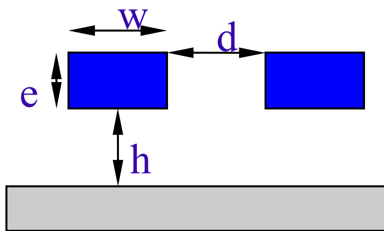
Geometry



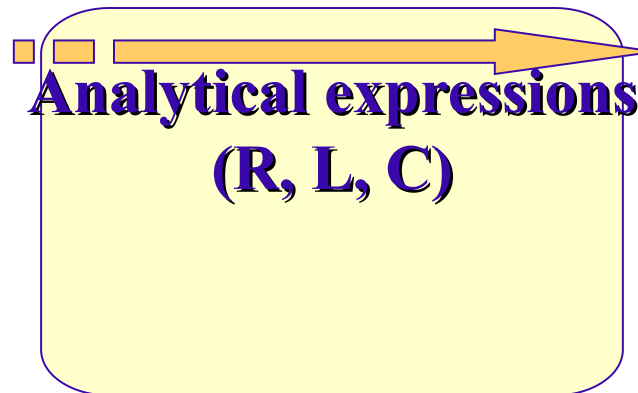


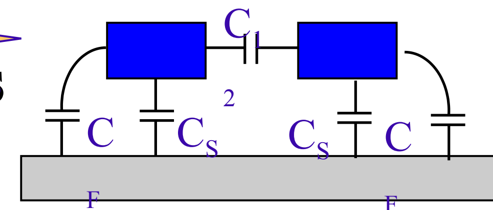
Interconnection parameters

- **Analytical approach**



Geometry





Interconnection parameters