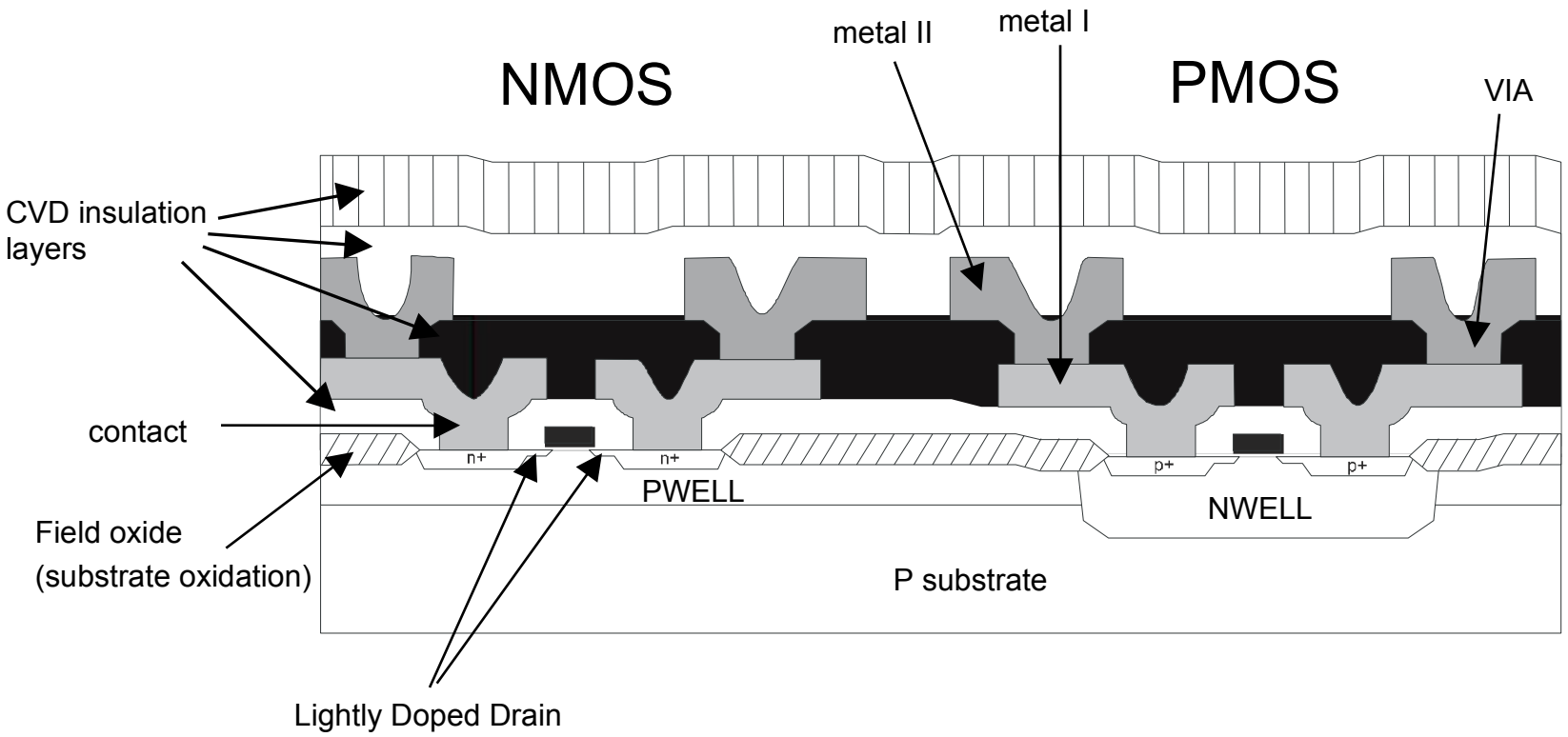
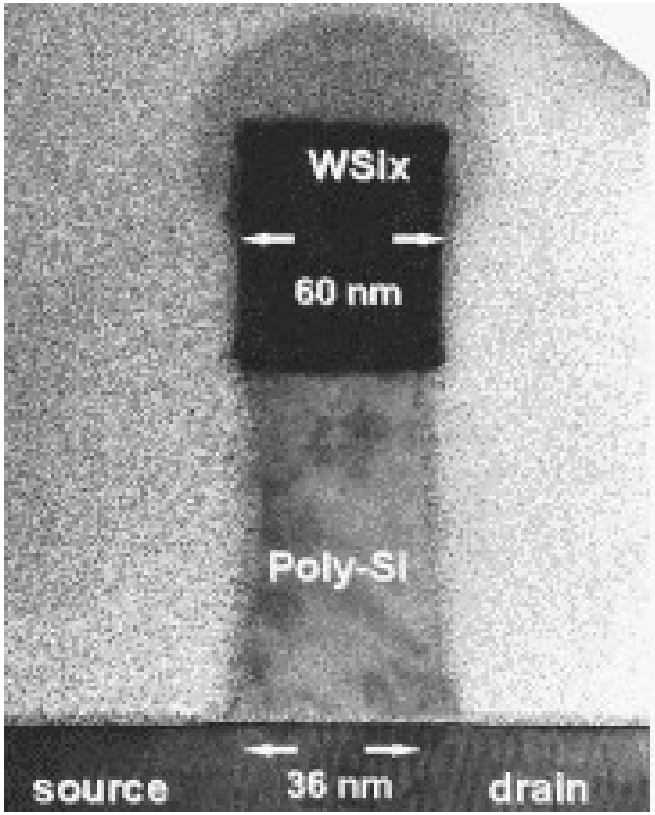
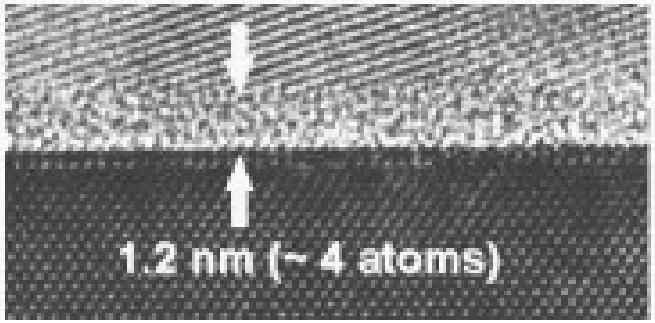
The CMOS Structure



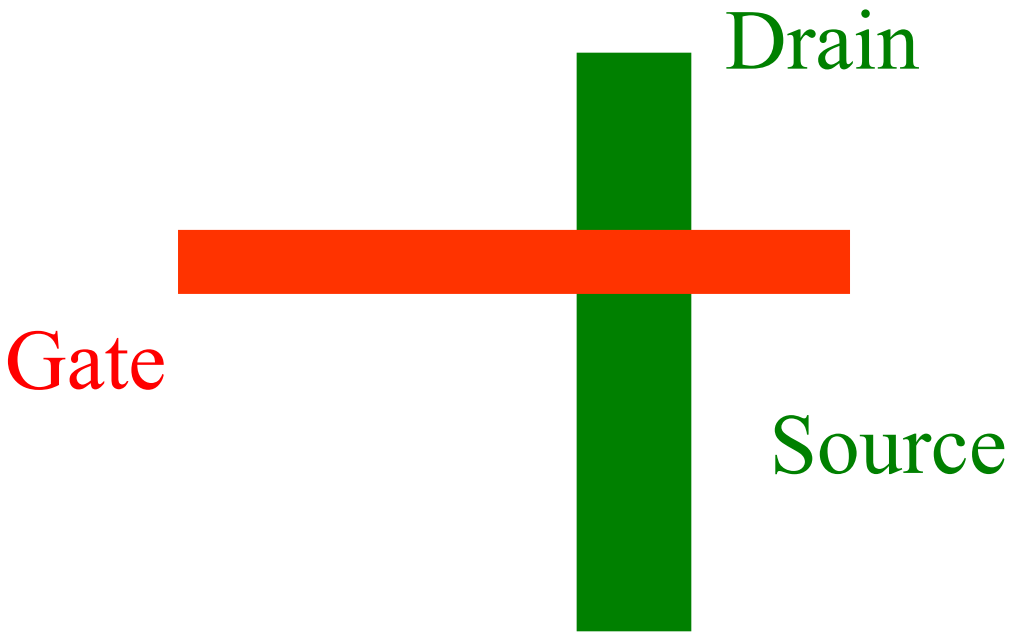
The MOS Transistor

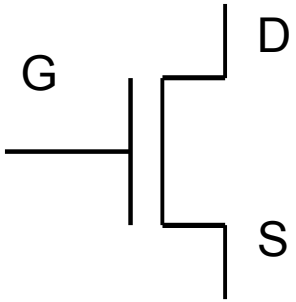




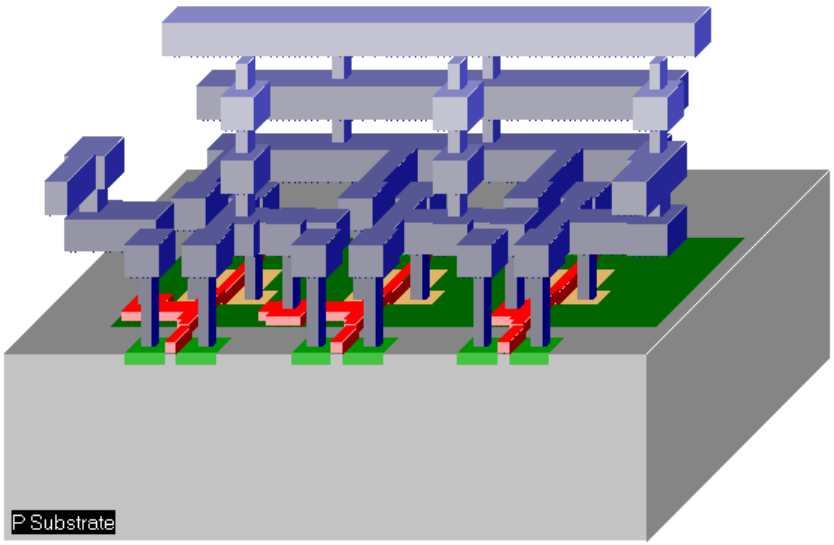
The MOS Transistor

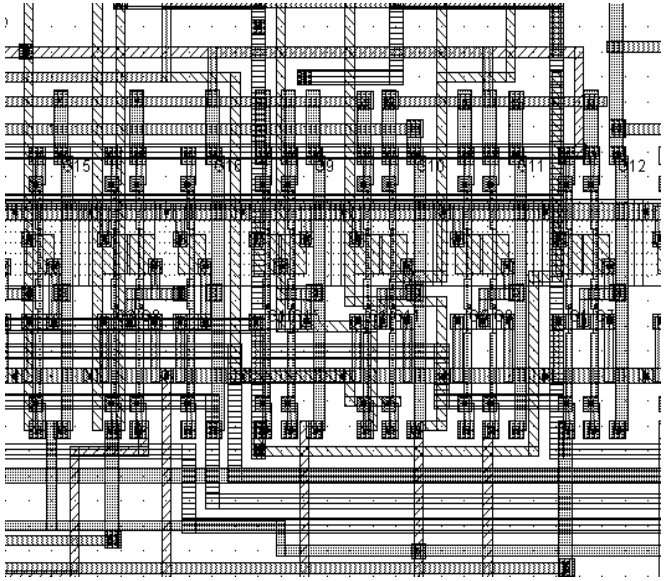
appears in an integrated circuit everywhere at the cross-section of polysilicon and diffusion



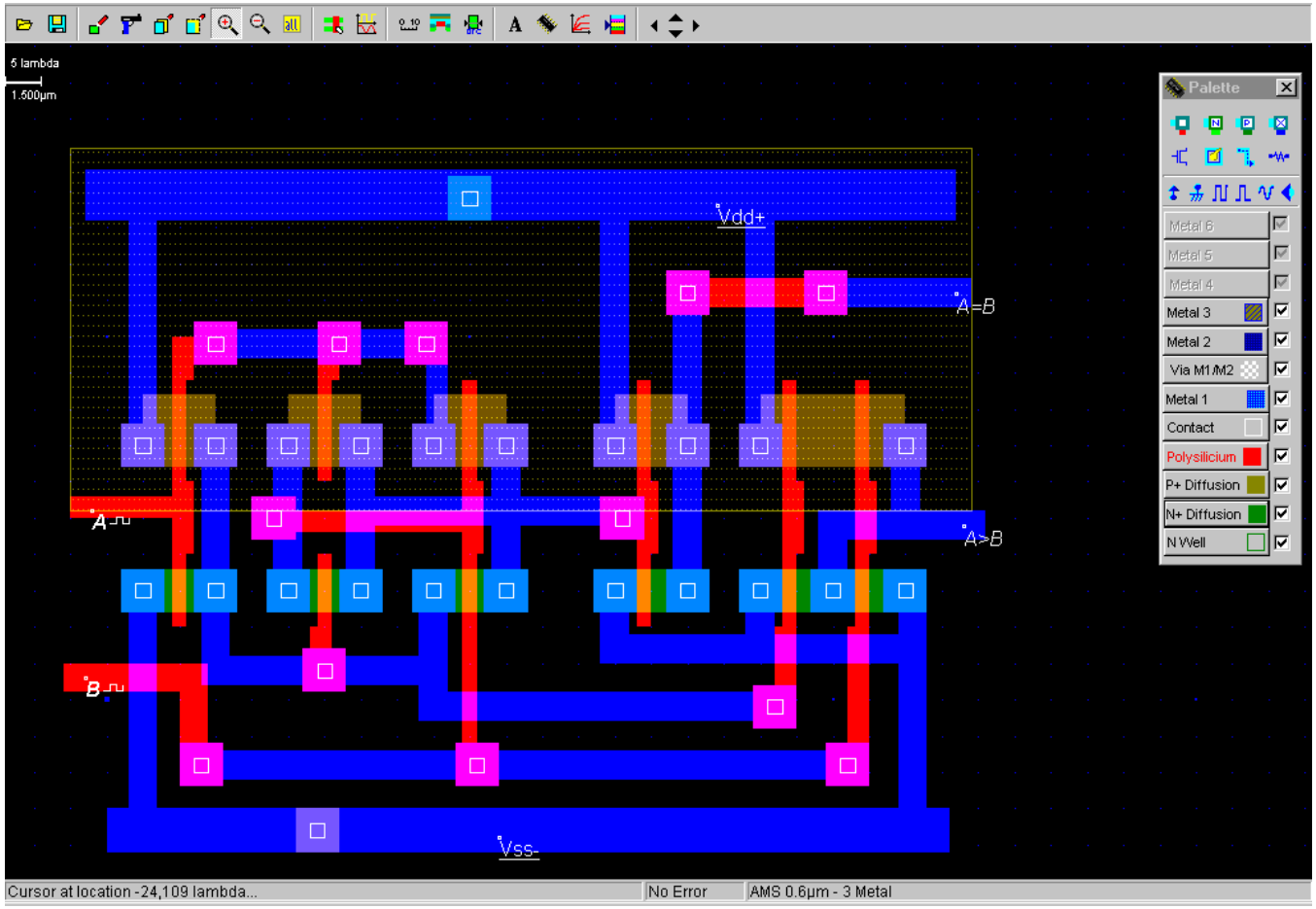


The masks are the stencils, which allow to replicate the ciruit structure over the entire surface of a silicon wafer



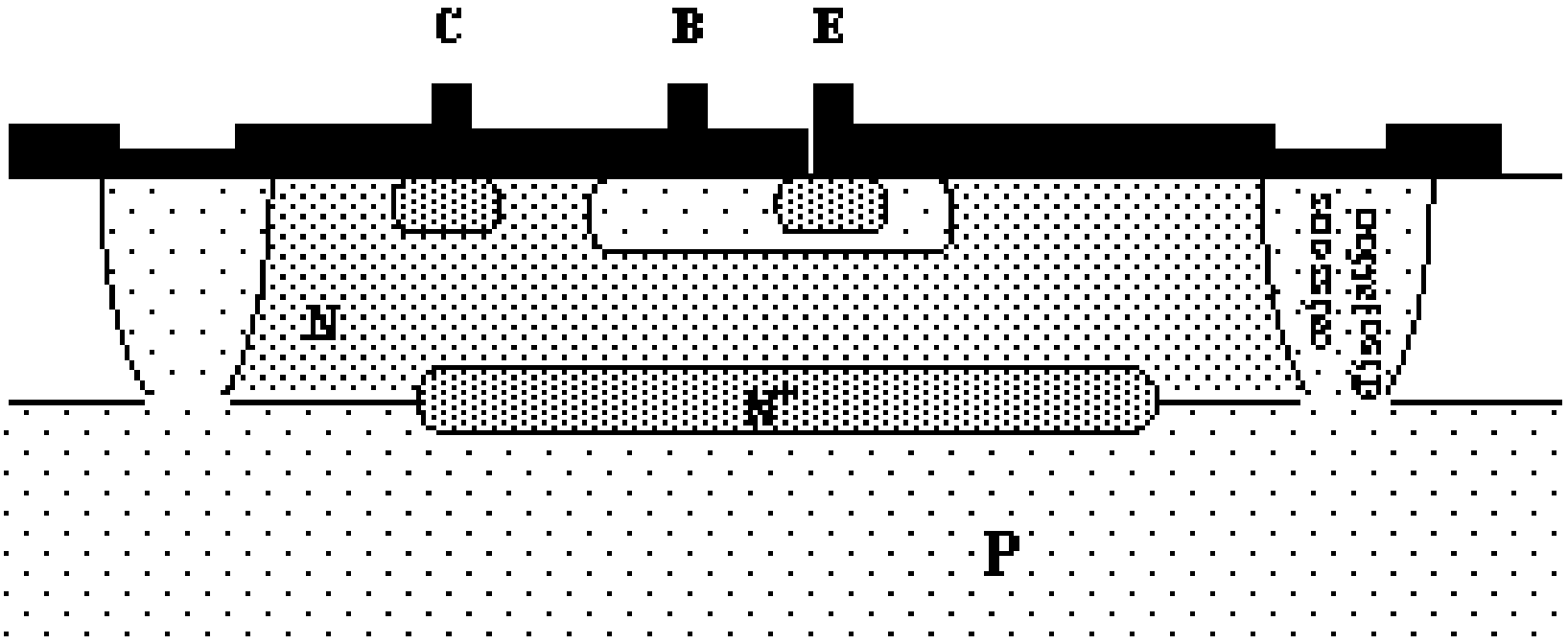


IC Layout Design in Microwind2



Planar technology

All device pins placed at the single flat surface of a silicon die



Technological Operations

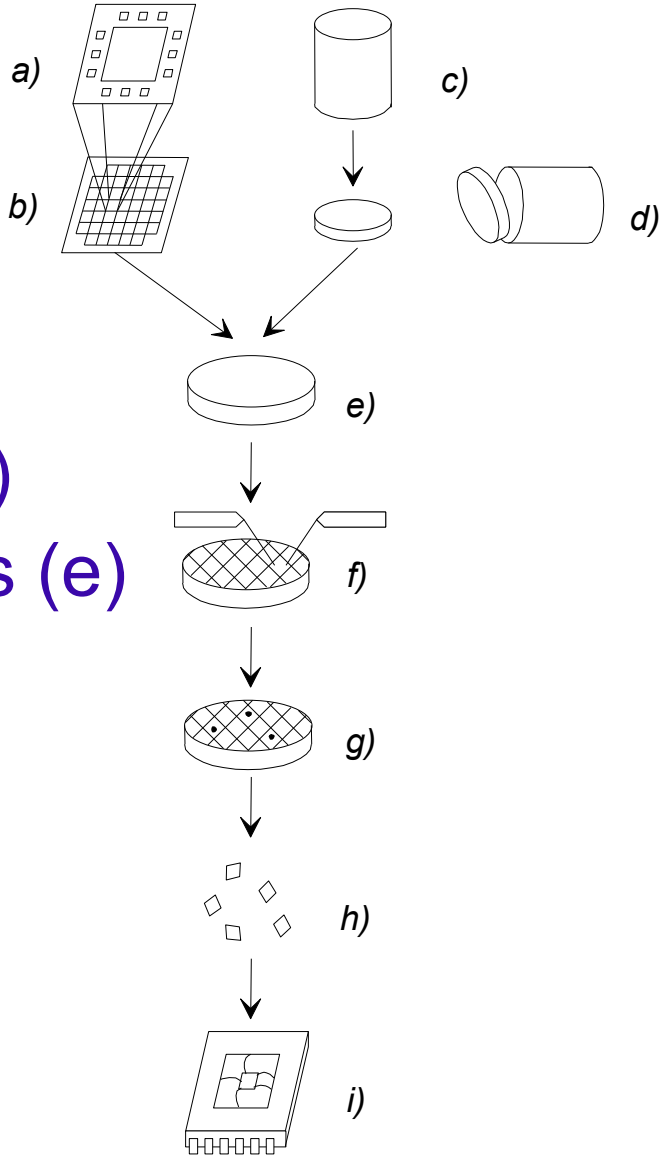
initial oxide
first nitride deposition
NTUB mask
well etch (nitride)
NTUB implant
well oxidation
self aligned P-well implant
well drive-in
pad oxide
second nitride deposition
active area mask
active area etch (nitride)
N-field mask
N-field implant
field oxide
sacrificial oxide
Vt adjust implant
gate oxide
poly1 deposition

high-resistive implant
high-resistive mask
poly1 doping
capacitor oxide
poly2 deposition
poly2 doping
poly2 mask
poly2 etch
poly1 mask
poly1 etch
N-LDD mask
N-LDD implant
P-LDD implant
spacer formation
N+ implant mask
N+ implant
P+ implant mask
P+ implant
S/D anneal

BPSG deposition/reflow
contact mask
contact etch
plug implant mask
plug implant / anneal
barrier deposition
metal1 deposition
metal1 mask
metal1 etch
IMD / planarisation
via mask
via etch
metal2 deposition
metal2 mask
metal2 etch
passivation deposition
pad mask
pad etch
alloy
back side grinding

Silicon technology

- Mask manufacturing (a,b)
- Silicon wafer manufacturing (c,d)
- Components and interconections (e)
- Wafer probe (f)
- Marking of bad dies (g)
- Die separation (h)
- Packaging (i)
- Final testing



Wafer Manufacturing

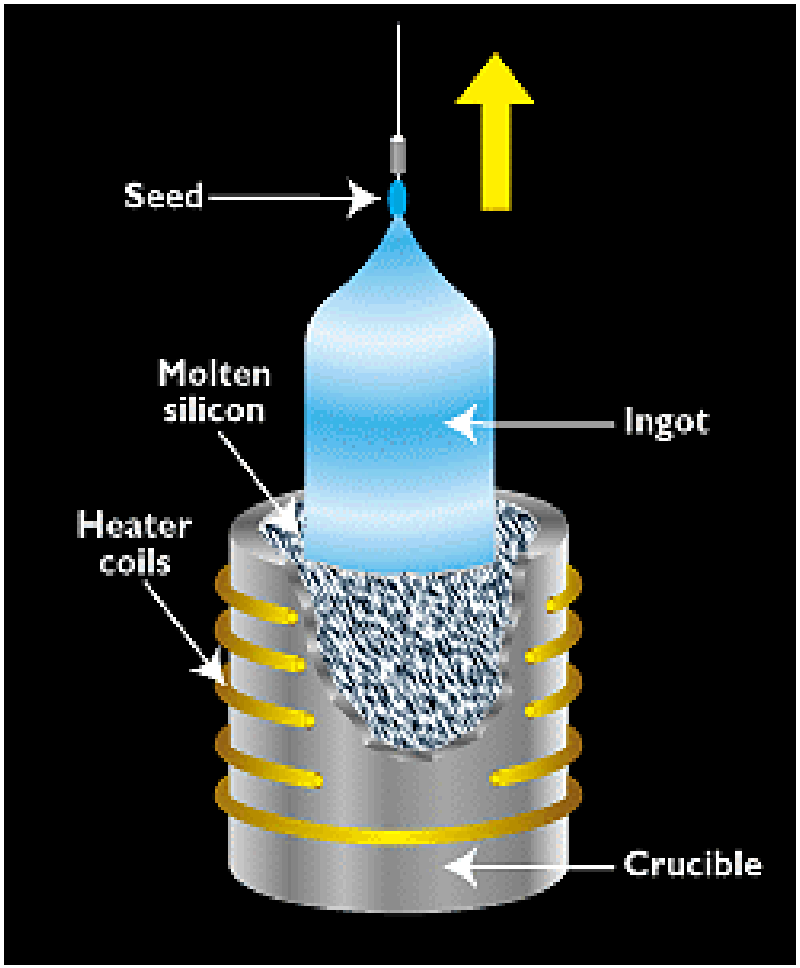
- Polycrystalline silicon
- Monocrystalline silicon
- Slicing
- Chemical and mechanical polishing
- Cleaning
- Testing
- Packaging and shipping

Pure Silicon

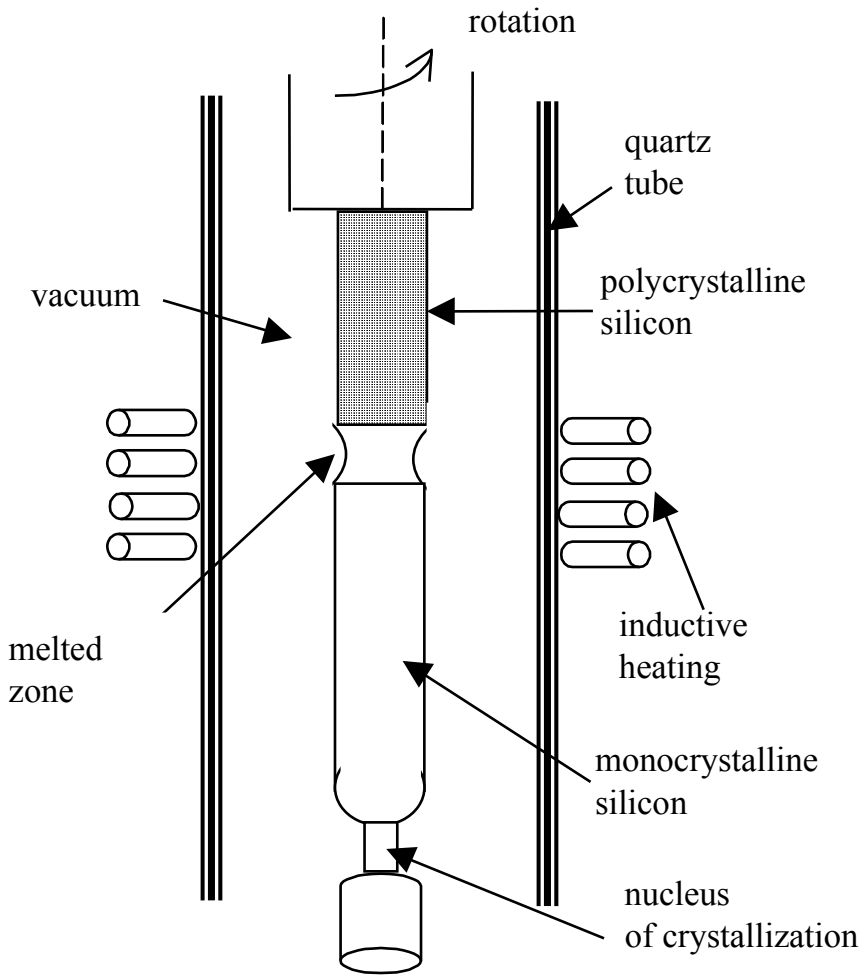
- Impurity concentration less than 10^{13} at/cm^3
- One impurity atom per 10 billion silicon atoms
- 99.9999999% pure silicon

The Czochralski's Method

The Czochralski's Method

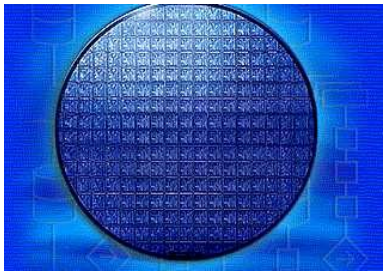


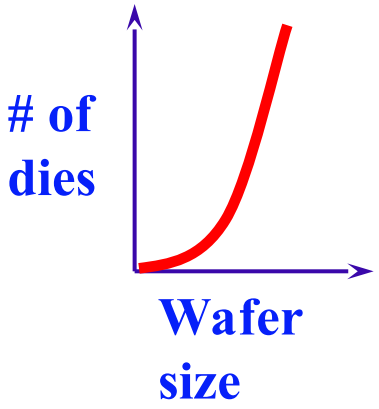
Zone Melting

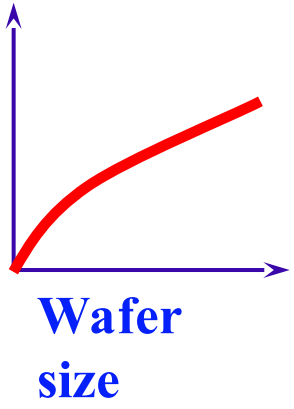


Silicon Wafer Diameter

2” dia. → **12” dia.**





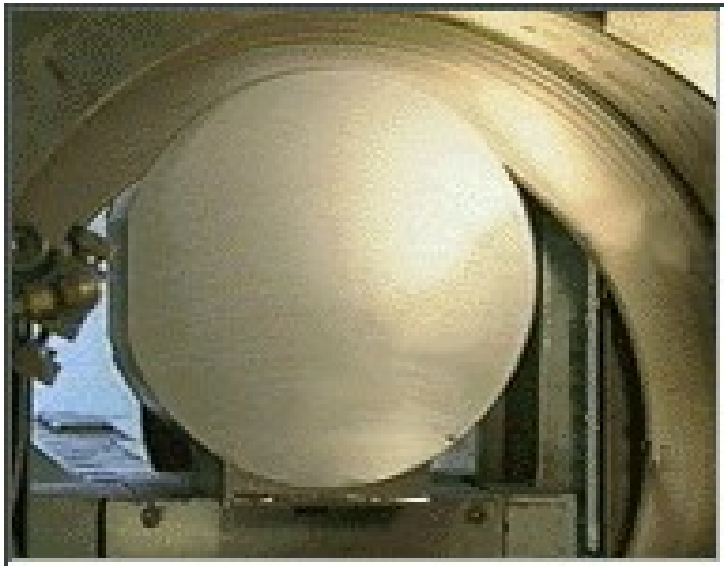


12-Inch Ingot

Weight
up to 300 kg

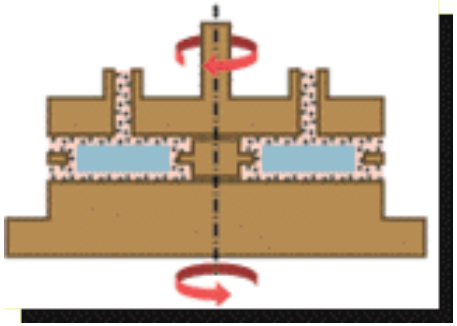
Cutting

Using diamond blade saw into 0.5-1.0 mm wafers.
Wafer surfaces are rough.



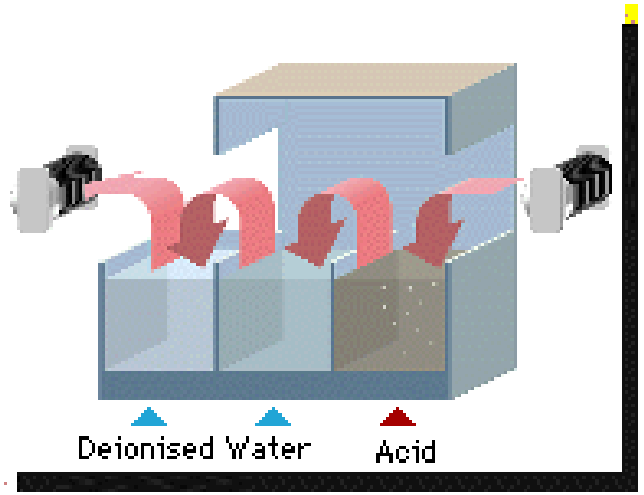
Lapping

- Removal of damaged silicon
- Flattening of the surfaces, needed for photolithography
- Improvement of parallel positioning of wafer surfaces



Chemical Polishing

- **Performed after mechanical polishing in order to remove microcracks and other mechanical damage.**
- **Etching in mixture of nitric and acetic acid or sodium hydroxide.**

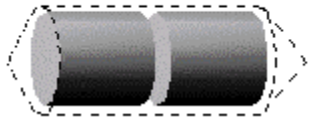


1. Polycrystalline Silicon

2. Crystal Growth

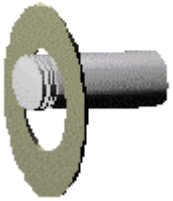
3. Single Crystalline Silicon Ingot

4. Shaping



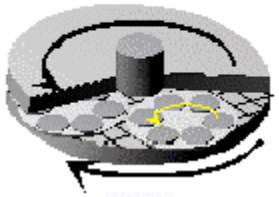
5. Single Crystalline Silicon Ingot

6. Slicing

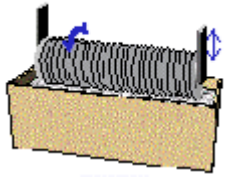


7. Edge Rounding

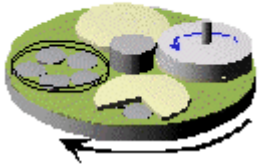
8. Lapping



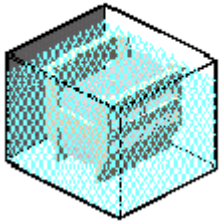
9. Etching



10. Polishing



11. Cleaning



12. Inspection

13. Packaging

14. Shipping

Manufacturing of Components and Interconnections

- Change of material properties or deposition of a new layer
- Photolithography
- Etching

Change of Material Properties

- Doping by diffusion
- Doping by ion implantation
- Substrate oxidation

Doping by Diffusion

Diffusion: movement of atoms in crystal lattice caused by concentration gradient

- Temperature: 800 - 1200°C
  the higher the temperature, the faster the diffusion
- Boron, phosphorus or arsenic from gaseous phase
- Vertical and lateral diffusion

Two Types of Diffusion

depending on the method of supply of impurity atoms (boron, phosphorus or arsenic from gaseous phase)

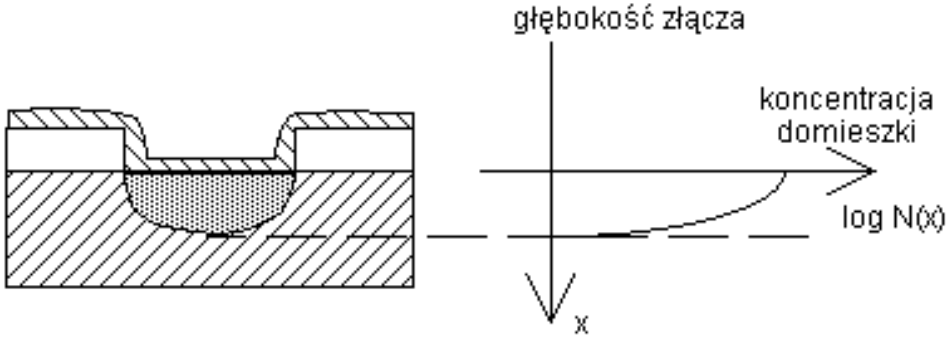
- **Infinite source**

  continuous, unlimited supply of dopant atoms to the substrate surface, resulting in the constant dopant concentration at the surface.

- **Finite source**

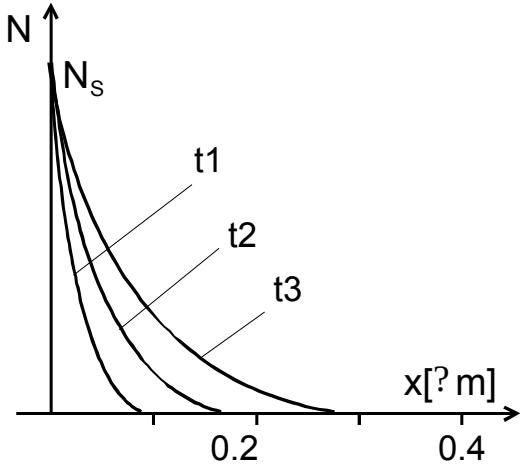
  total number of dopant atoms in the substrate and at the surface is constant, atoms diffuse from the surface into the interior.

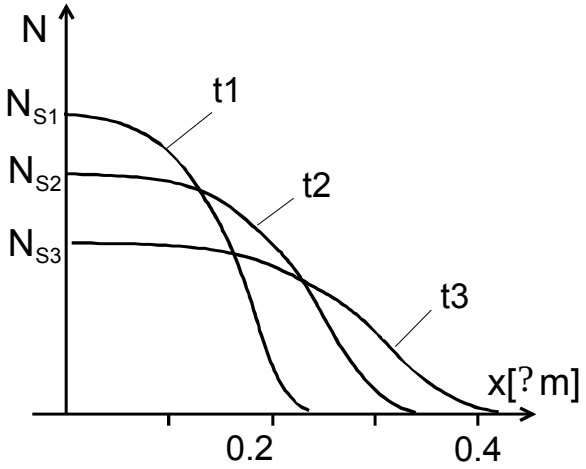
Doping Profile



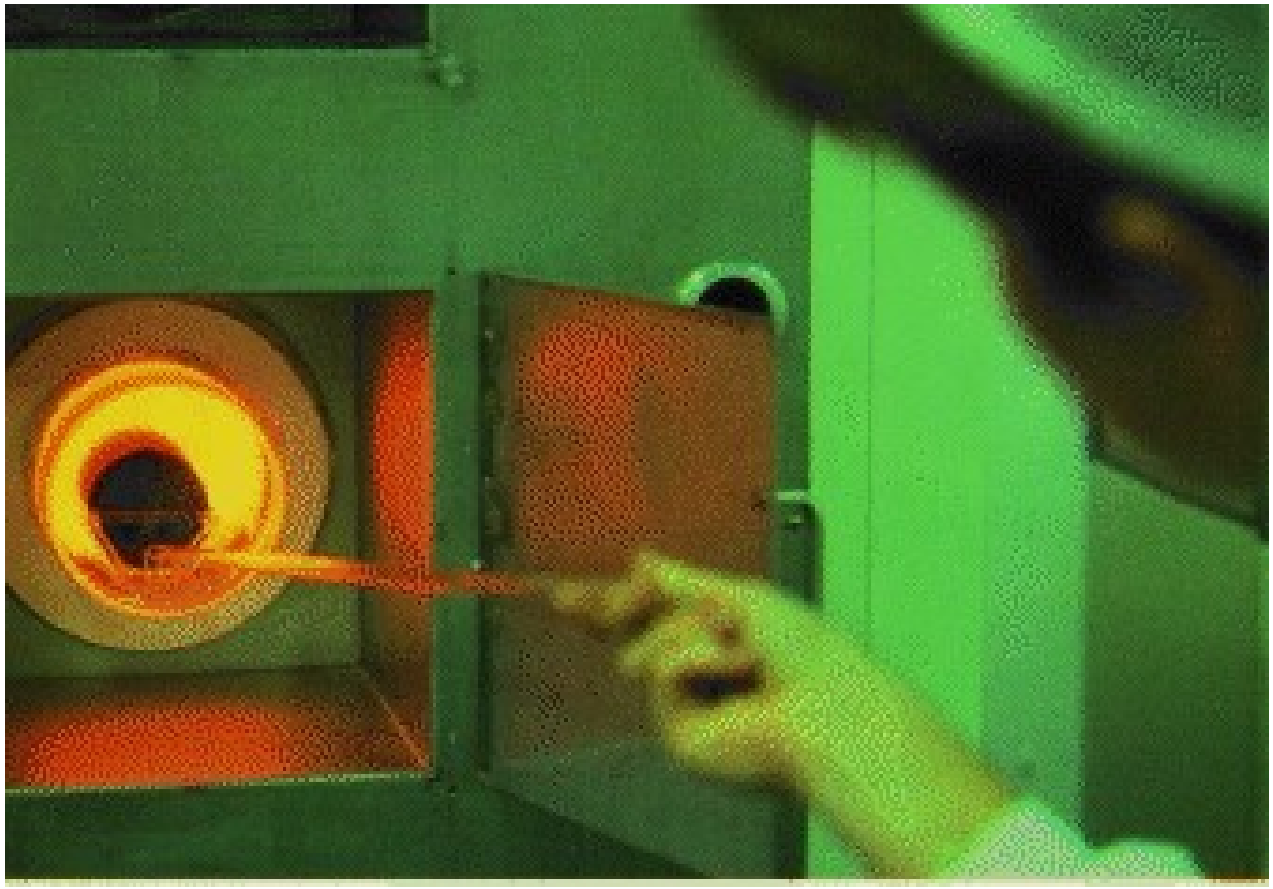
Diffusion from

unlimited source **limited source**





Diffusion Furnace



Doping by Ion Implantation

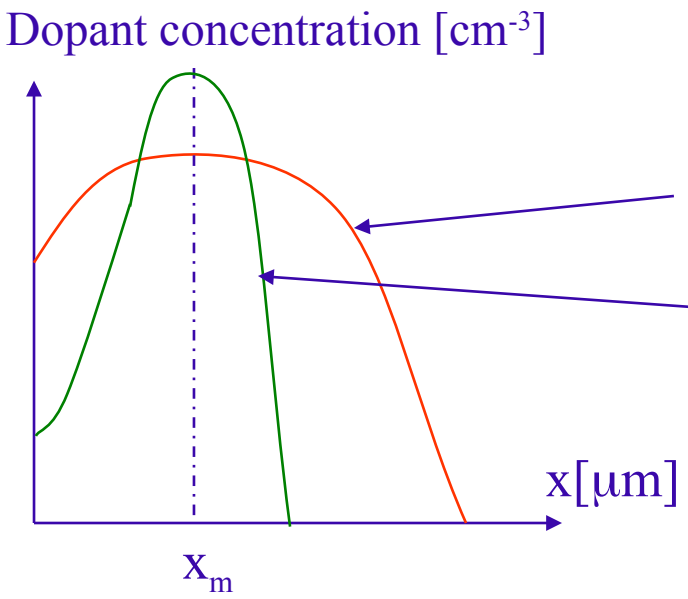
Shooting with dopant ions accelerated in electric field into the substrate

- **Ion energy: several hundred of keV**
- **Narrow doping profile**
- **Crystalline lattice is damaged**
- **Necessity of annealing and rediffusion**
- **High dose accuracy**

Implantation Is Influenced by:

- **Ion mass**
- **Ion energy**
- **Crystallographic orientation of the substrate with respect to the ion beam**

Annealing and Rediffusion



Doping profile

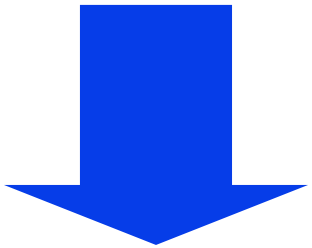
After rediffusion

Before rediffusion

The type and energy of ions determine the average penetration distance and doping profile (~ Gaussian)

The Ion Implanter

SiO2 Layers Manufacturing



Oxidation 

- Thermal dry
- Thermal wet

CVD - insulation layers placed apart from the substrate

Substrate Oxidation

Oxide thickness [nm]	Purpose	Method of manufacturing
2 - 6	tunelling oxides	dry oxidation
15 - 50	gate and capacitor oxides	dry oxidation
20 - 50	LOCOS pad oxides	dry oxidation
200 - 500	masking and passivation oxides	wet oxidation or CVD
300 - 1000	field oxides	wet oxidation

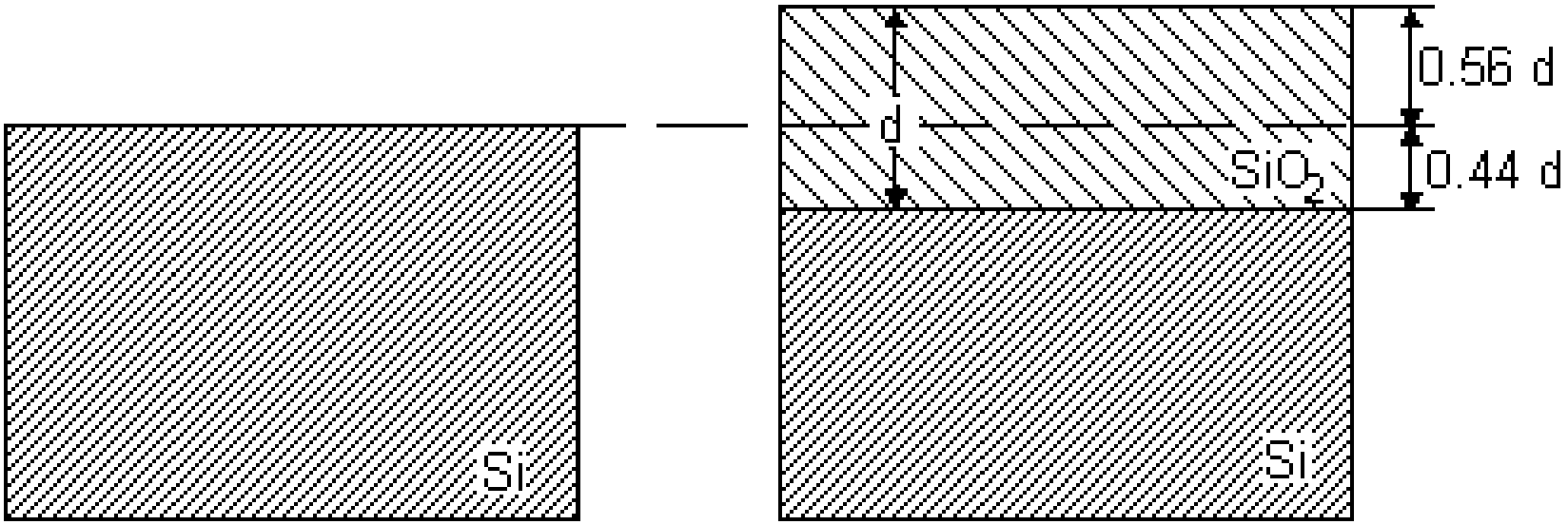
Substrate Oxidation

- Temperature: 950 - 1150°C
- "Eating-up" of the substrate (44% of oxide thickness)
- Speed depends on pressure and temperature
- Dry or wet:

$$Si + O_2 \rightarrow SiO_2$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

"Eating-up" of The Substrate



Deposition of New Layers

- Chemical Vapour Deposition (CVD)
  - Low Pressure CVD
  - Plasma Enhanced CVD
- Physical Vapour Deposition (PVD)

Chemical Vapour Deposition

- Epitaxy

  $SiCl_4 + SiH_4(silane) \rightarrow 2Si + 4HCl$

  950 - 1250 ˚C

  $SiCl_4 + 2H_2 \rightarrow Si + 4HCl$

- Policrystalline silicon
- Silicon nitride $3SiH_4(silane) + 4NH_3 \rightarrow Si_3N_4 + 12H_2$

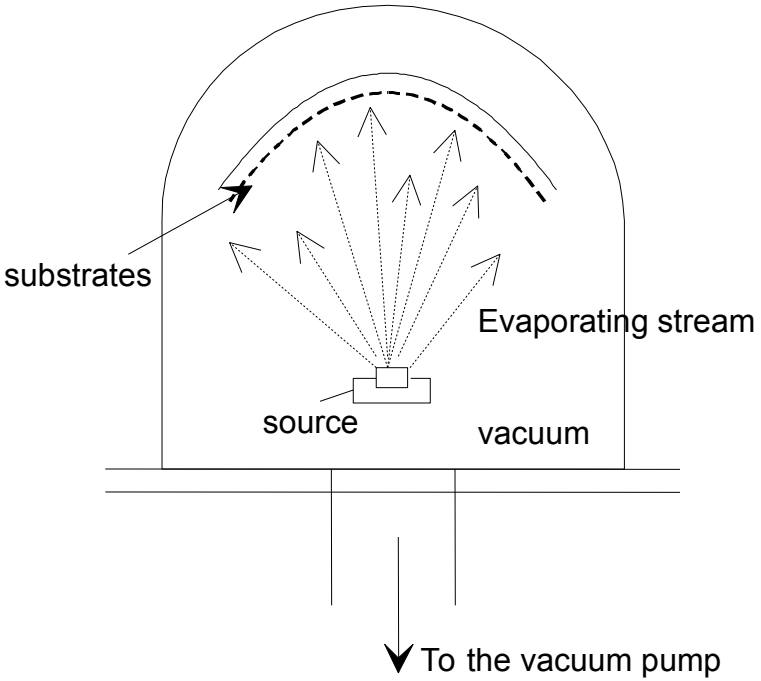
  300 ˚C PECVD, 700 ˚C LPCVD

- Silicon dioxide $SiH_4(silane) + O_2 \rightarrow SiO_2 + 2H_2$

  450-600 ˚C

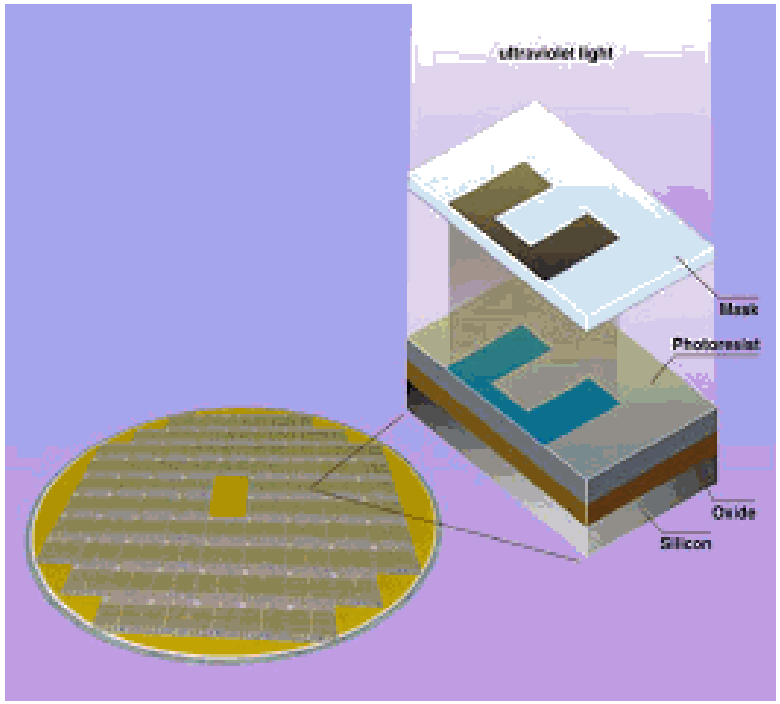
Physical Vapour Deposition

- Aka Thin Film Technology
- Thermal evaporation or sputtering
- Metallization or polycrystalline silicon



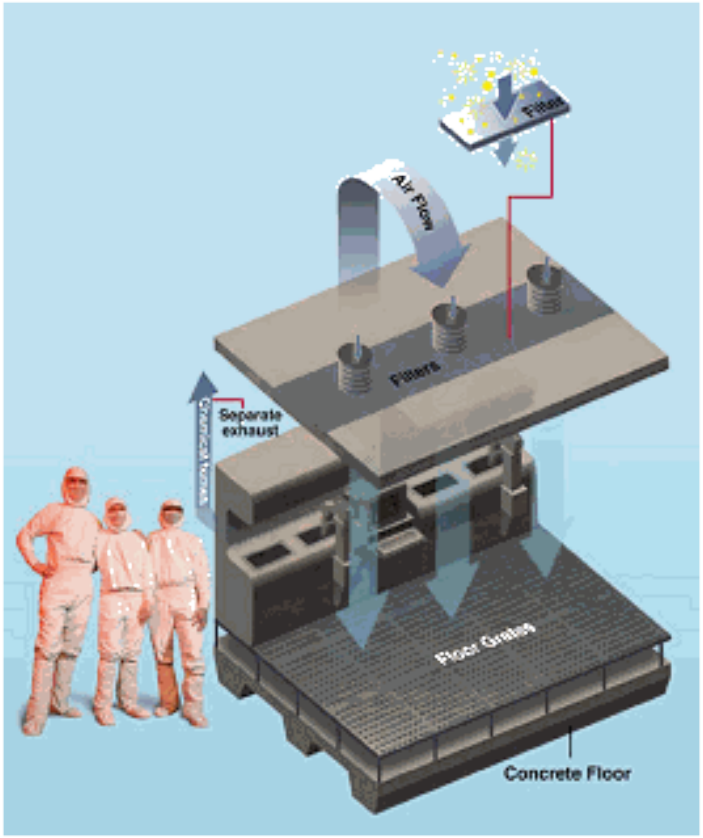
Masking and Lithography

Copying of the pattern representing the mask level to the semiconductor surface



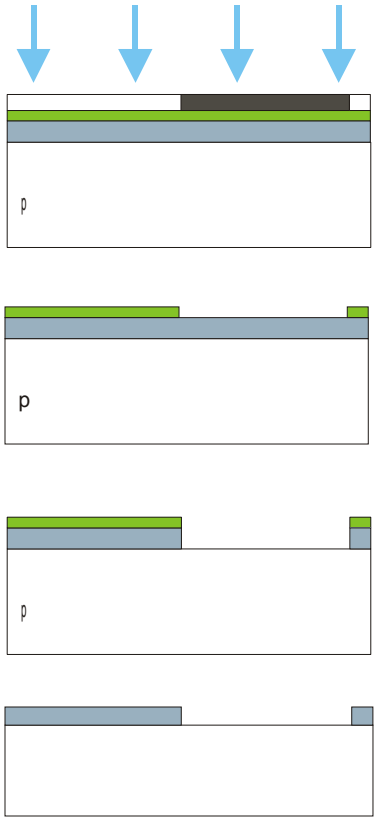
Clean Room Class

- Number of dust particles in a cubic foot
- From 1 to 10 000



Photolitography
(Stone Carving with Light)

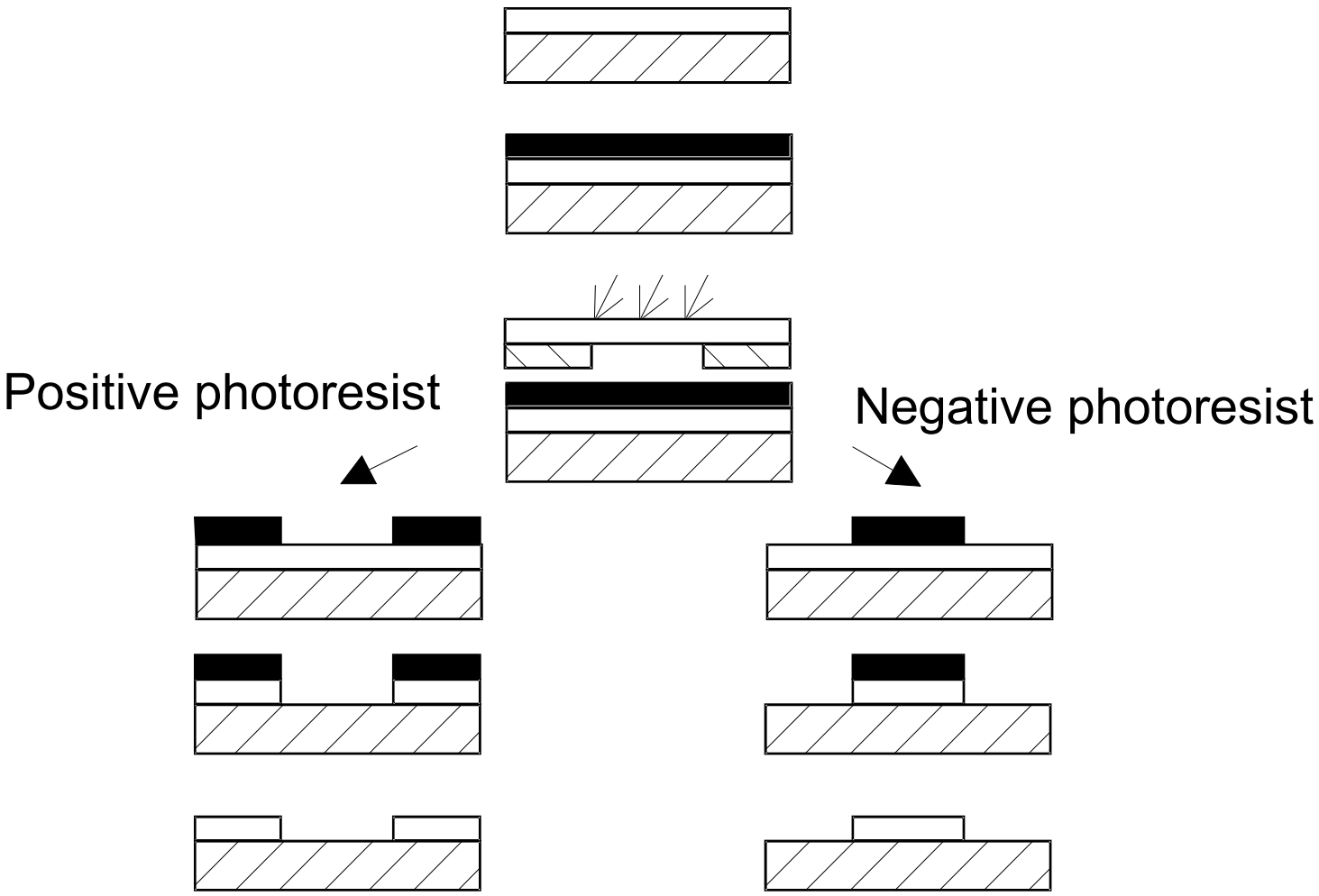
- Covering of the substrate with the uniform layer of photoresist
- Exposure
- Removal of exposed or non-exposed photoresist
- Technological operation on open areas
- Removal of hardened photoresist



Positive and Negative Photoresist

Exposed areas are removed during development, non-exposed areas will be the mask

Image on the photoresist corresponds directly to the image on the mask, hence the name "positive".


Positive photoresist
Negative photoresist

Photolitography

The sequence of processes to transfer the pattern from the masks to the photoresist.
Radiation affects the molecular structure of photoresist and its solvability.

The resolution is limited by the wavelength

- **ultraviolet,**
- **low energy X-rays,**
- **electron beam**
- **ion beam**

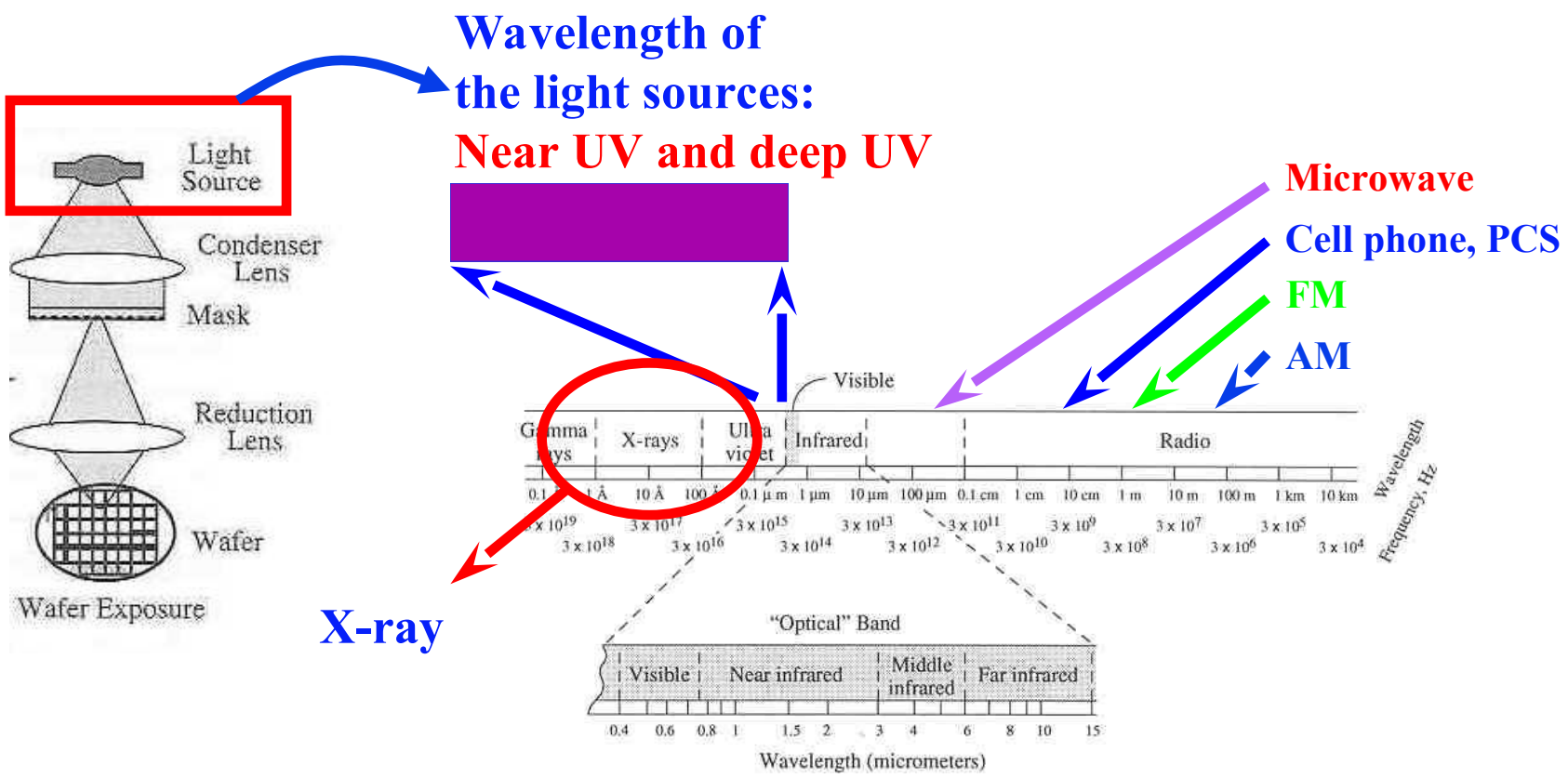
Masks

- **Mask is a stencil for the modified/deposited layer, its accuracy must be a few times higher than desired accuracy of reproduction.**
- **Masks are usually made of sodium-calcium, boron-silicium or quartz glass.**
- **The mask pattern material is usually chromium.**

Not all methods require masks -
controlled beam of high-energy particles bombarding the substrate can be applied

- **electrons**
- **ions**

Light Sources in Photolitography



Types of Litography

- Proximity litography

  Mask a few μm from the substrate

- Contact litography

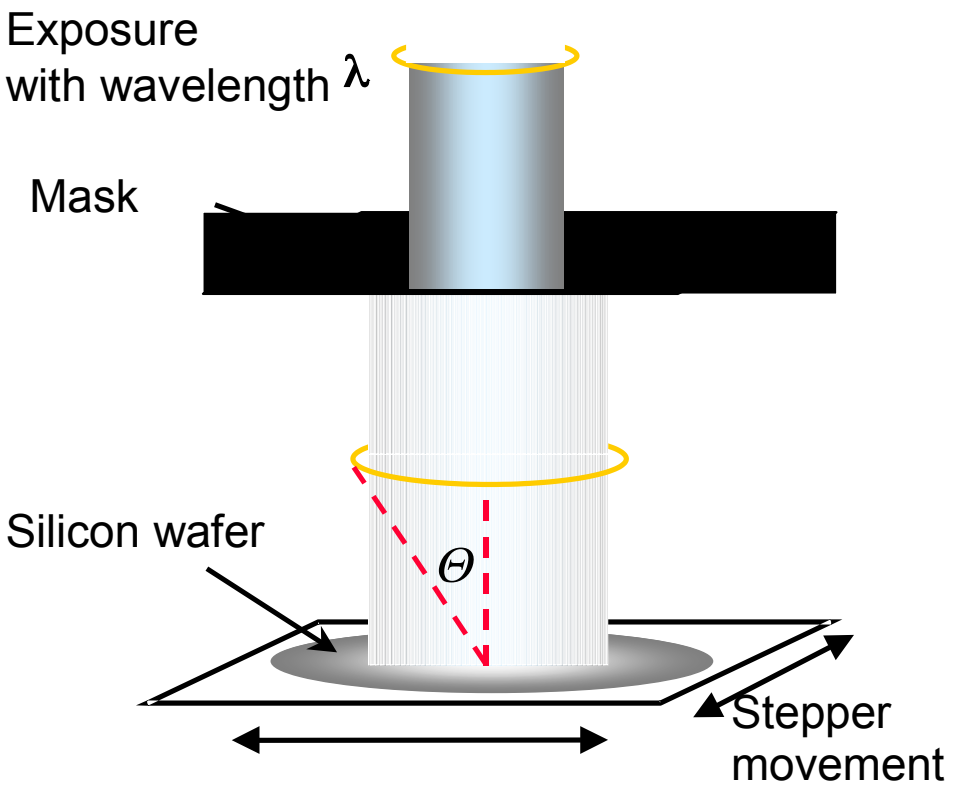
  Mask touches the substrate

- Projection litography

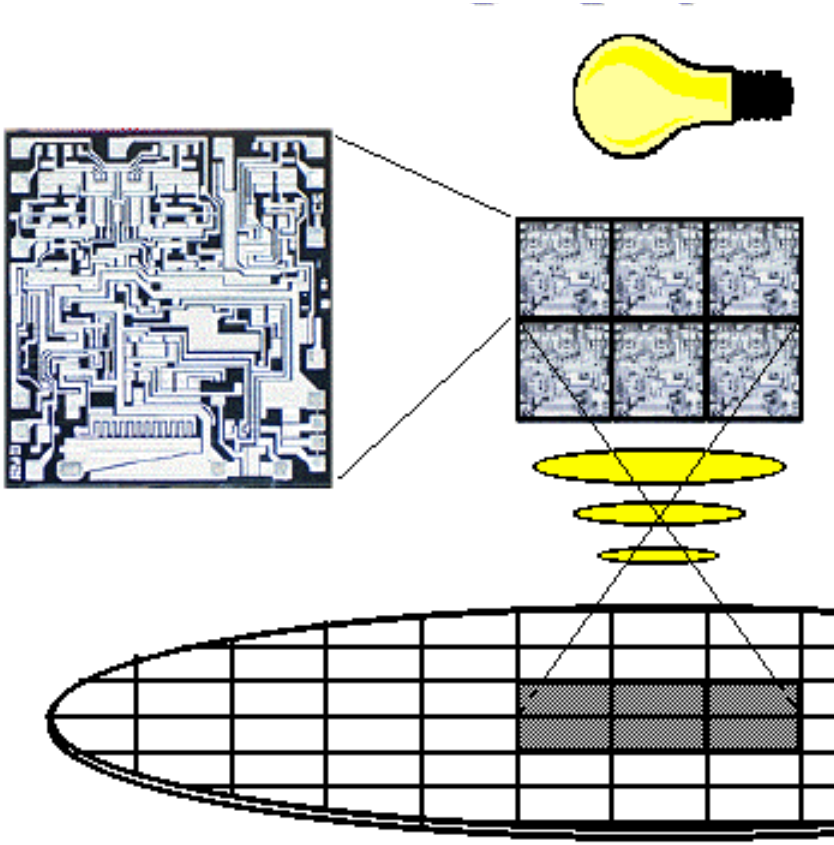
  Image of a mask is projected through the lens to the surface of the substrate

Projection Litography

The image of a single chip mask is projected through the lens to the surface of the substrate. The wafer is moved using the stepper to expose all the chips.



Projection Litography



- The wafer is coated with photoresist material
- The reticle containing a layer's image of one or more die are exposed by a light source through a lens system onto the wafer
- The wafer is then stepped over to the next die and the process repeated until the wafer is completely exposed

Optical Litography Limitations

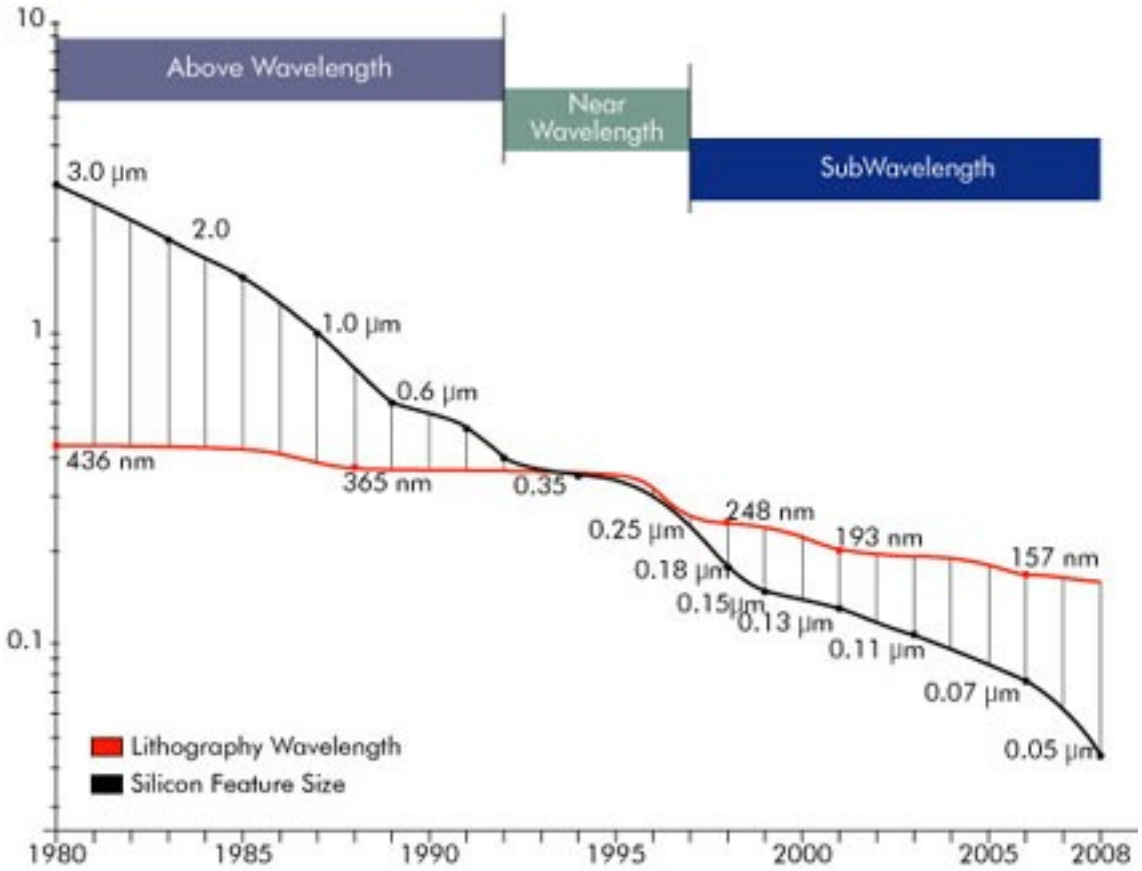
- MTF - Modulation Transfer Function - a measure of contrast

$$MTF = \frac{2}{\pi}\left(\phi - \frac{1}{2}\sin(2\phi)\right)$$

$$\phi = \cos^{-1}\left(\frac{\lambda}{4Wn_a}\right)$$

- λ=157 nm, W=100nm, n_a(=n sin(θ/2))=0.6 $\Rightarrow$MTF=23%

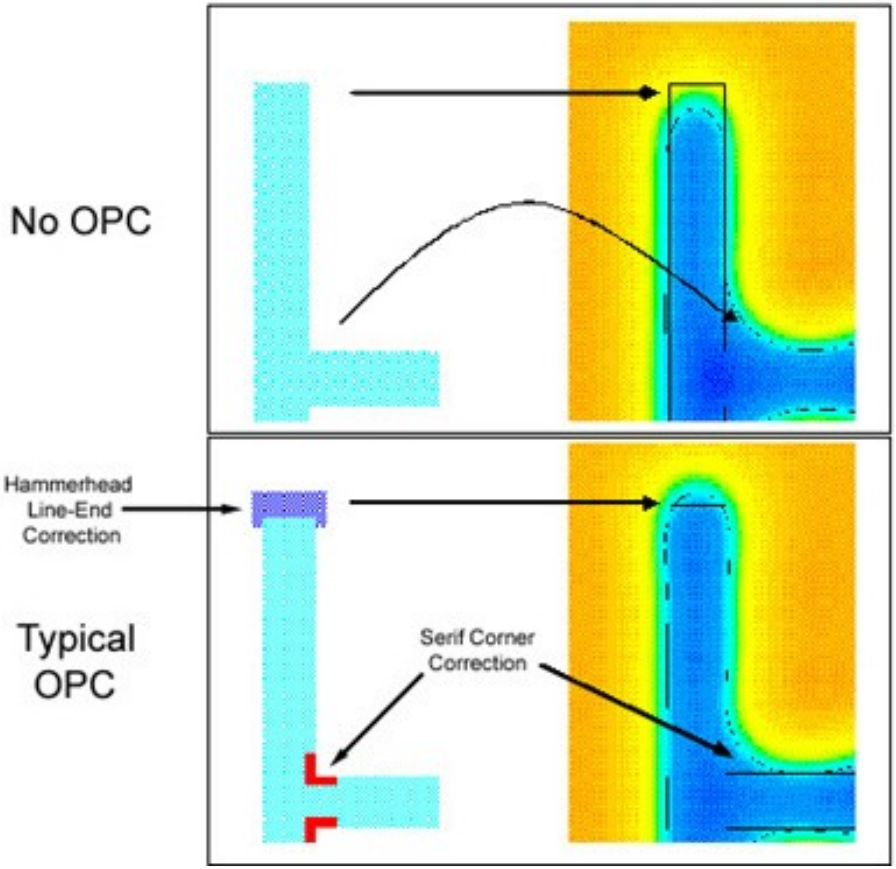
Photolitography Wavelength and the Feature Size

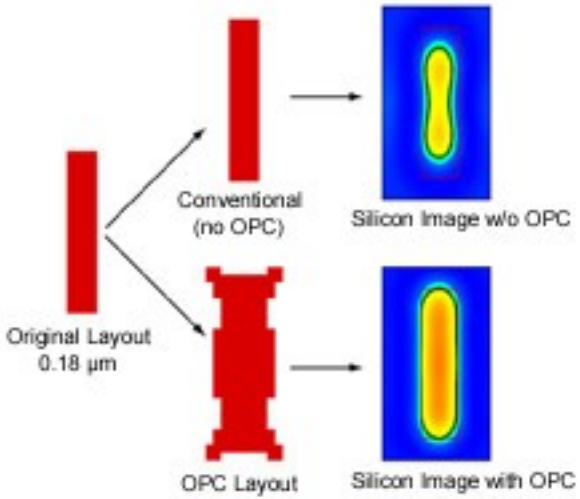


Source: Numerical Technologies http://www.numeritech.com

Optical Proximity Correction

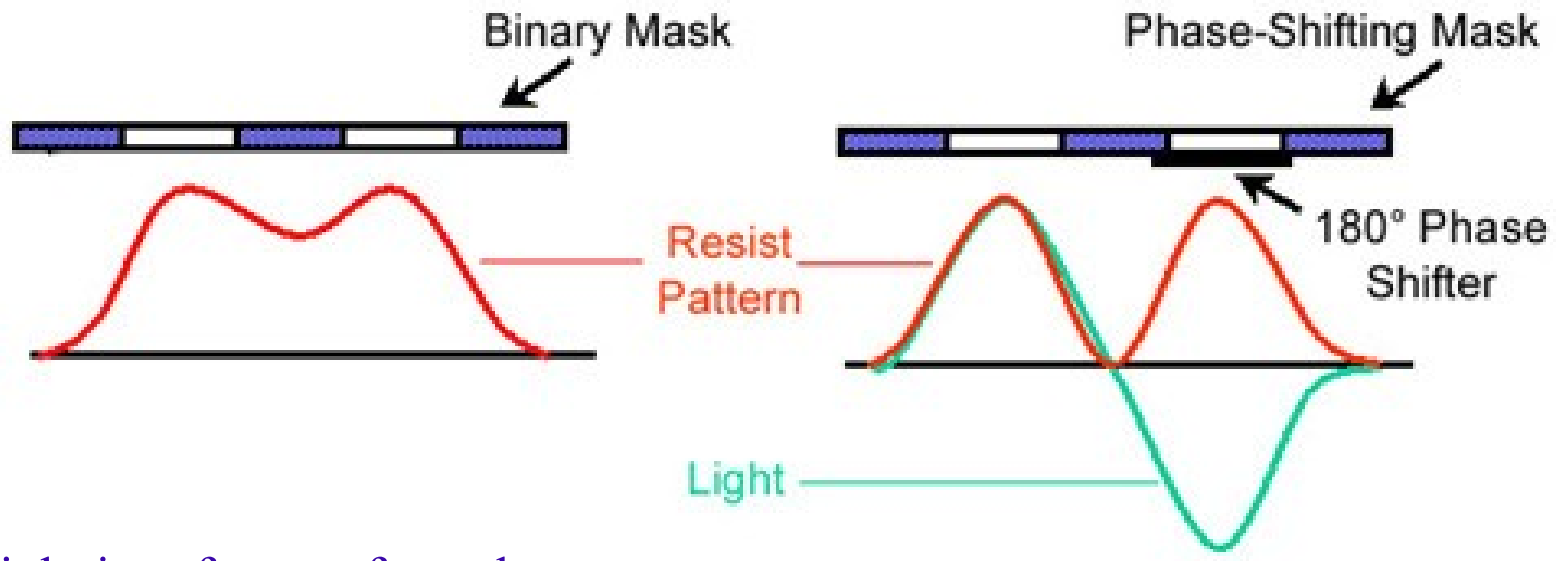
correction of an optical density of a light beam





Source: Numerical Technologies http://www.numeritech.com

Phase - Shift Masks



Light interference from the neighbouring mask openings

Phase-shift mask

Source: Numerical Technologies http://www.numeritech.com

Removal of Excessive Photoresist

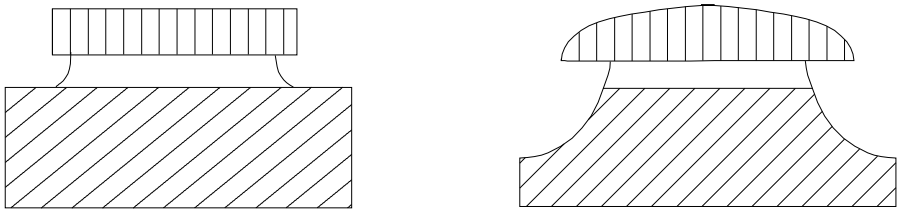
- **Organic solvent**
- **Inorganic acid**
- **Monoatomic oxide**

Etching

- Wet or dry
- Dry etching advantages:
  - High resolution
  - High anisotropy
- Dry etching
  - physical
  - chemical
  - chemical-physical
  - photochemical

Etching Characteristics

Selectivity - ability to selectively etch one material without attacking others



Anisotropy - higher speed of etching in one direction