Electronic Technology Design and Workshop

Presented and updated by

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DMCS room 2

2007

Electronic Technology Design and Workshop

Lecture 6

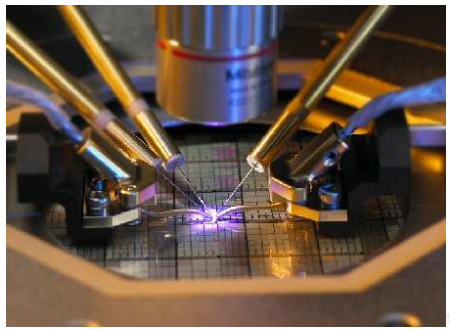
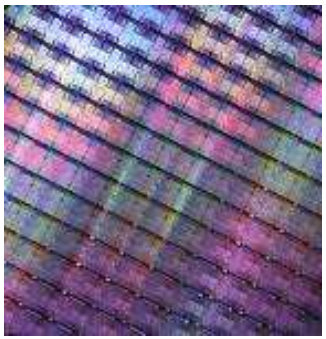
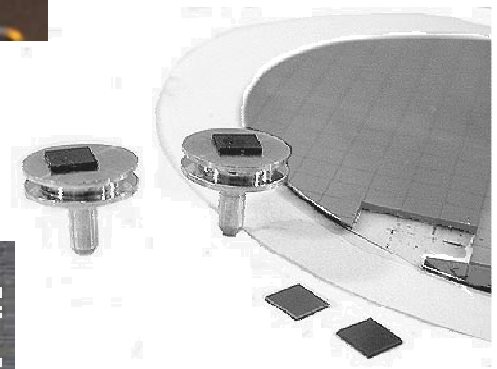
Microelectronics technology (part 2) Packages and Printed Circuits Boards

The lecture was prepared using wikipedia.org and other web pages dedicated to IC design

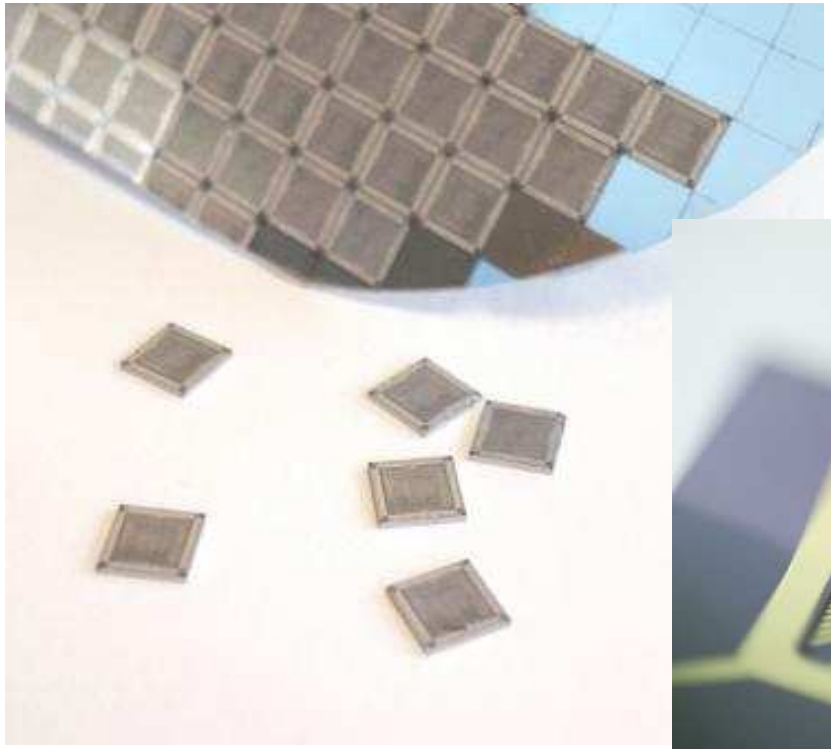
Silicon Integrated Circuits Technology

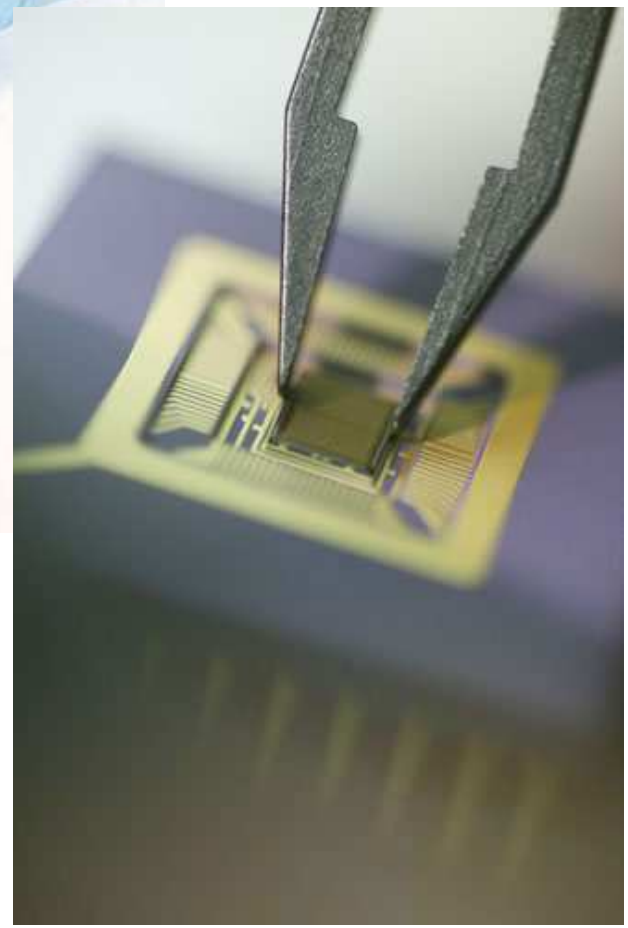
- Silicon wafer fabrication
- Silicon devices fabrication
- On-wafer testing
- Wafer-cutting
- Packaging
- **PCB**

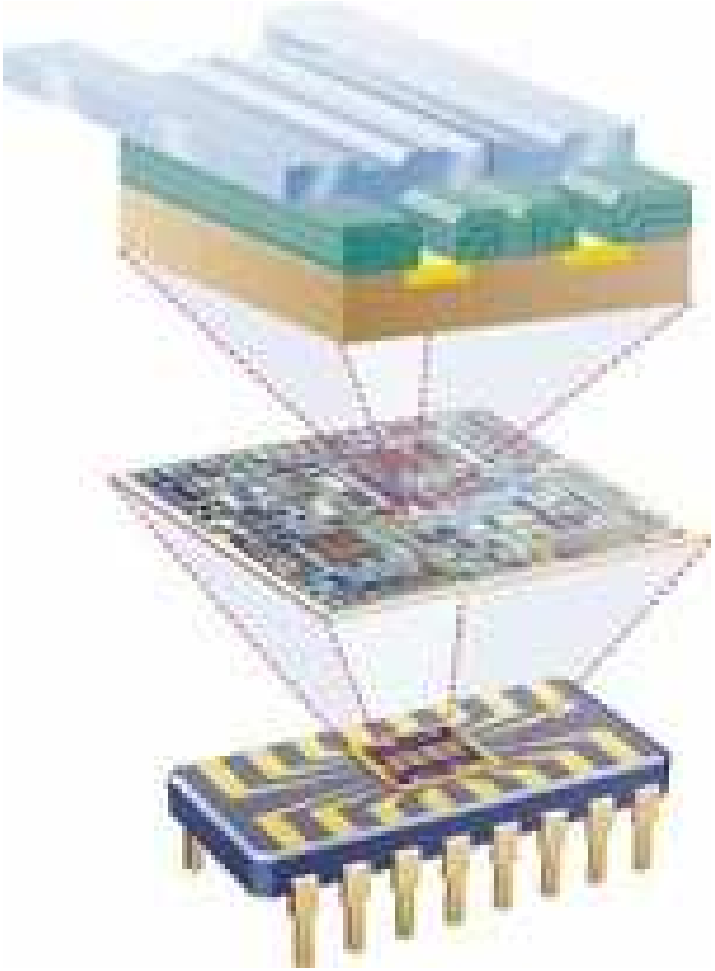


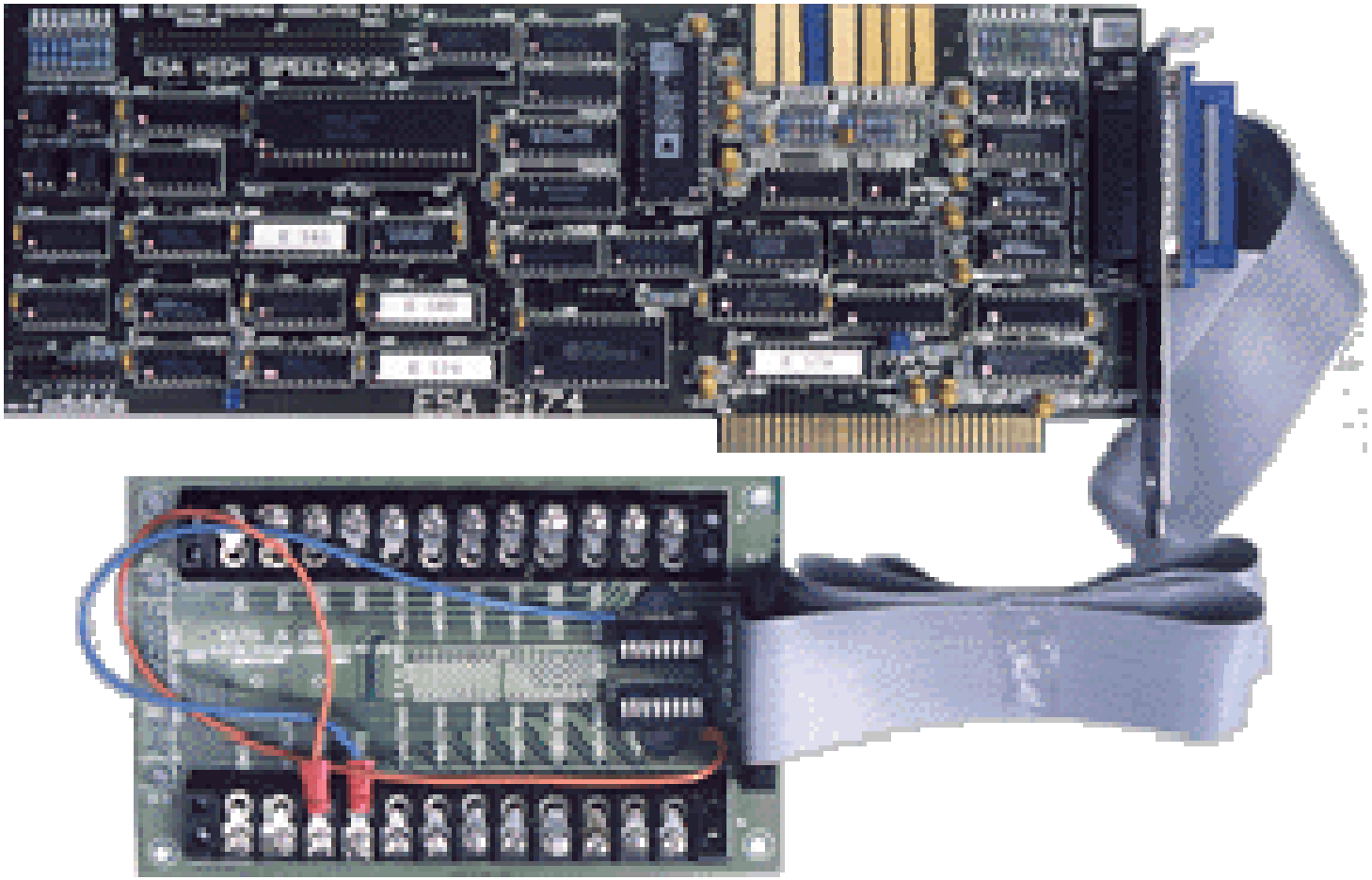
Introduction



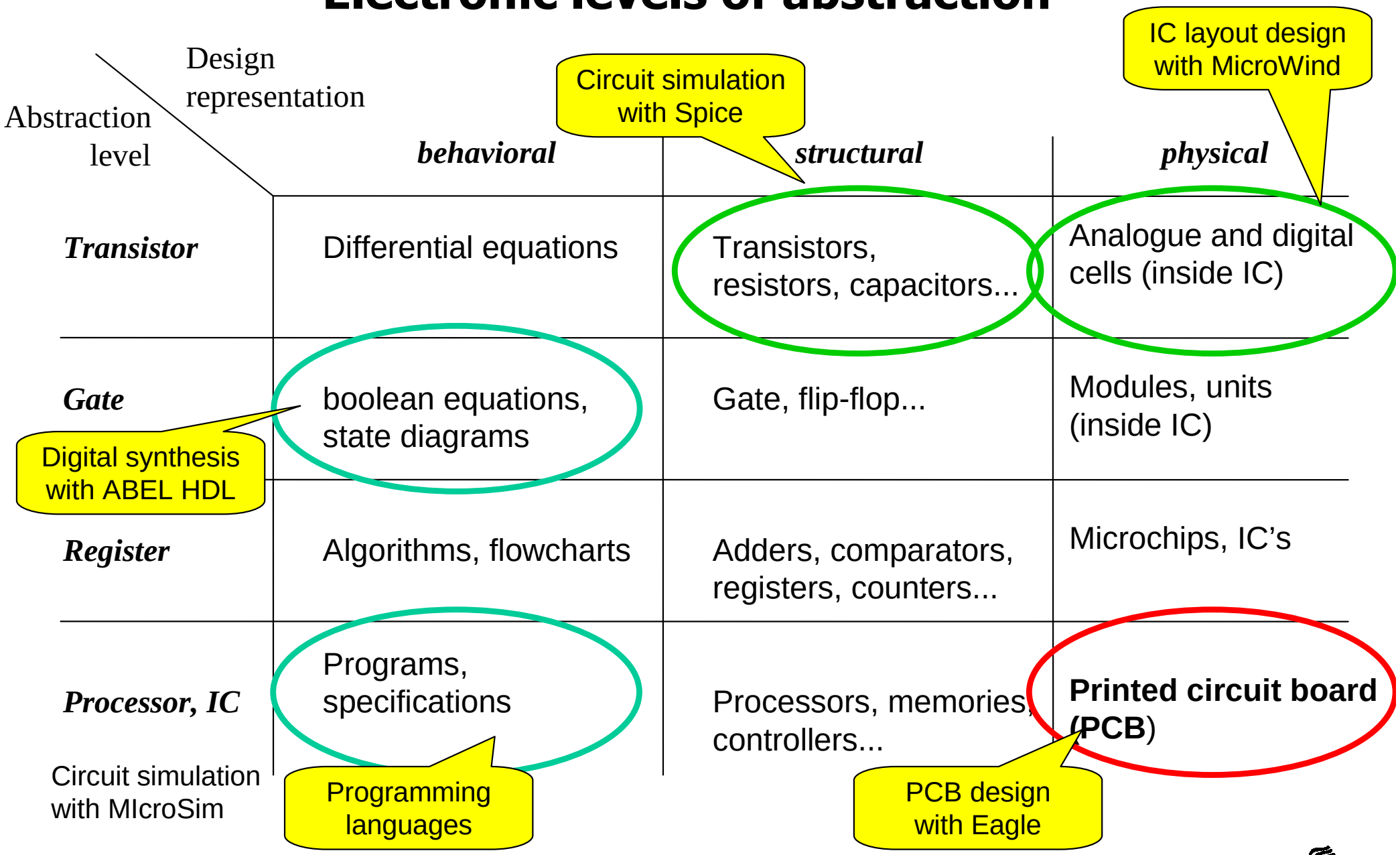




Printed Circuit Boards (PCBs)



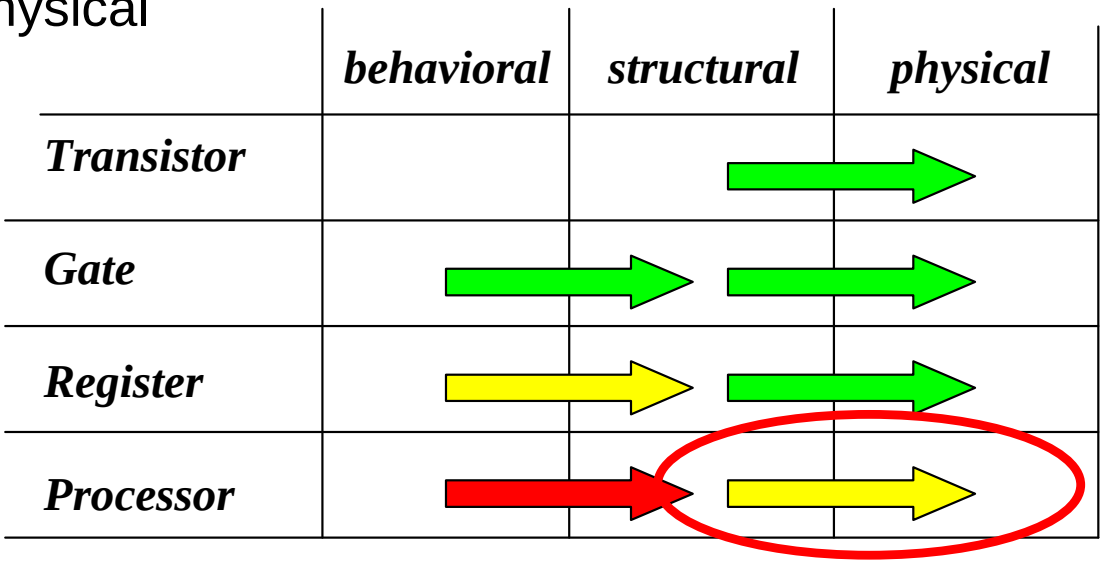
Electronic levels of abstraction



PCB Synthesis

Automatic translation of the circuit description to less abstract representations, e.g.

a) from behavioural to structural
b) from structural to physical
c) from behavioural to physical



Not supported
(some support possible in specific cases - *software-hardware codesign*)

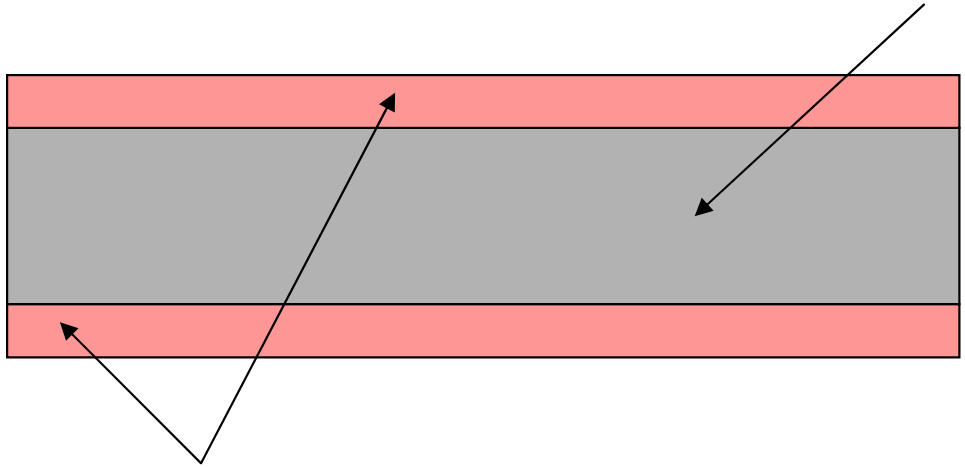
Partially supported (fully supported for certain types of digital designs)

Fully supported

Types of PCBs

Organic PCB

epoxy glass laminate
(organic resin reinforced with
paper, glass or quartz fibers)



copper sheets

Advantages:
- very cheap
- good electro-mechanical properties
- easy to manufacture in any shape
- suited to multilayer structures

Disadvantages
- low maximal working temperature
(125 ℃- 250 ℃)
- low thermal conductivity

Types of PCBs

Organic PCB

Rigid - epoxy glas laminate - most commonly used boards to host electronic components

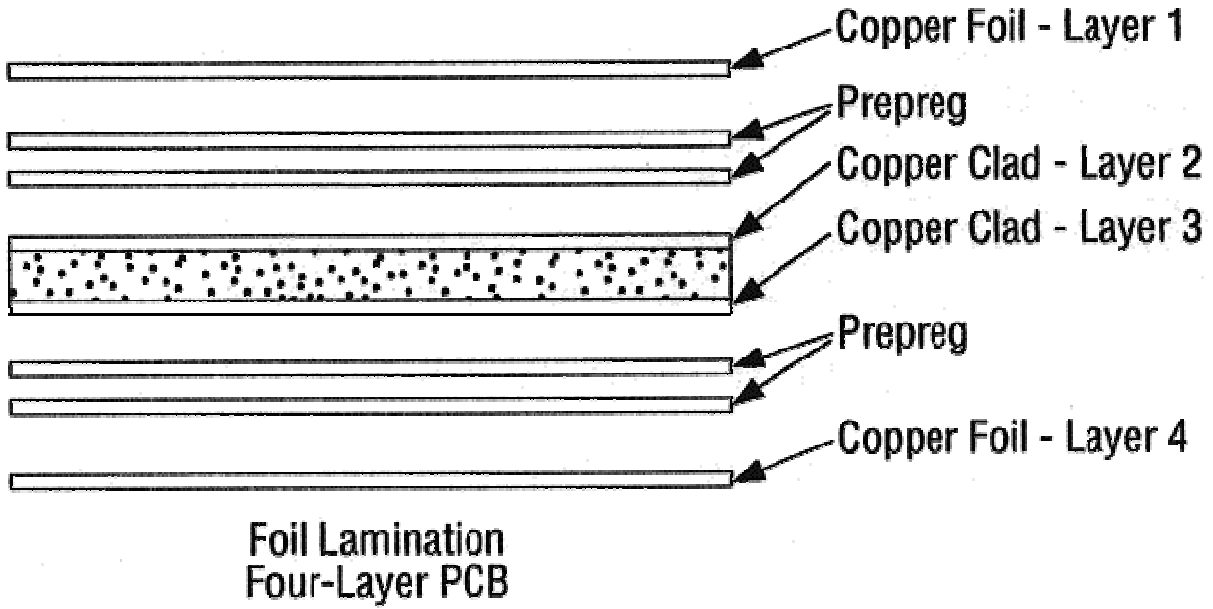
Flexible - polyiamids films - used for flat or ribbon cables

Single sided - for simplest electronics and development boards

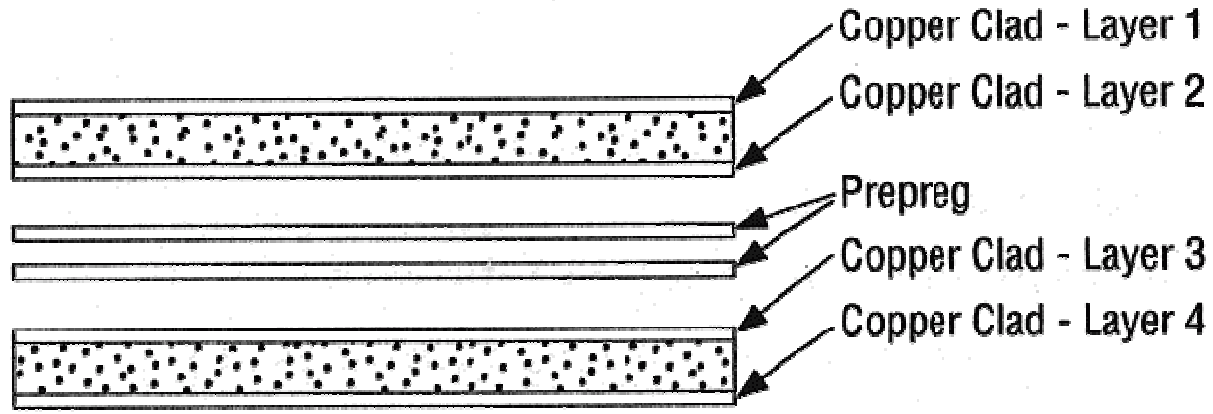
Double sided - for simple and medium complicated electronic circuits prototypes and development boards

Multilayer - for majority of high-level electronic circuits

Multilayer PCBs

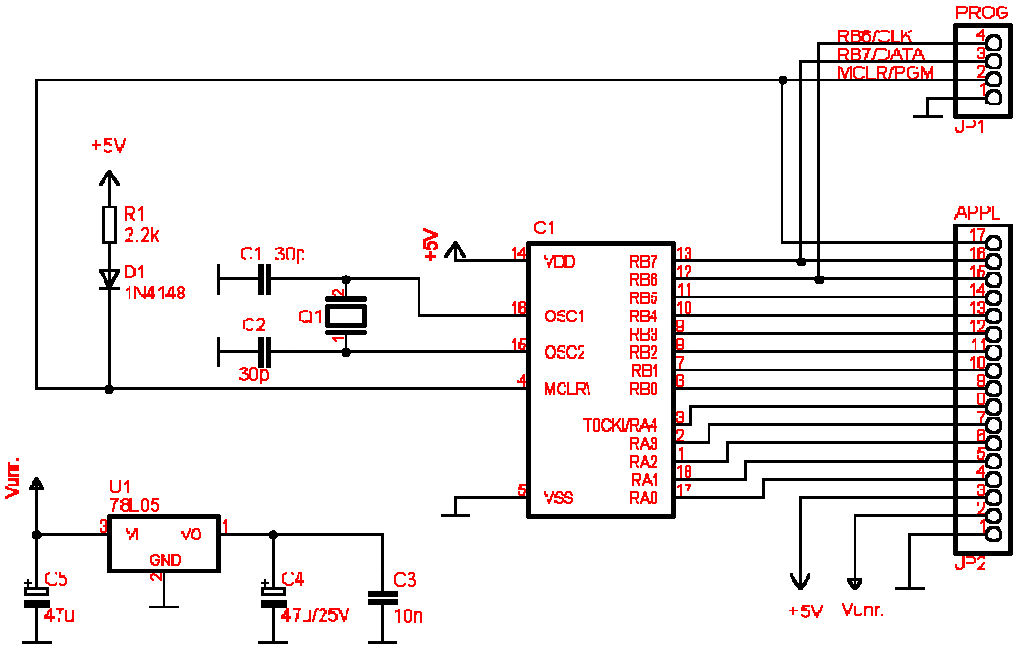


Foil Lamination
Four-Layer PCB



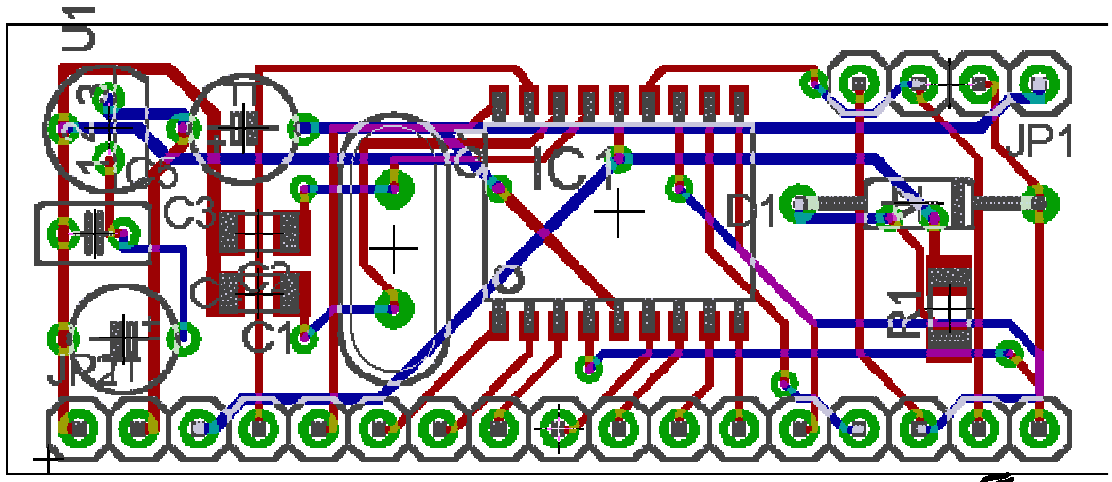
Cap Sheet Lamination
Four-Layer PCB

Design of PCBs



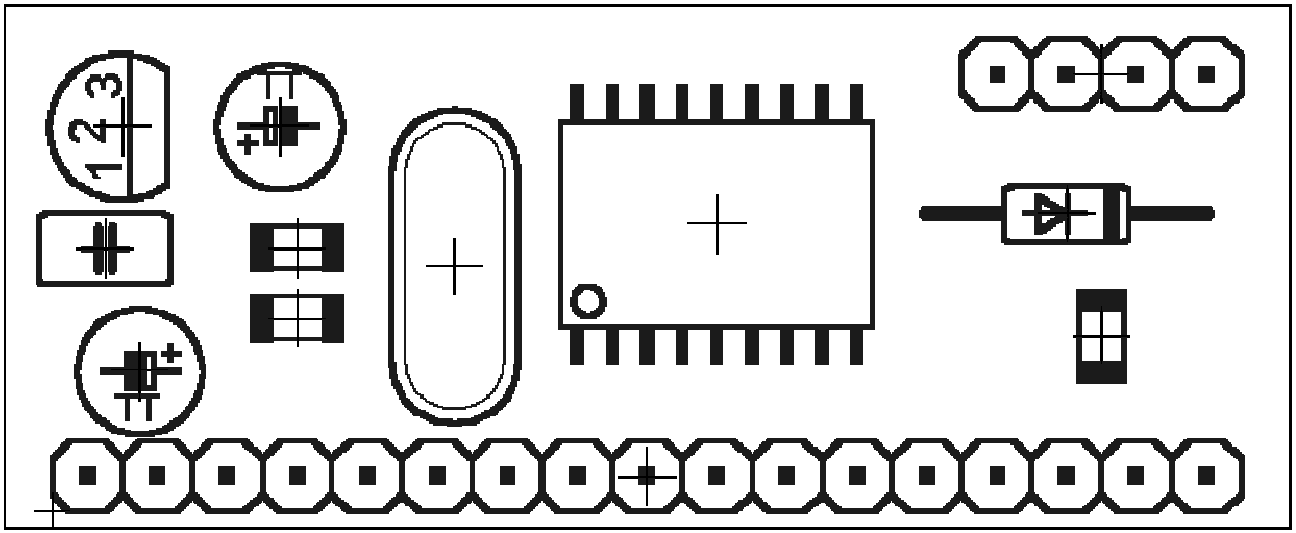
Schematic editor
with simulation aids

PCD editor
with autorouting aids

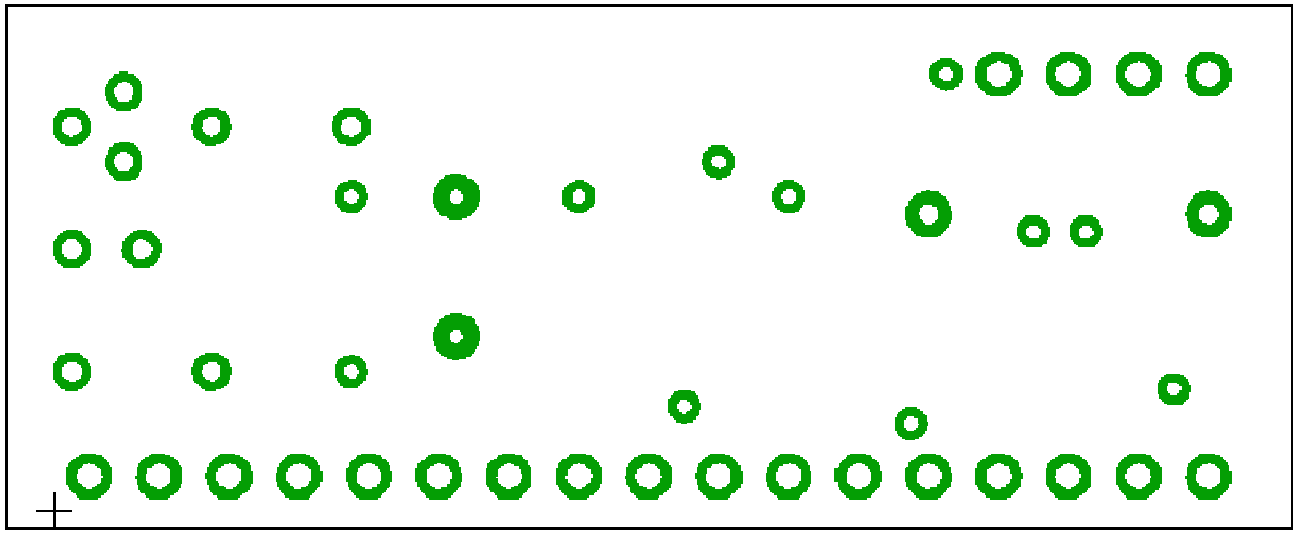


Drawing PCB masks

Positioning of elements

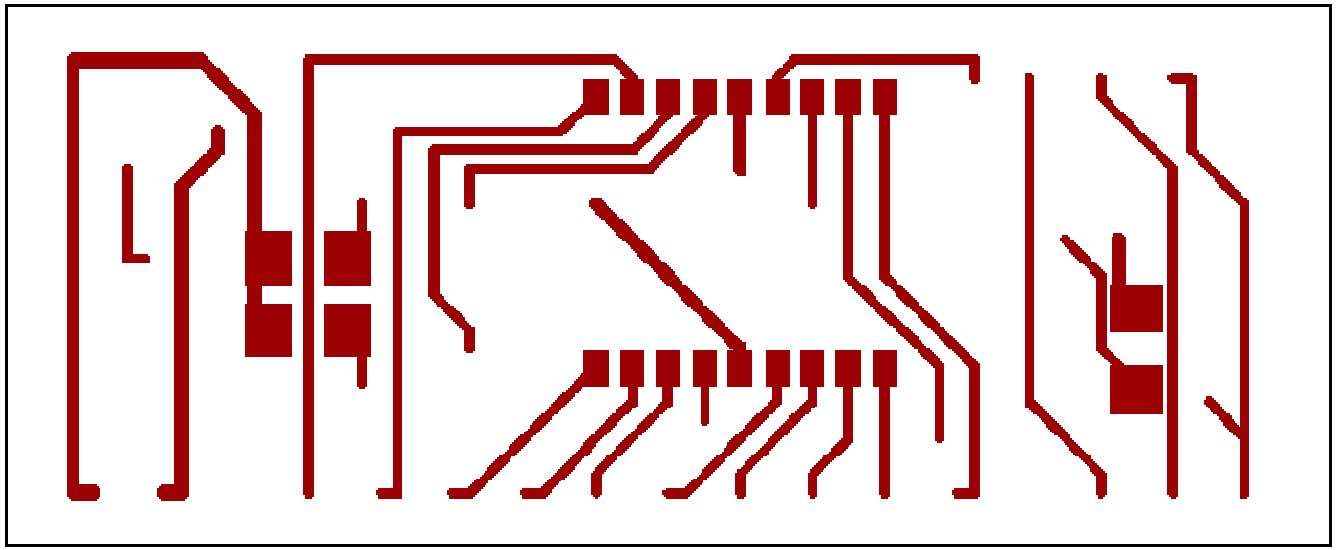


Positions of pads, holes and vias

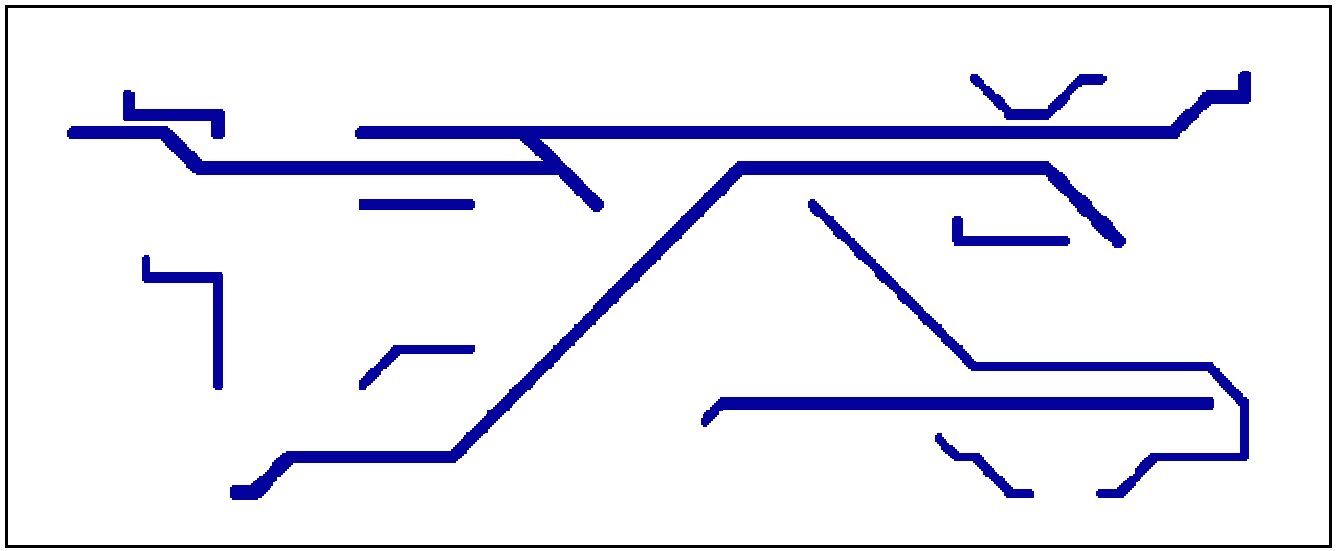


Drawing PCB masks

Top layer mask

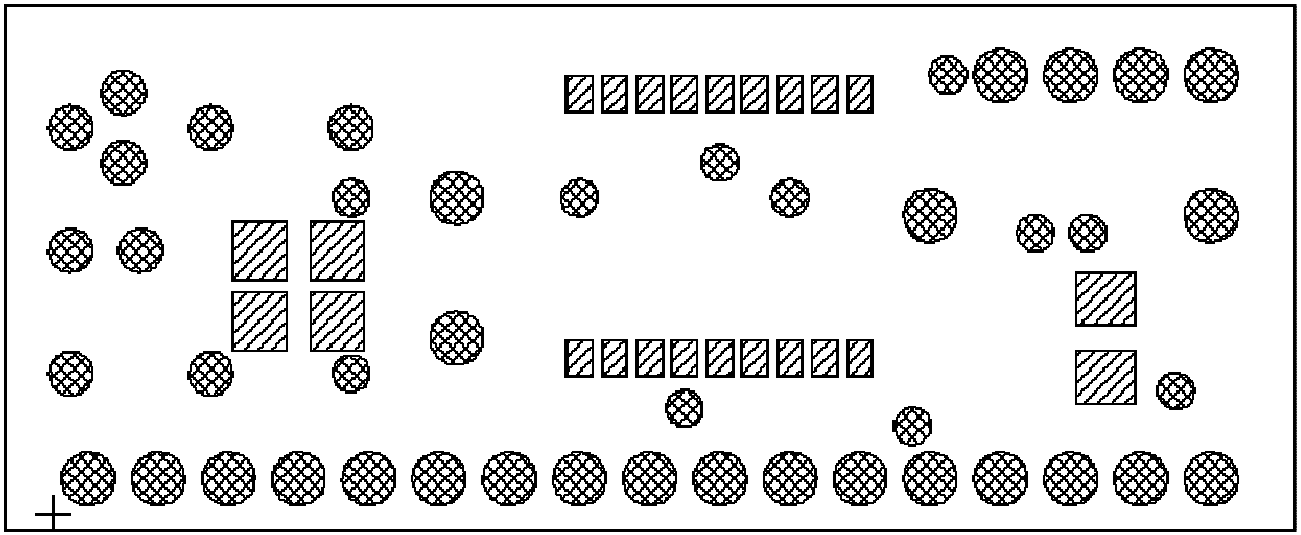


Bottom layer mask

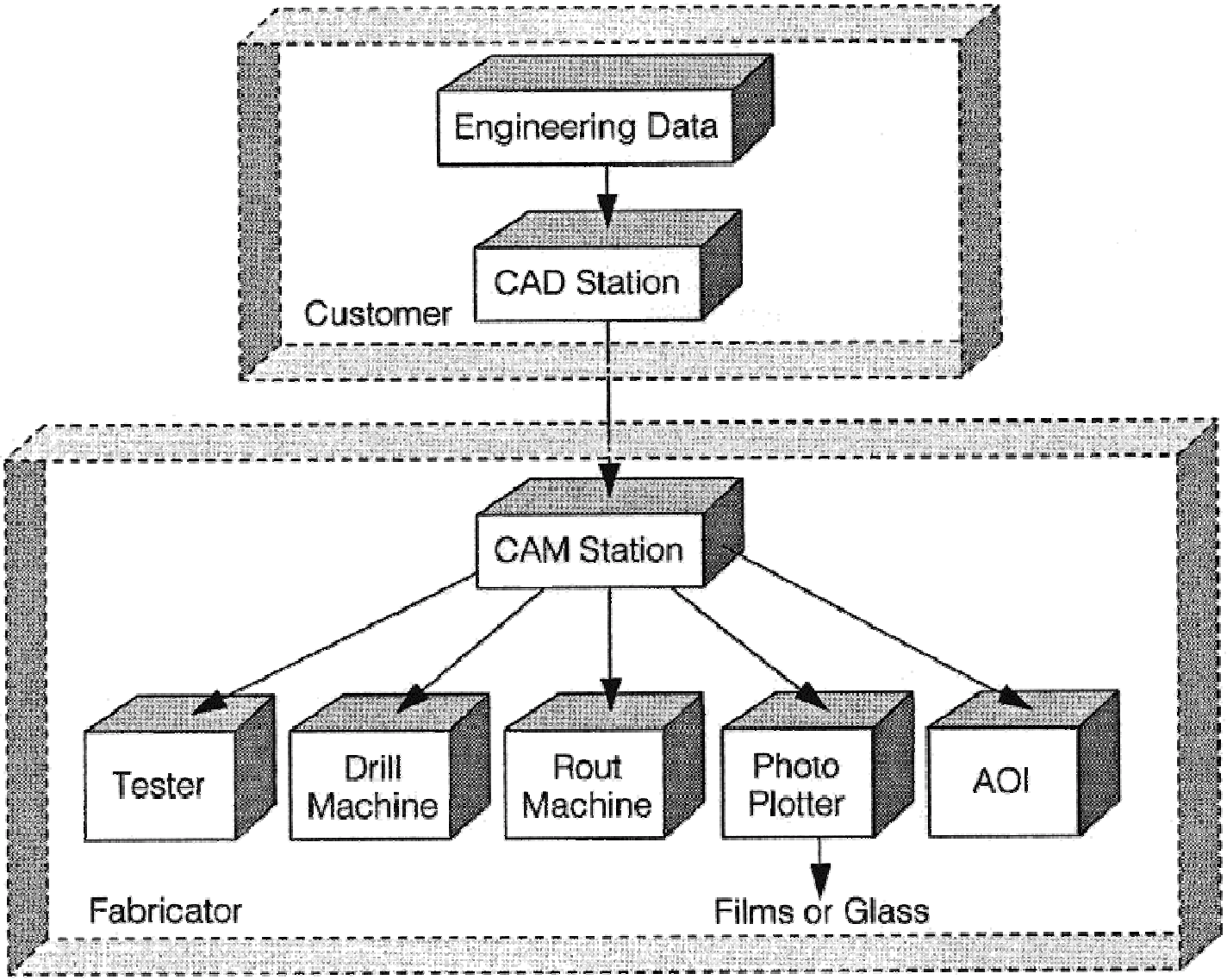


Drawing PCB masks

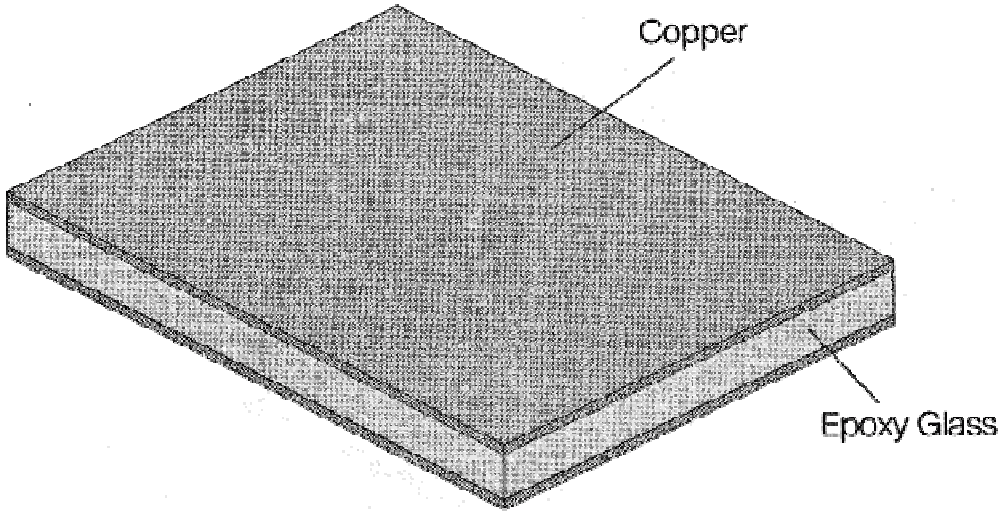
Solder mask



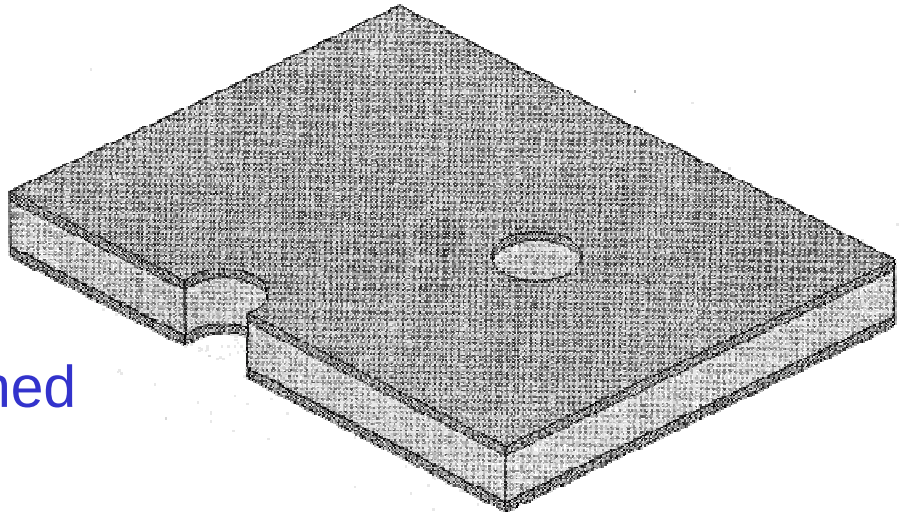
Computer integrated manufacturing of PCB



Double-sided PCB manufacturing



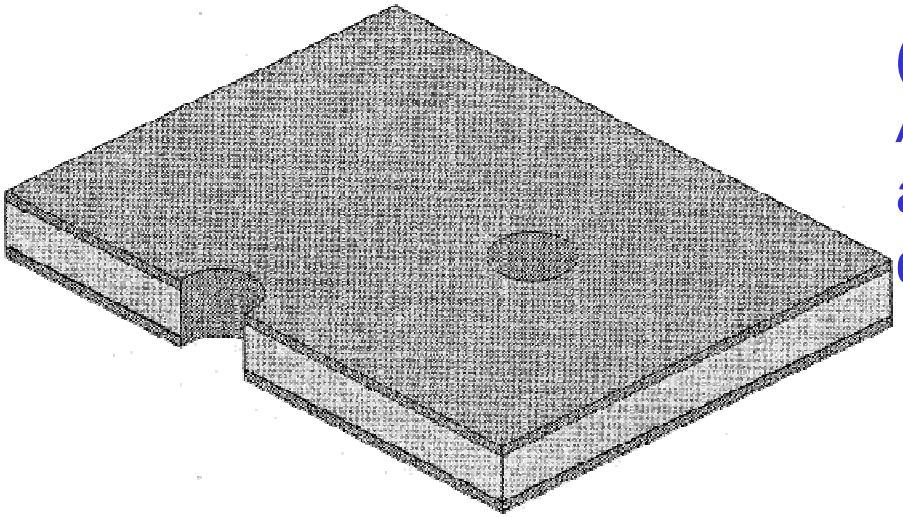
(1) *Copper-clad epoxy glass*



(2) Drill

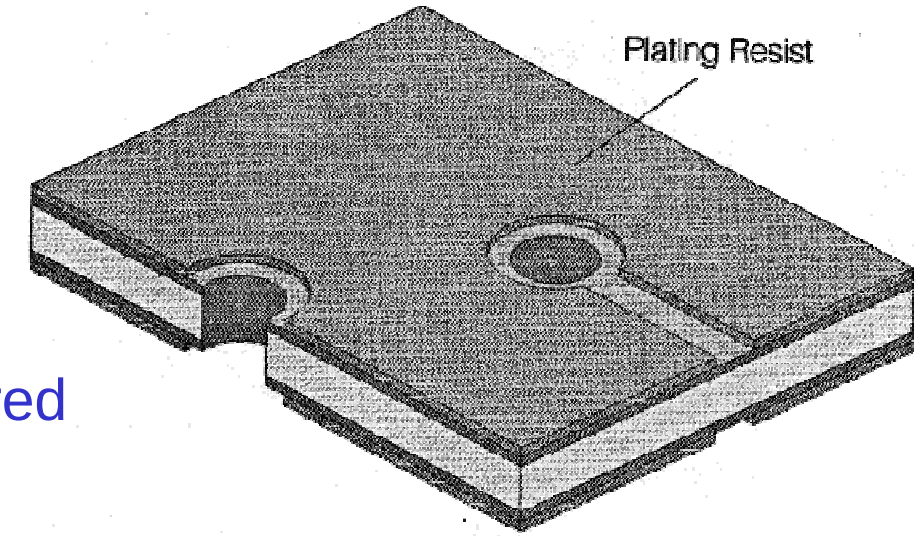
Hole sizes and location are determined by drill data provided by customer

Double-sided PCB manufacturing



(3) Electro lees copper plate

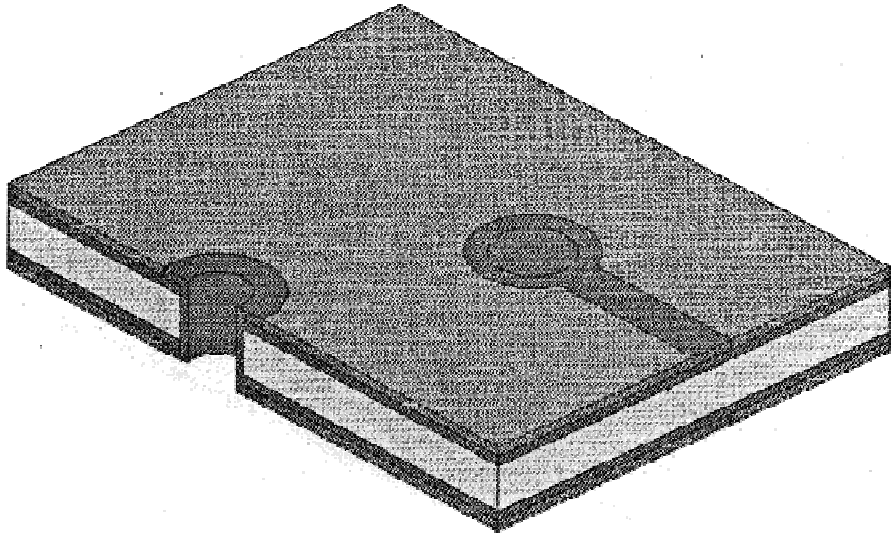
A thin layer of copper is deposited on all surfaces including the walls of the drilled holed



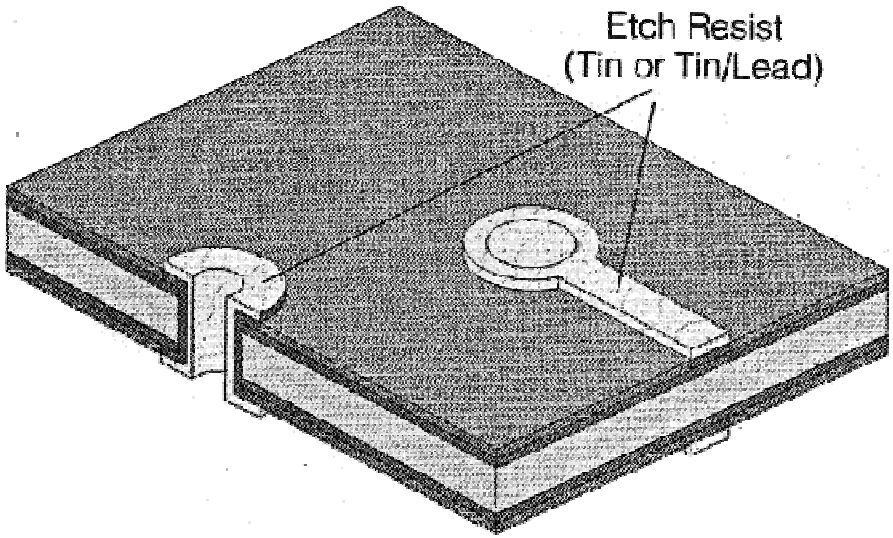
(4) Apply plating resist

The desired circuitry is left uncovered

Double-sided PCB manufacturing

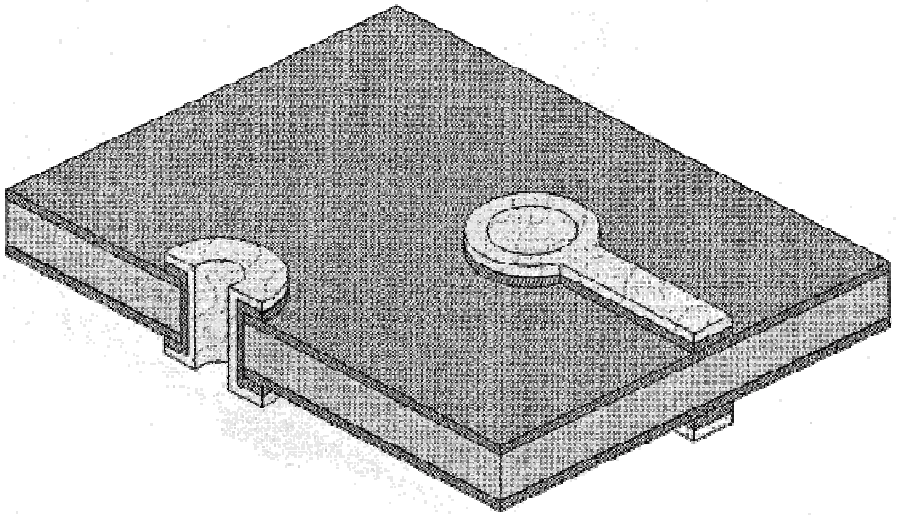


(5) Electroplate copper
The specified thickness is electrolytically deposited (usually 0.001”)

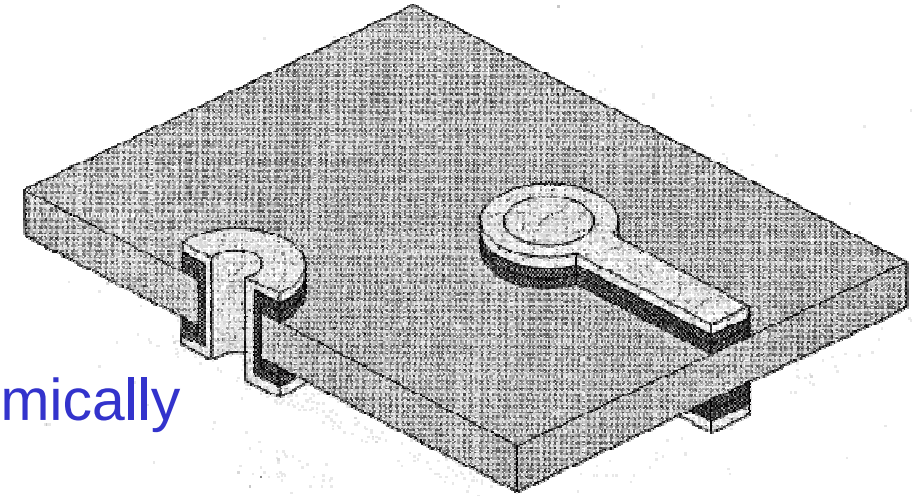


(6) Electroplate etch resist
Tin or tin/lead is electrolytically deposited over the copper plating

Double-sided PCB manufacturing

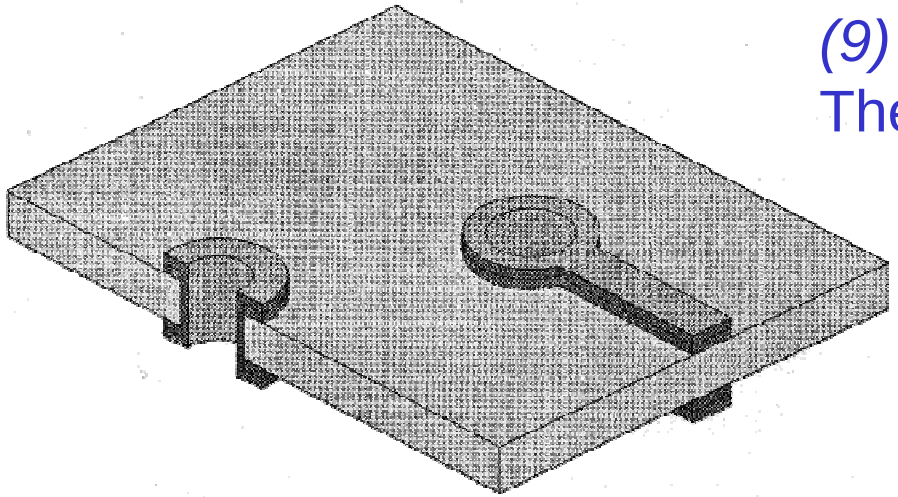


(7) Strip plating resist
Plating resist is chemically removed, revealing the surface copper



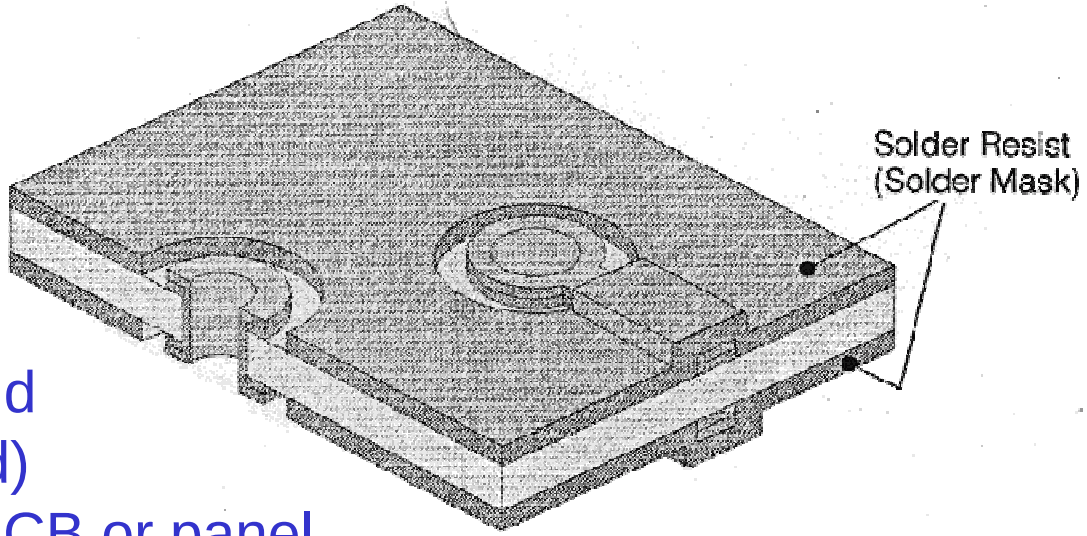
(8) Etch
The unwanted copper is removed chemically by an etchant that attacks copper, but not tin or tin/lead

Double-sided PCB manufacturing



(9) Strip etch resist

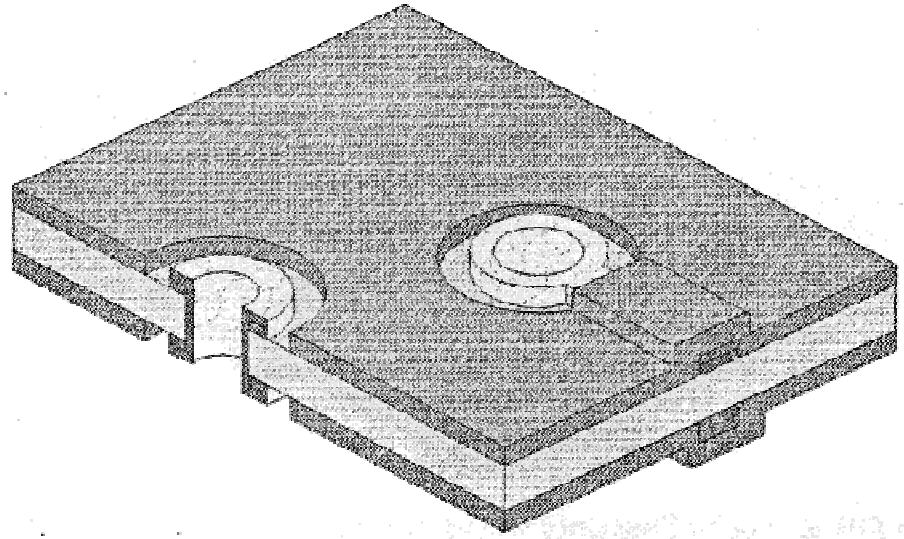
The tin or tin/lead is chemically removed



(10) Apply solder resist

The specified resist (dry film, liquid photoimageable or screen printed) is applied to the surfaces of the PCB or panel

Double-sided PCB manufacturing

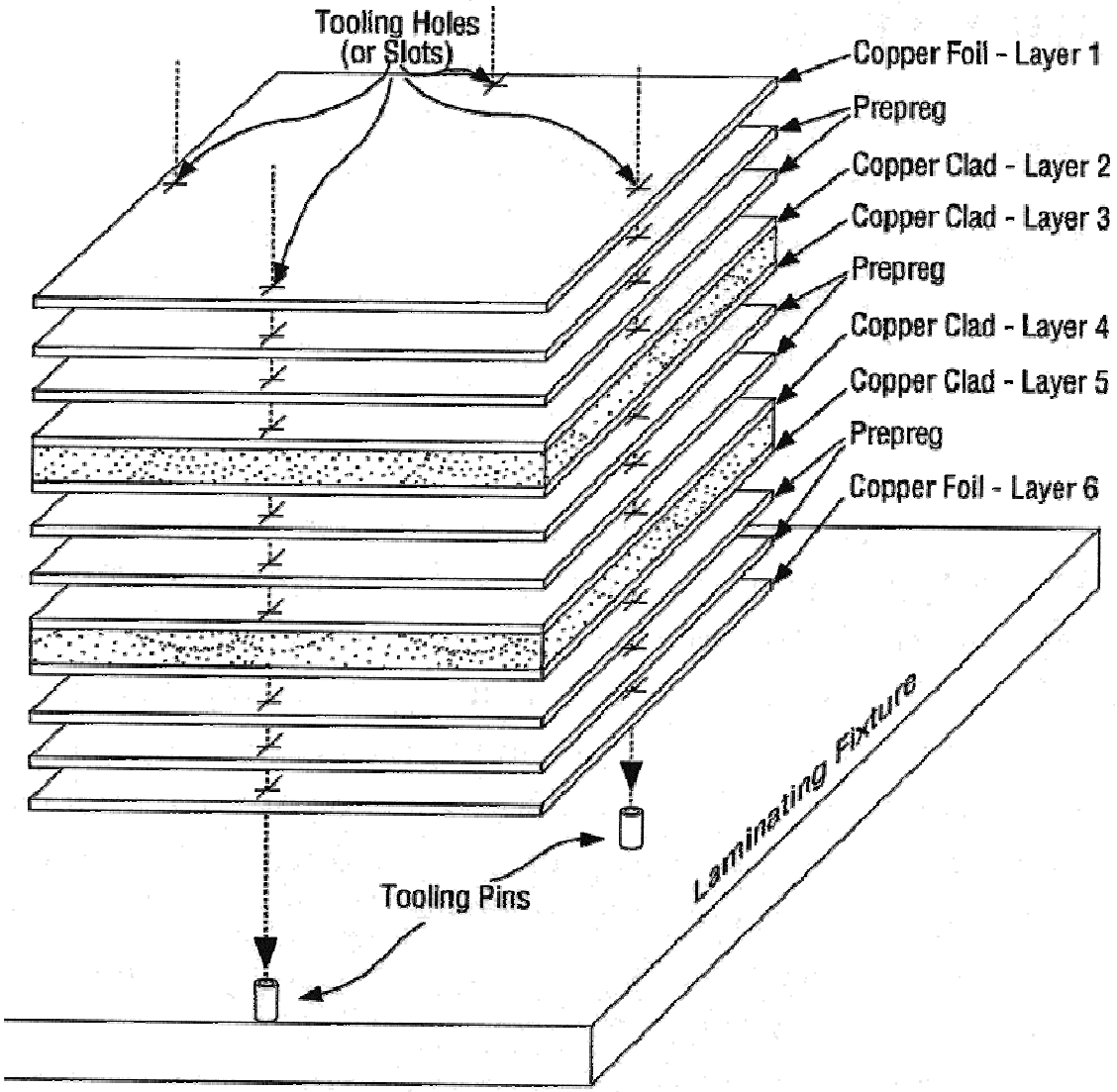


(11) Solder coat

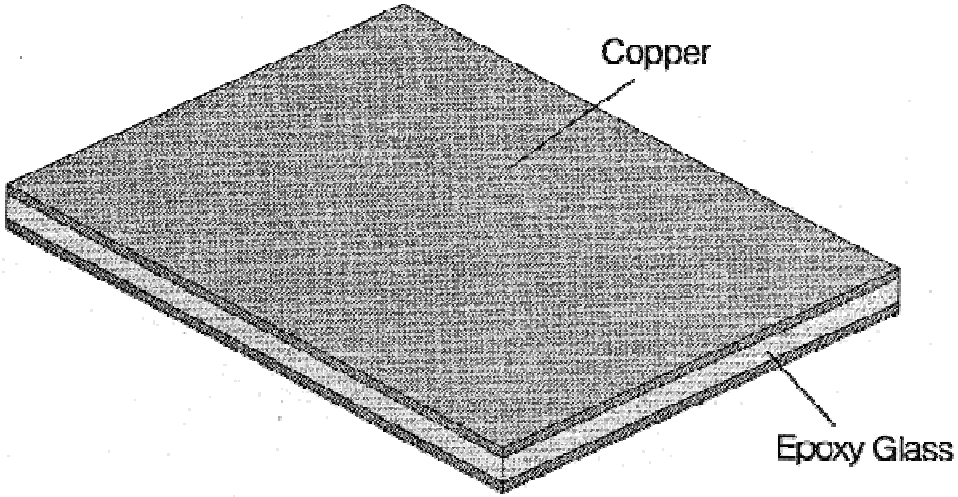
Solder (tin/lead) is applied to the exposed copper and the excess solder is removed

Multilayer PCB manufacturing

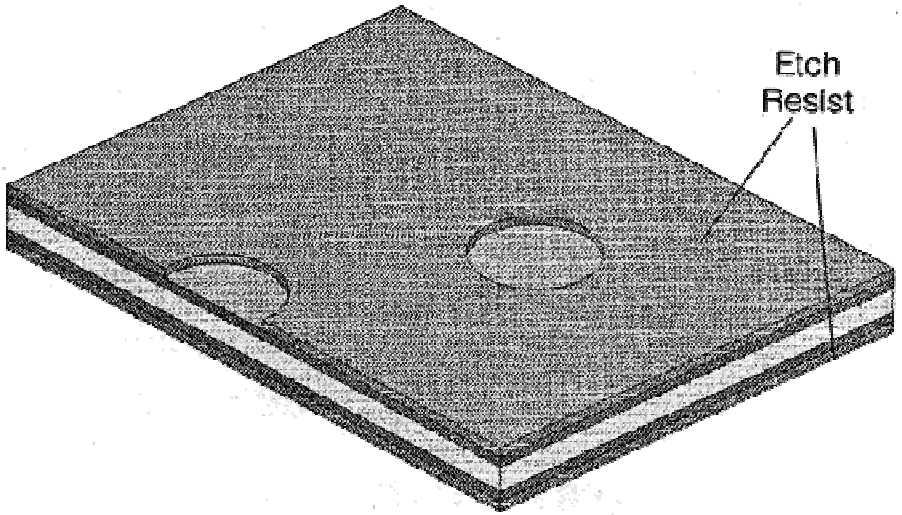
Build-up diagram for a 6-layer multilayer PCB



Multilayer PCB manufacturing

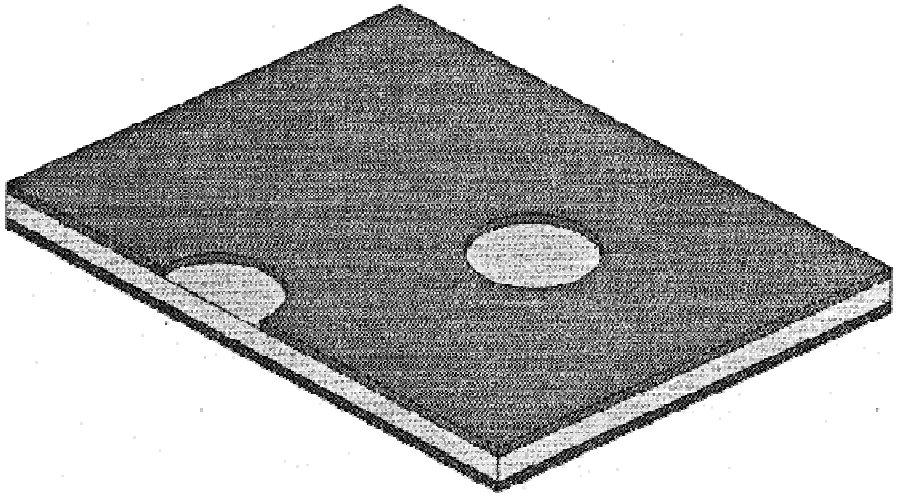


(1) *Copper-clad epoxy glass*
Inner-layers

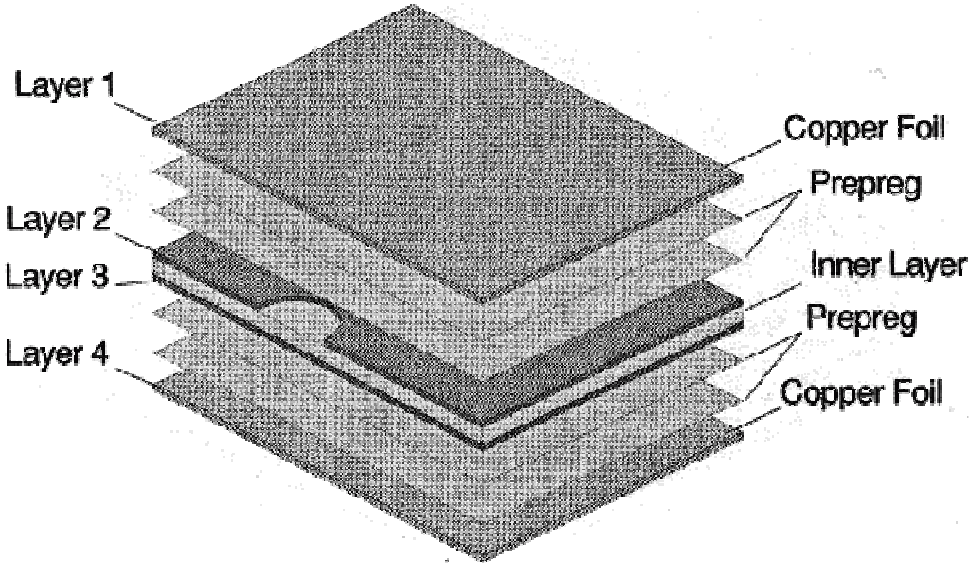


(2) *Apply etch, print and develop*
Unwanted copper is exposed

Multilayer PCB manufacturing

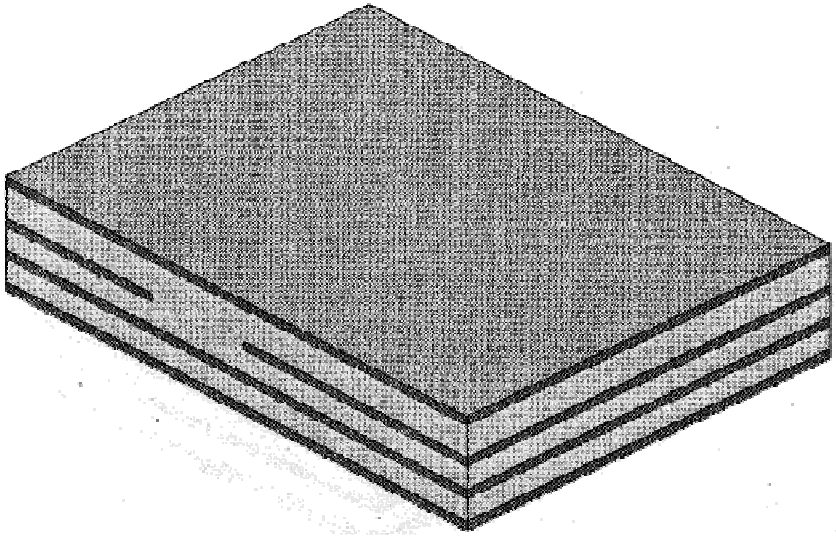


(3) *Etch*
Strip etch resist and treat surface with oxide

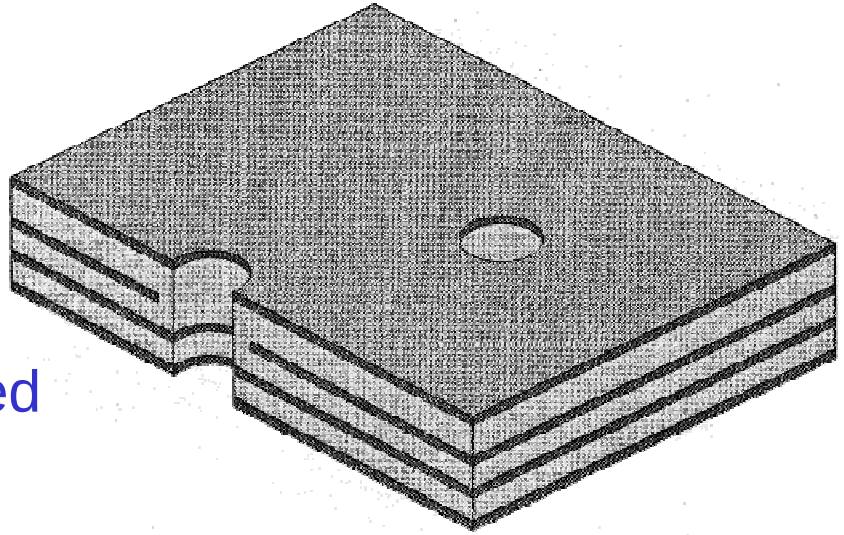


(4) *Layup*
4-layer multileyer using foil lamination technique

Multilayer PCB manufacturing

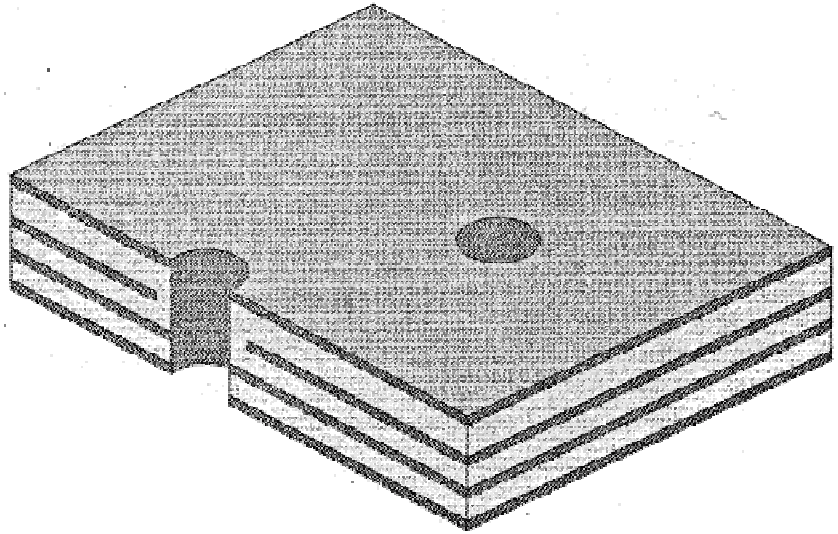


(5) *Laminate*
Heat and pressure cause prepreg to flow and bond layers together

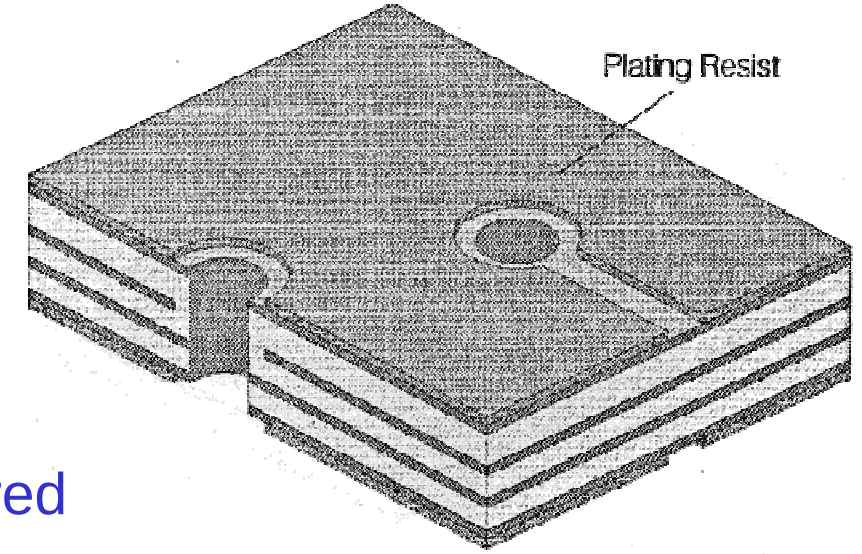


(6) *Drill*
Hole sizes and location are determined by drill data provided by customer

Multilayer PCB manufacturing

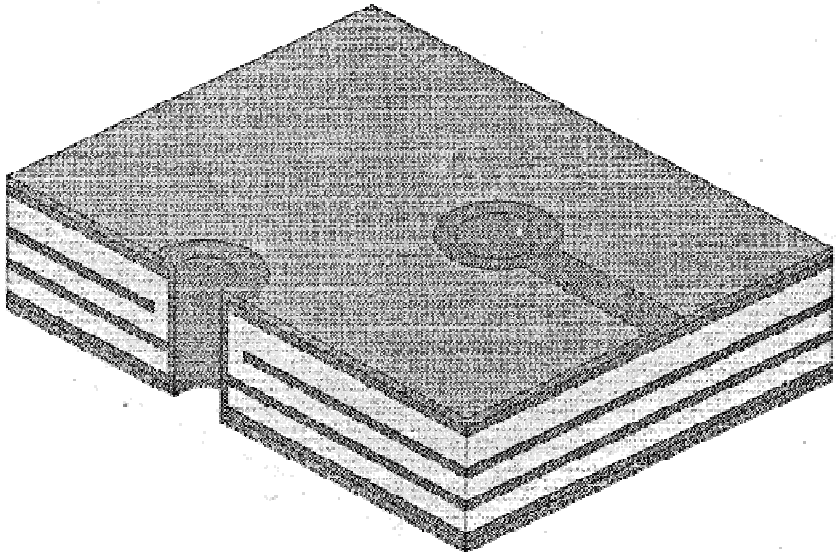


(7) *Electroless copper plate*
A thin layer of copper is deposited following smear removal, cleaning and preparation

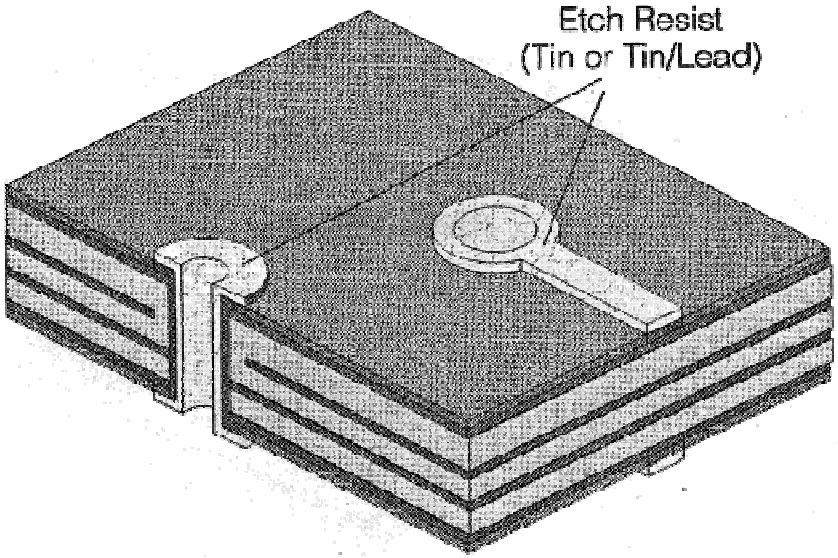


(8) *Apply plating resist*
The desired circuitry is left uncovered

Multilayer PCB manufacturing

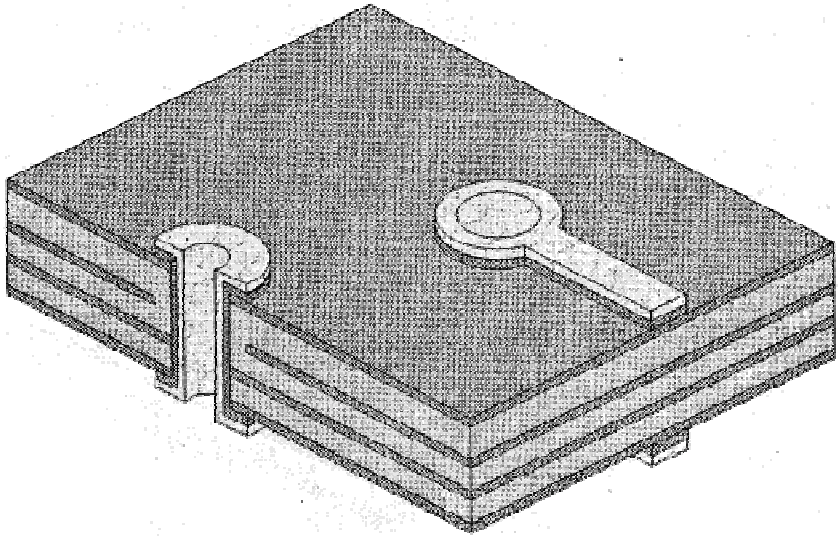


(9) *Electroplate copper*
The specified thickness is electrolytically deposited (usually 0.001”)

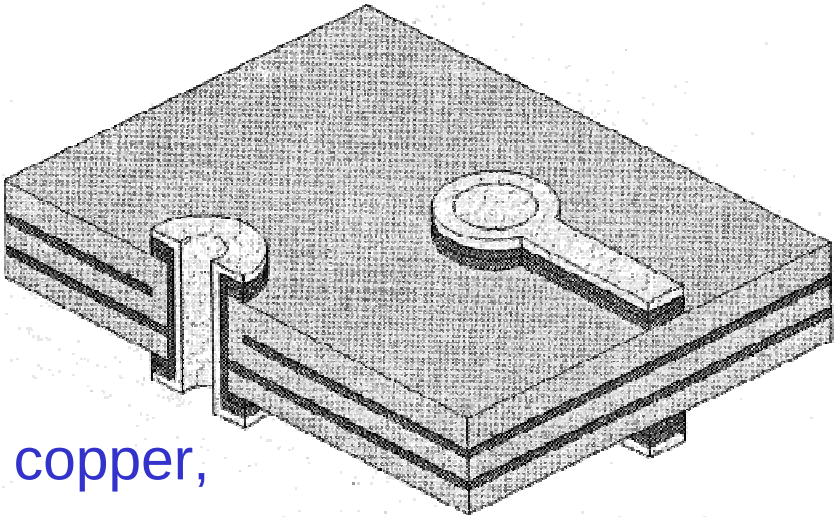


(10) *Electroplate etch resist*
Tin or tin/lead is electrolytically deposited over the copper plating

Multilayer PCB manufacturing

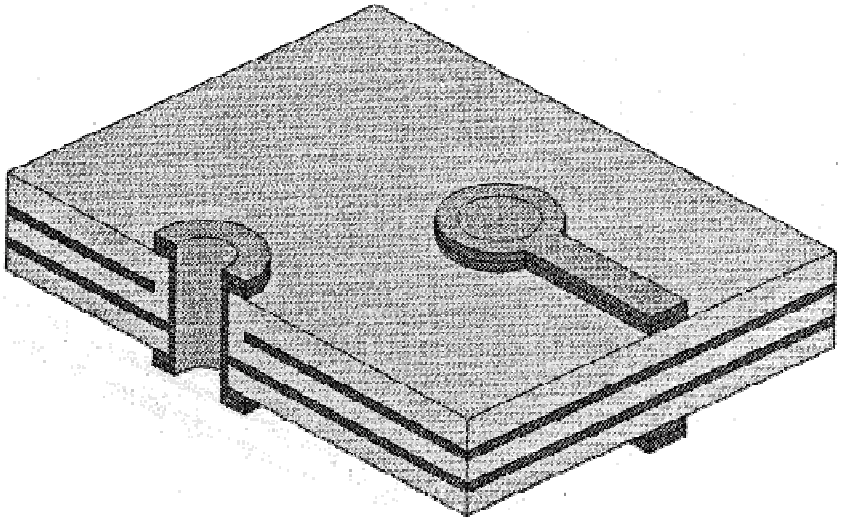


(11) *Strip plating resist*
Plating resist is chemically removed, revealing the copper surface

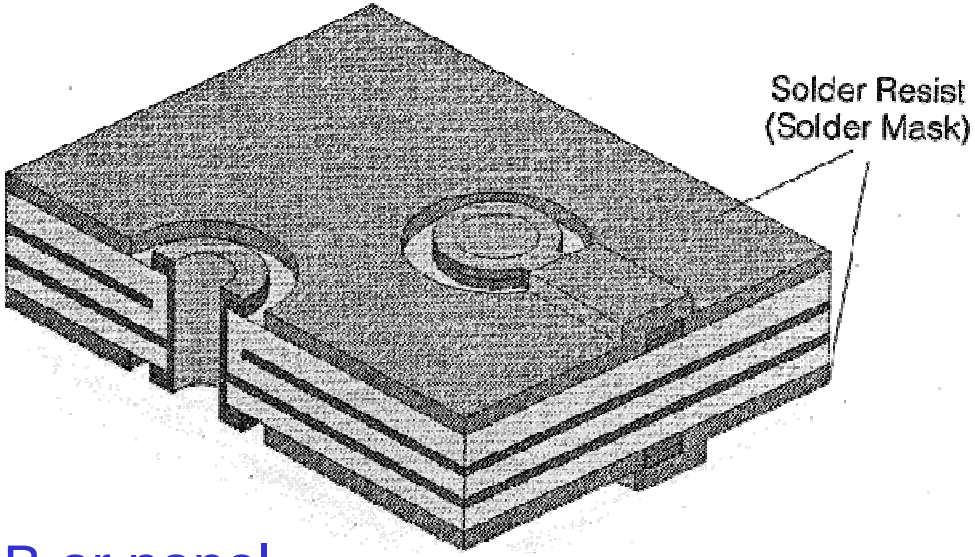


(12) *Etch*
The unwanted copper is removed chemically by an etchant that attacks copper, but not tin or tin/lead

Multilayer PCB manufacturing

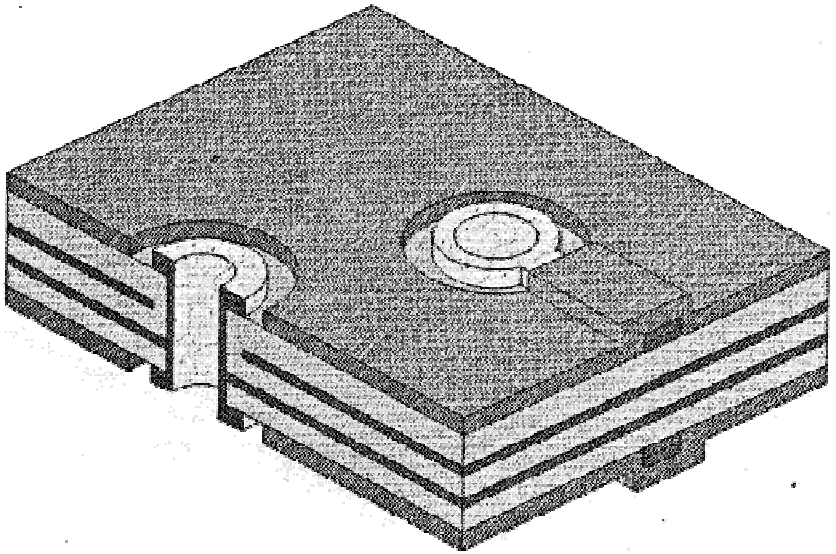


(13) *Strip etch resist*
The tin or tin/lead is chemically removed



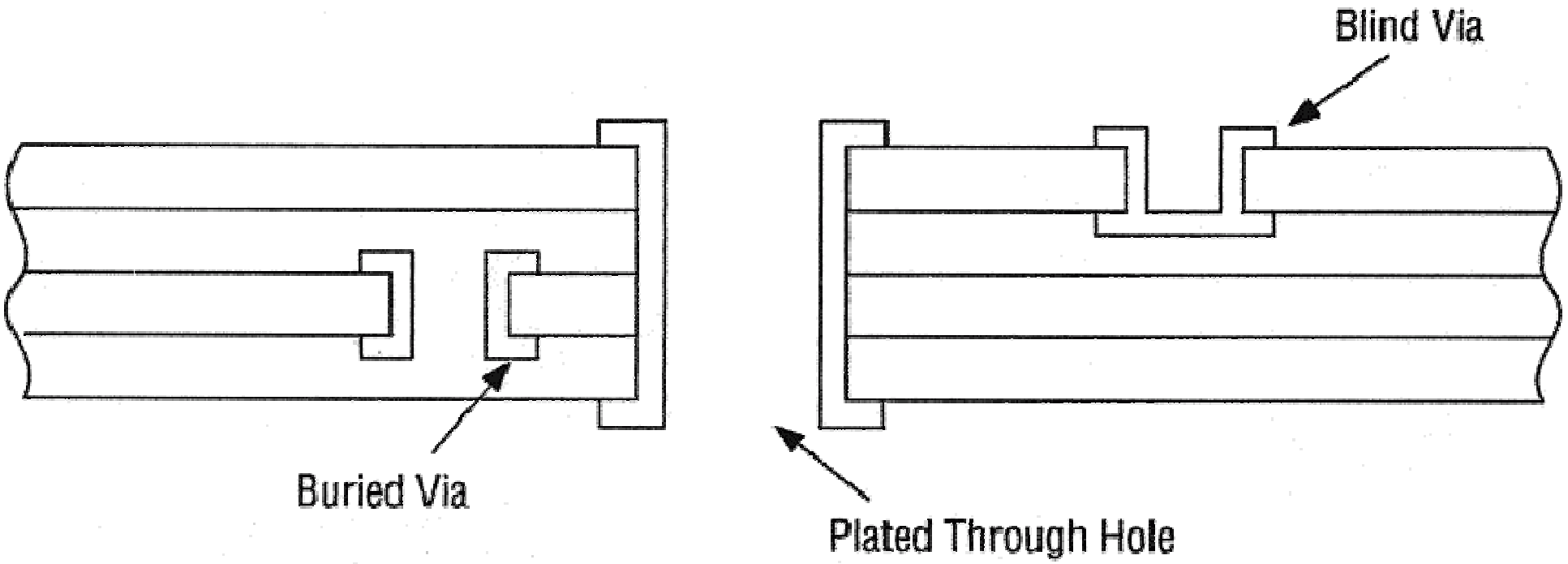
(14) *Apply solder resist*
The specified resist (dry film, liquid photoimageable or screen printed) is applied to the surfaces of the PCB or panel

Multilayer PCB manufacturing



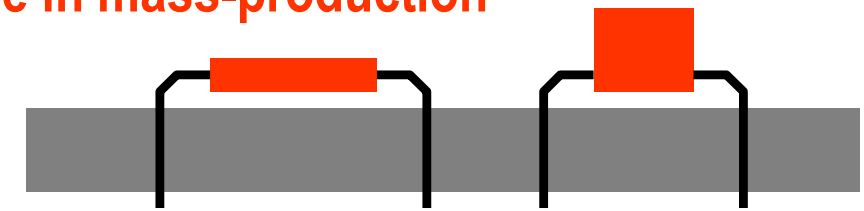
(15) *Solder coat*
Solder (tin/lead) is applied to the exposed copper areas and the excess solder is removed

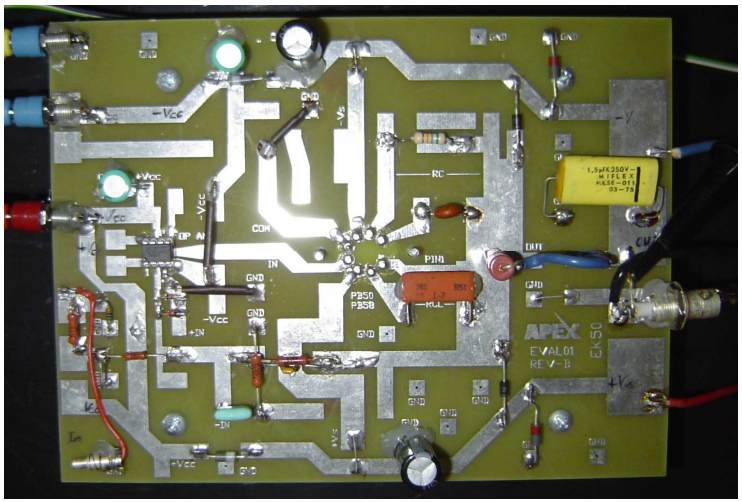
Through, blind and buried vias



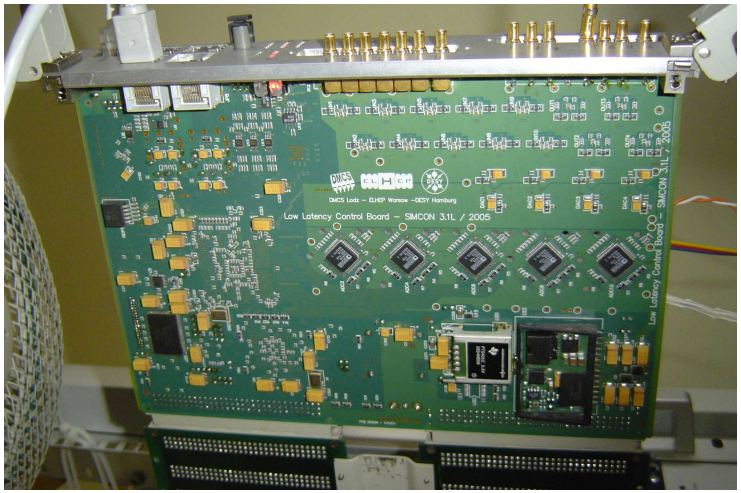
Mounting technologies

- **Through-hole technology**
  - provides stronger mechanical bonds
  - easy for design and modification (prototyping)
  - limited routing area due to the holes
  - expensive in mass-production





- **Surface-mount technology**
  - Low cost in mass-production
  - Smaller and more complex designs

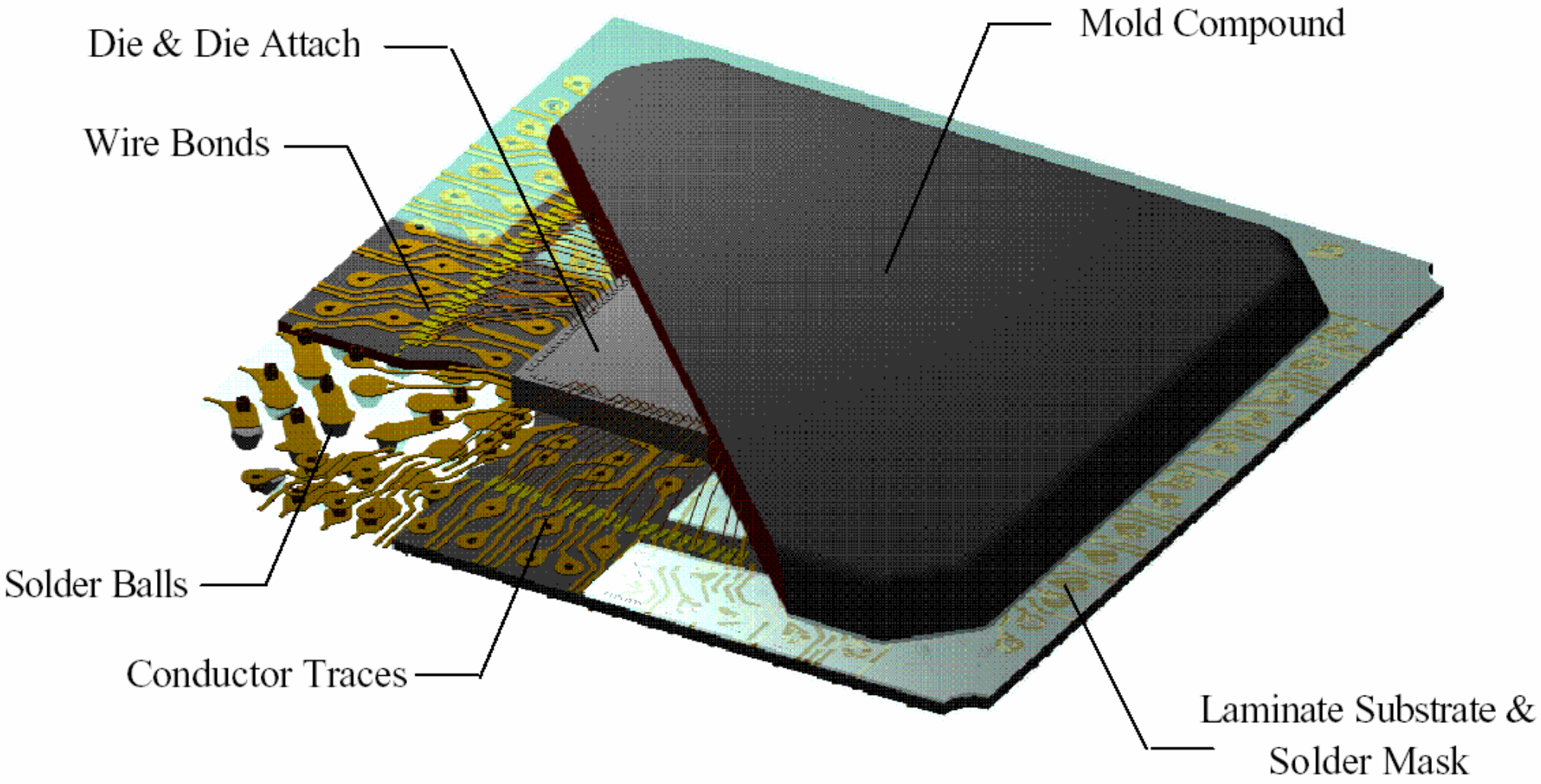


Mounting technologies (special)

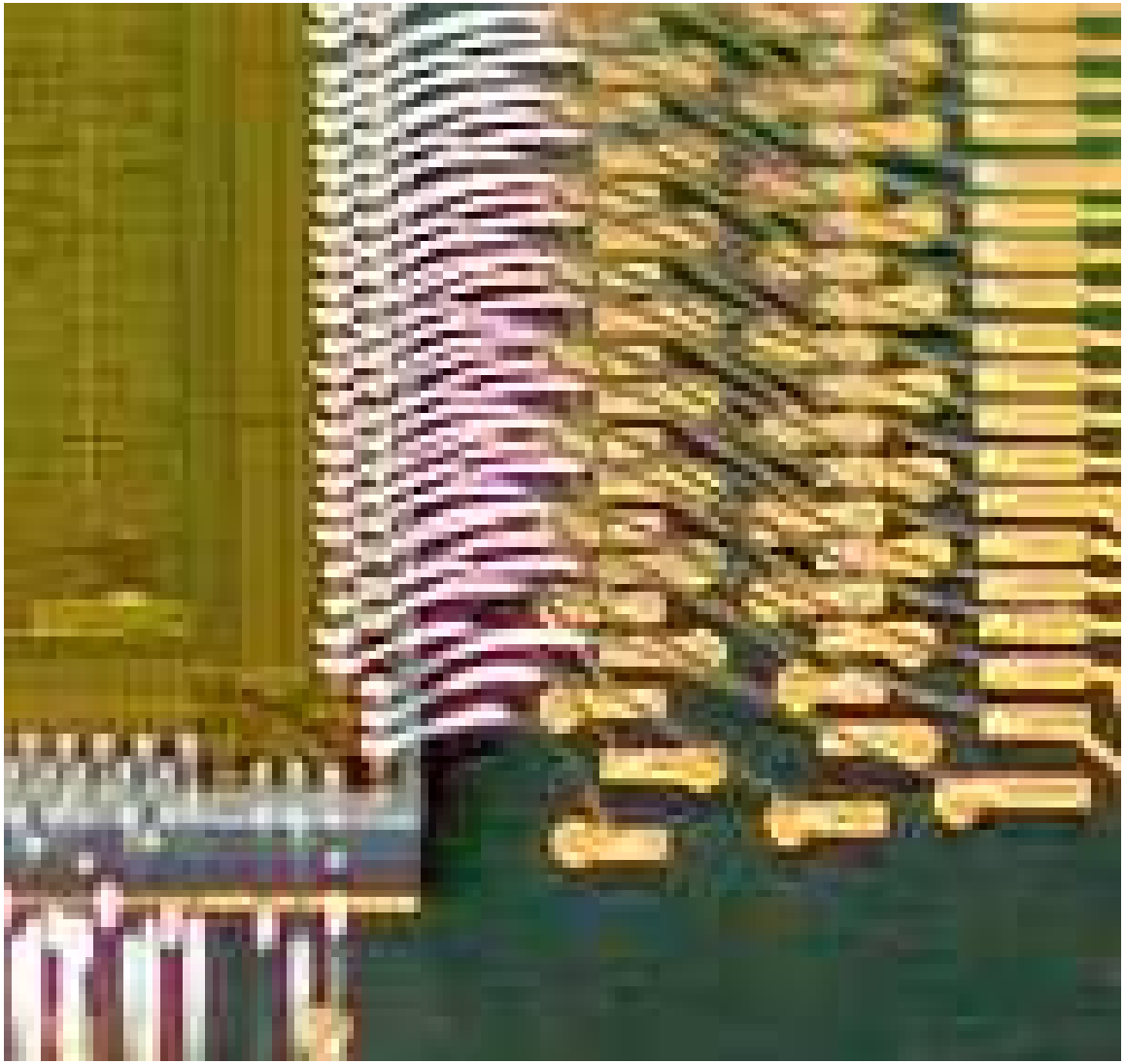
Cordwood module

Advantages: large space-saving
Application: i.e. missile guidance and telemetry systems

Package


Die & Die Attach
Wire Bonds
Mold Compound
Solder Balls
Conductor Traces
Laminate Substrate &
Solder Mask

Die interconnections



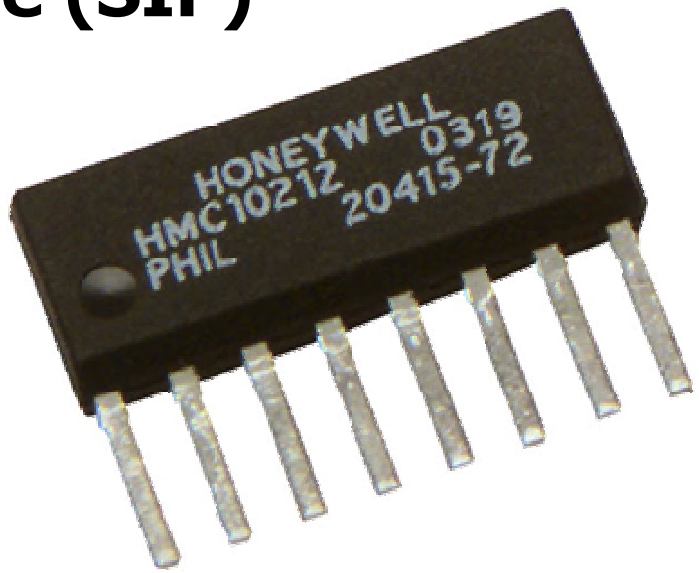
Types of IC packages

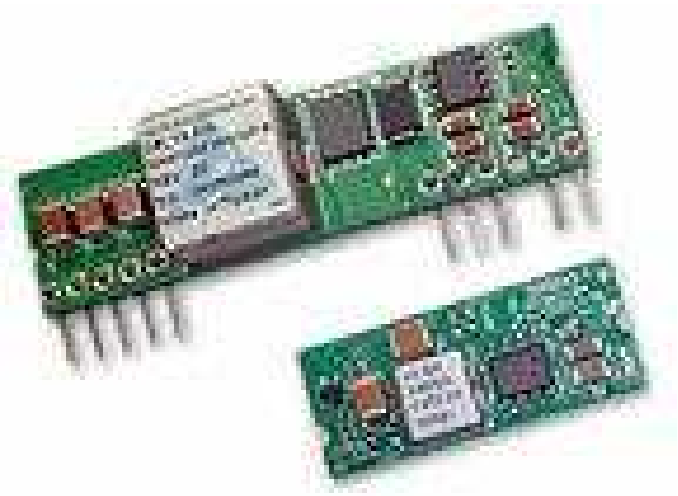
- Single in-line package (SIP)
- Dual In-line Package (DIP)
- Zig-zag in-line package (ZIP)

- Dual-in-line (SOIC, SOP, ….)
- Quad-in-line (PLCC, QFP, …
- Grid arrays (PGA, BGA, CGA, others)

Single in-line package (SIP)

- SIP is an electronic device package with a rectangular housing and one row of electrical connecting pins



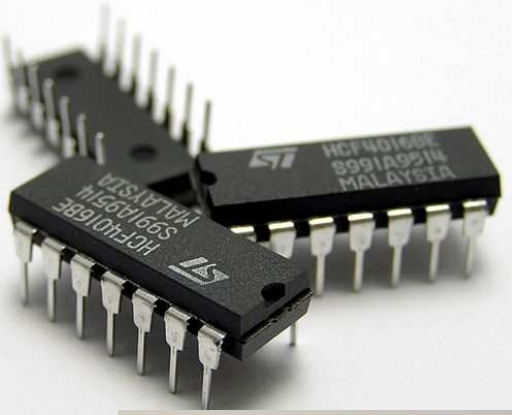


Currently the whole subsytsems might be encapsulated in SIP package

Dual In-line Package (DIP)

DIP (DIL) is an electronic device package with a rectangular housing and two parallel rows of electrical connecting pins, usually protruding from the longer sides of the package and bent downward.

The inter-lead spacing (lead pitch) is 0.1" (2.54 mm) and a row spacing is either 0.3 in (7.62 mm) or 0.6 in (15.24 mm).



DIPs were the mainstream of the microelectronics industry in the 1970s and 80s. Their use has subsided in recent years due to the emerging new surface-mount technology (SMT) packages such as PLCC and SOIC.

Zig-zag in-line package (ZIP)

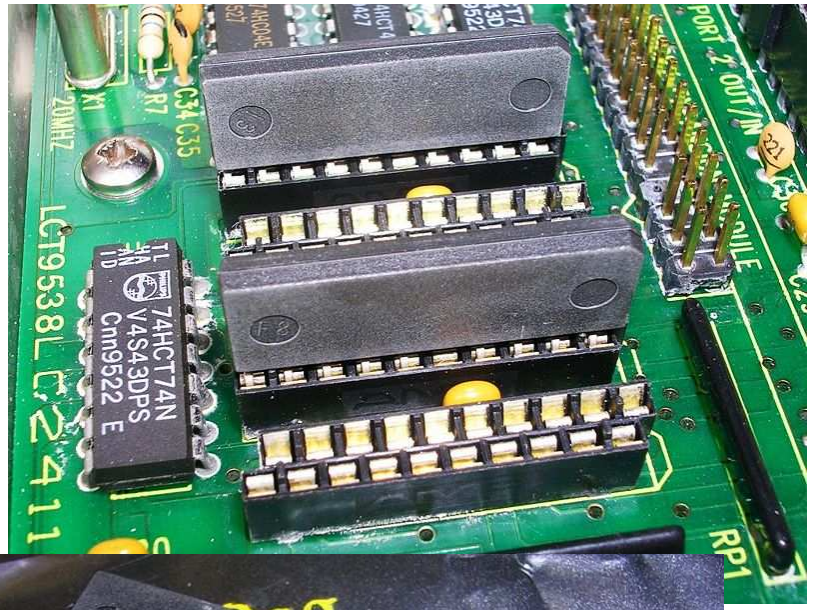
IC is encapsulated in a slab of plastic of dimension about 3 mm x 30 mm x 10 mm.

The package's pins protrude in two rows from one of the long edges (the rows are staggered by 1.27 mm (0.05"), giving them a zig-zag appearance)

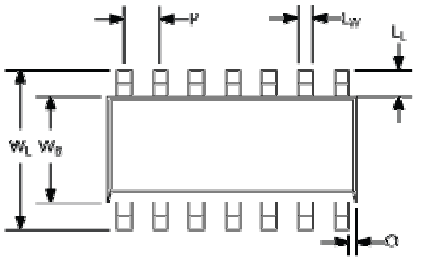
This solution allowing them to be spaced more closely than a rectangular grid would allow.

The pins are inserted into holes in a printed circuit board, with the packages standing at right-angles to the board, allowing them to be placed closer together than DIPs of the same size.

Currently ZIPs have been superseded by surface-mount packages such as the thin small-outline packages (TSOPs) used on single-in-line memory modules (SIMMs) and dual-in-line memory modules (DIMMs).

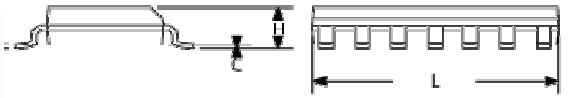


Dual-in-line Packages



- **Small-Outline Integrated Circuit (SOIC)**

  small-outline integrated circuit, dual-in-line, 8 or more pins, gull-wing lead form, pin spacing 1.27 mm

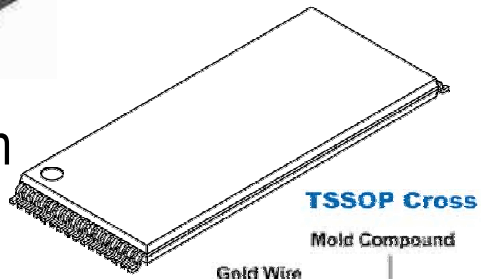


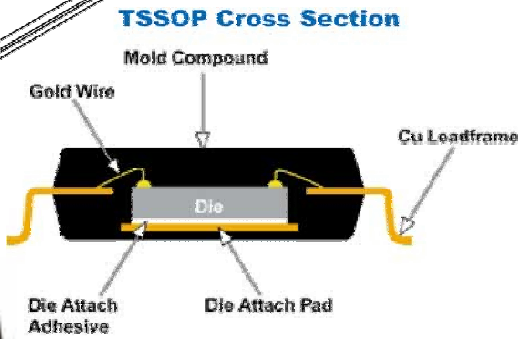
- **Small Outline Package (SOP),**

  with a pin spacing of 0.65 mm:

- **Thin small-outline package (TSOP),**

  thinner than SOIC with smaller pin spacing of 0.5 mm





- **Shrink small-outline package (SSOP)**

  pin spacing of 0.635 mm or in some cases 0.8mm

- **Thin shrink small-outline package (TSSOP)**

- **Quarter-size small-outline package (QSOP)**

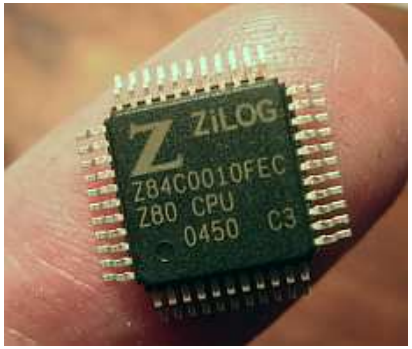
  with pin spacing of 0.635 mm

- **VSOP**

  even smaller than QSOP; 0.4, 0.5 mm or 0.65 mm pin spacing

- **other**

Quad-in-line packages



- **plastic leaded chip carrier PLCC**
  square, J-lead, pin spacing 1.27 mm
- **Quad Flat Package QFP**
  various sizes, with pins on all four sides
- **Low-profile Quad Flat Package LQFP**
  1.4 mm high, varying sized and pins on all four sides
- **plastic quad flat-pack PQFP**
  a square with pins on all four sides, 44 or more pins

- **ceramic quad flat-pack CQFP**
  similar to PQFP
- **Metric Quad Flat Pack MQFP**
  a QFP package with metric pin distribution
- **thin quad flat pack TQFP**
  a thinner version of PQFP
- **quad flat pack, no-leads QFN**
  smaller footprint than leaded equivalent

- **Leadless Chip Carrier LCC**
  contacts are recesses vertically to "whick-in" solder.
  Common in aviation electronics because of mechanical endurance against vibration.
- **others**

Grid array packages

- **Pin grid array (PGA)**
- **Ball grid array (BGA)**

  with a square or rectangular array of solder balls on one surface, ball spacing typically 1.27 mm
- **Low profile fine pitch BGA (LFBGA)**

  with a square or rectangular array of solder balls on one surface, ball spacing typically 0.8 mm
- **Column grid array CGA**

  in which the input and output points are high temperature solder cylinders or columns arranged in a grid pattern.
- **Ceramic column grid array CCGA**

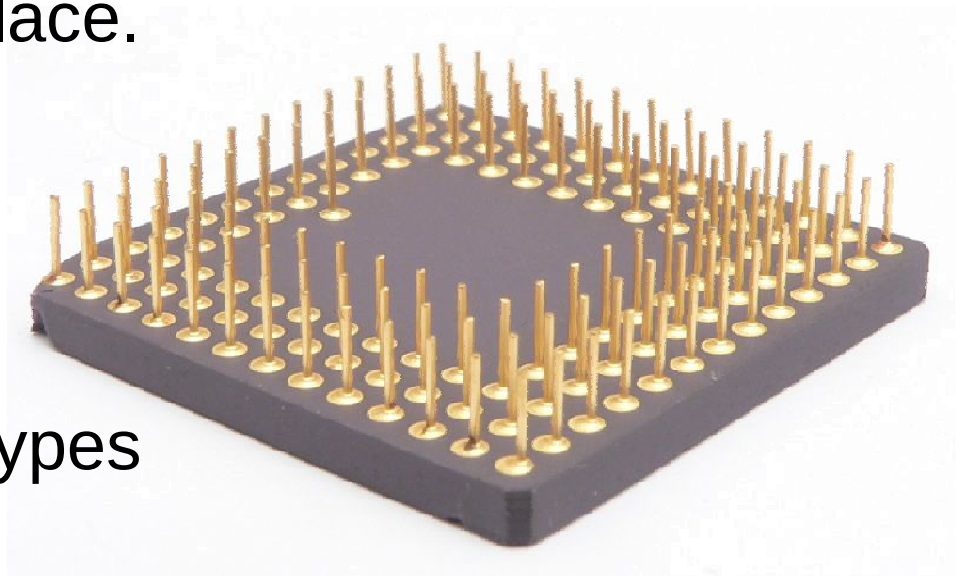
  in which the input and output points are high temperature solder cylinders or columns arranged in a grid pattern. The body of the component is ceramic.
- **micro-BGA µBGA,**

  with ball spacing less than 1 mm
- **Lead Less Package LLP**

  with metric pin distribution (0.5 mm pitch).

Pin Grid Array PGA

- The IC is mounted in a ceramic slab
- one face is covered, or partially covered, in a square array of metal pins.
- The space between pins is 2.54 mm (a tenth of an inch)
- The pins can then be inserted into the holes in a printed circuit board and soldered in place.



Advantages:

Less space occupation than older types such as the DIP.

Ball Grid Arrays BGA

The pins are replaced by balls of solder stuck to the bottom of the package.

Mounting:

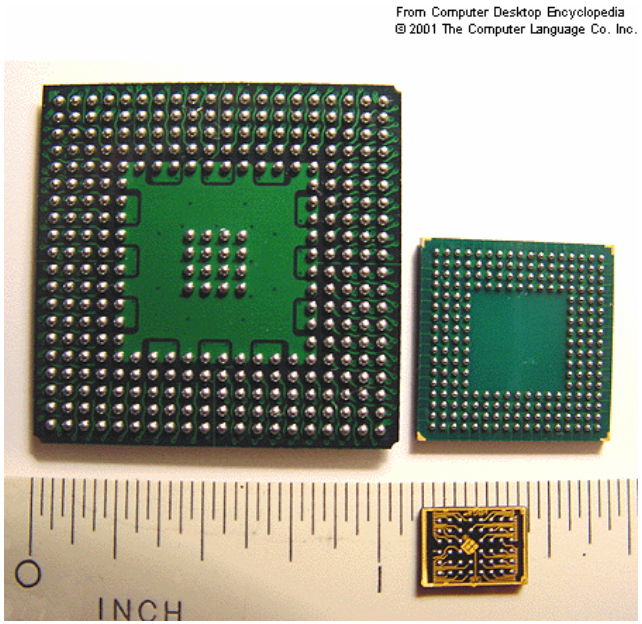
The device is placed on a PCB that carries copper pads in a pattern that matches the solder balls. The assembly is then heated, either in a reflow oven or by an infrared heater, causing the solder balls to melt. Surface tension causes the molten solder to hold the package in alignment with the circuit board, at the correct separation distance, while the solder cools and solidifies.

Advantages:

- high density, no problems with soldering
- good heat conduction (good contact with PCB)
- Low connection inductance

Disadvantages

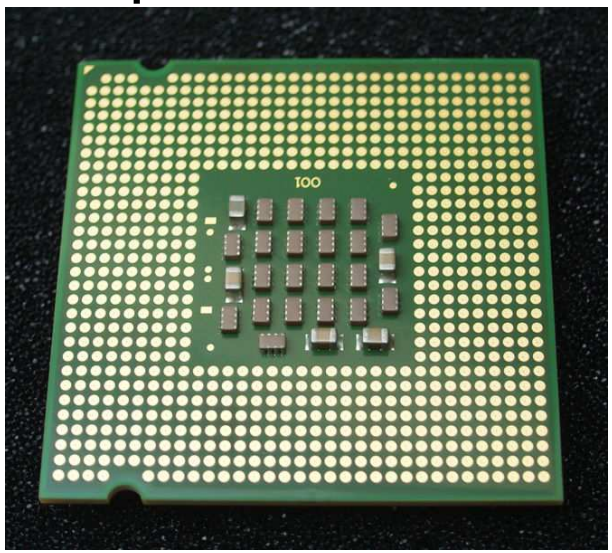
- Share stresses between BGA and PCB
- Hard inspection

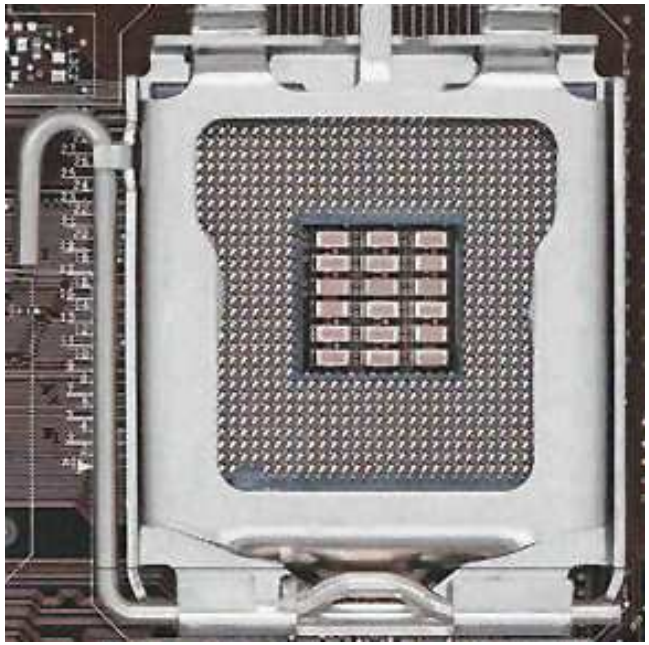


Land Grid Array LGA

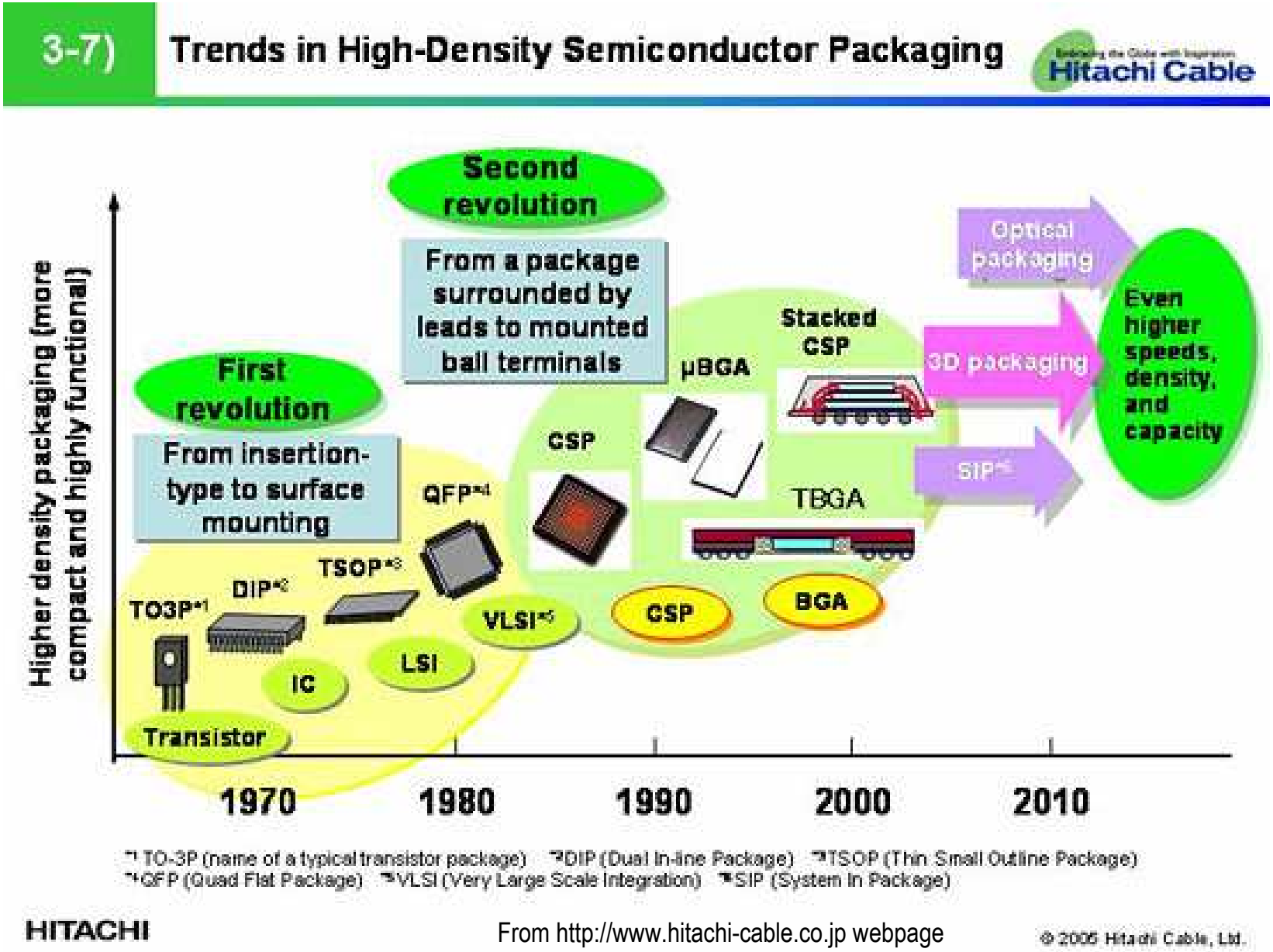
- Similar to Pin Grid Array but there are no pins on the chip;
- in place of the pins are **pads** of bare gold-plated copper that touch pins on the motherboard.

Application:
Intel Pentium 4, Intel Xeon,
Intel Core 2 and AMD Opteron families





Trends in IC packaging



From http://www.hitachi-cable.co.jp webpage

Non-packaged device

- surface mount, (require specific process for assembly)
- Types of non-packaged devices:
  - **chip-on-board (COB)**

    a bare silicon chip, that is usually an integrated circuit, is supplied without a package and is attached, often with epoxy, directly to a circuit board. The chip is then wire bonded and protected from mechanical damage and contamination by an epoxy "glob-top".
  - **chip-on-flex (COF)**

    as before, but a chip is mounted directly to a flex circuit.
  - **chip-on-glass (COG)**

    as COB, but chip is mounted directly to a piece of glass - typically an *LCD display*

Flex circuit assembling

It is not rare to use flex circuits ….

Olympus Stylus camera with skins removed, showing flex circuit assembly

from wikipedia.org

Thank you for your attention