Electronic Technology Design and Workshop

Presented and updated by

Przemek Sekalski

DMCS room 2

2007

Electronic Technology Design and Workshop

Lecture 5

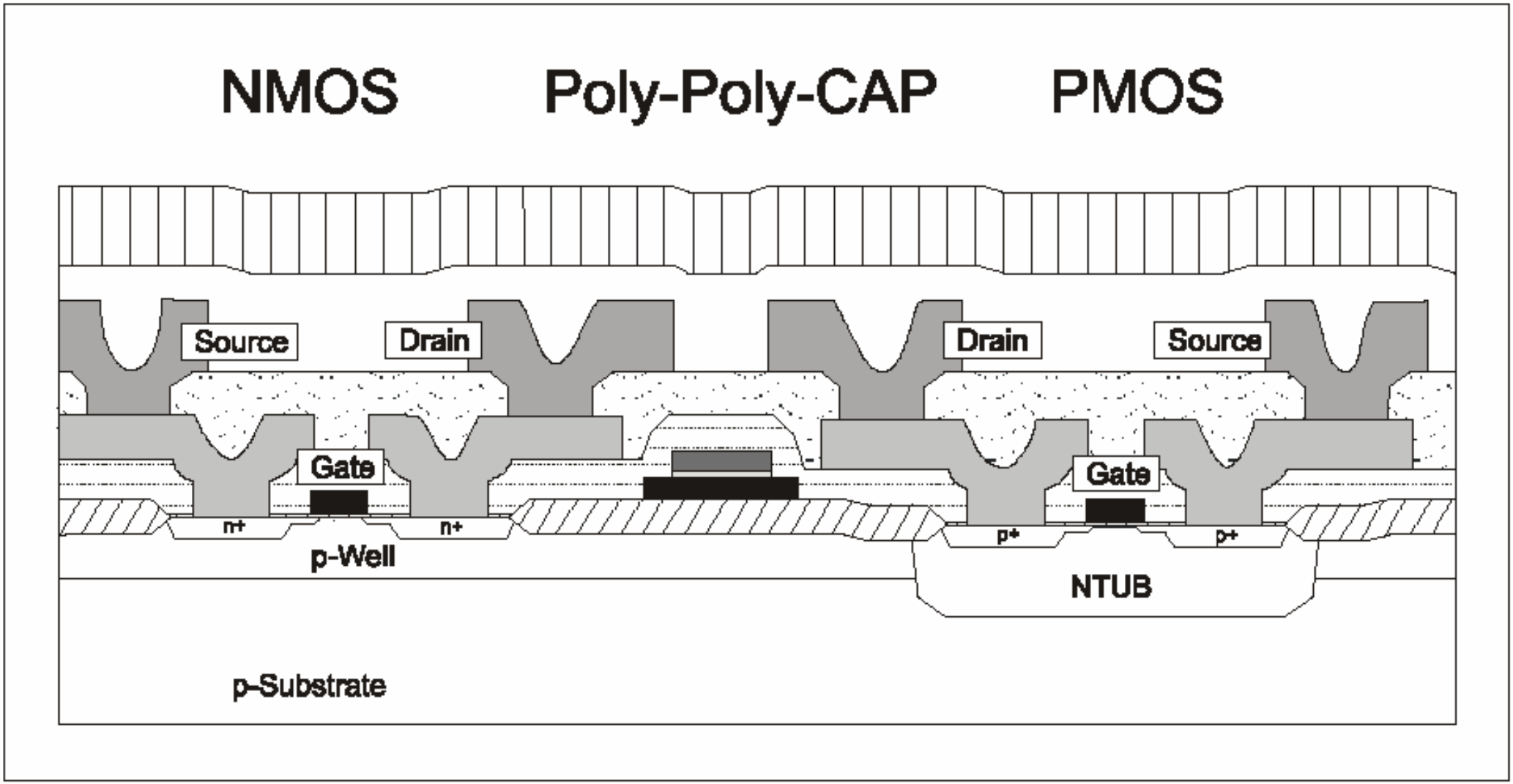
Microelectronics technology

Acknowledgement

During preparation of this lecture many photos and descriptions was taken from various web pages.

To clarify the lecture I have not included all web addresses however I acknowledge the invaluable support

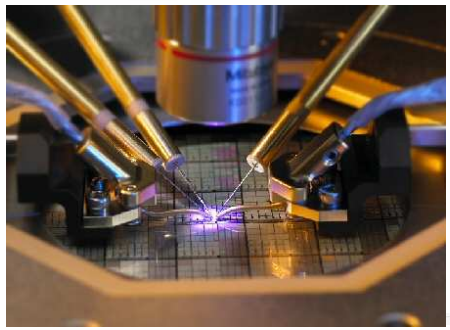
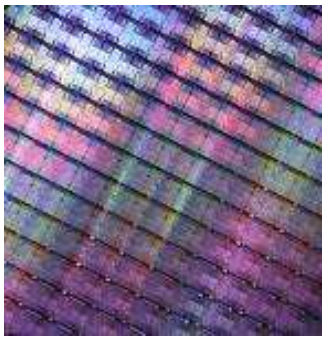
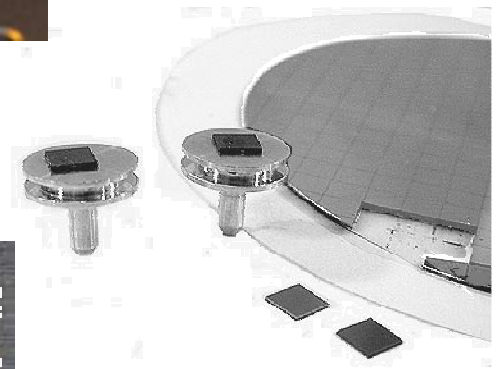
CMOS Structure



Silicon Integrated Circuits Technology

- Silicon wafer fabrication
- Silicon devices fabrication
- On-wafer testing
- Wafer-cutting
- Packaging
- Final testing



Silicon wafer fabrication

- Monocrystalic silicon fabricating
- Cutting
- Mechanical and chemical polishing

Monocrystalic silicon fabricating

Let’s dig the microchips … silica SiO_2…

Monocrystalic silicon fabricating

Pure silicon crystals are very rare (inclusions with gold and in volcanic exhalations).

Commonly silicon is found in the form of silicon dioxide SiO_2 (silica), and silicate.

Measured by mass, silicon makes up 26% of the Earth's crust.

It is, after oxygen, the second most abundant element on Earth.

Monocrystalic silicon fabricating

Silicon is commercially prepared by the reaction of high-purity silica with wood, charcoal, and coal, in an electric arc furnace using carbon electrodes. At temperatures over 1900 ℃, the carbon reduces the silica to silicon according to the chemical equation:

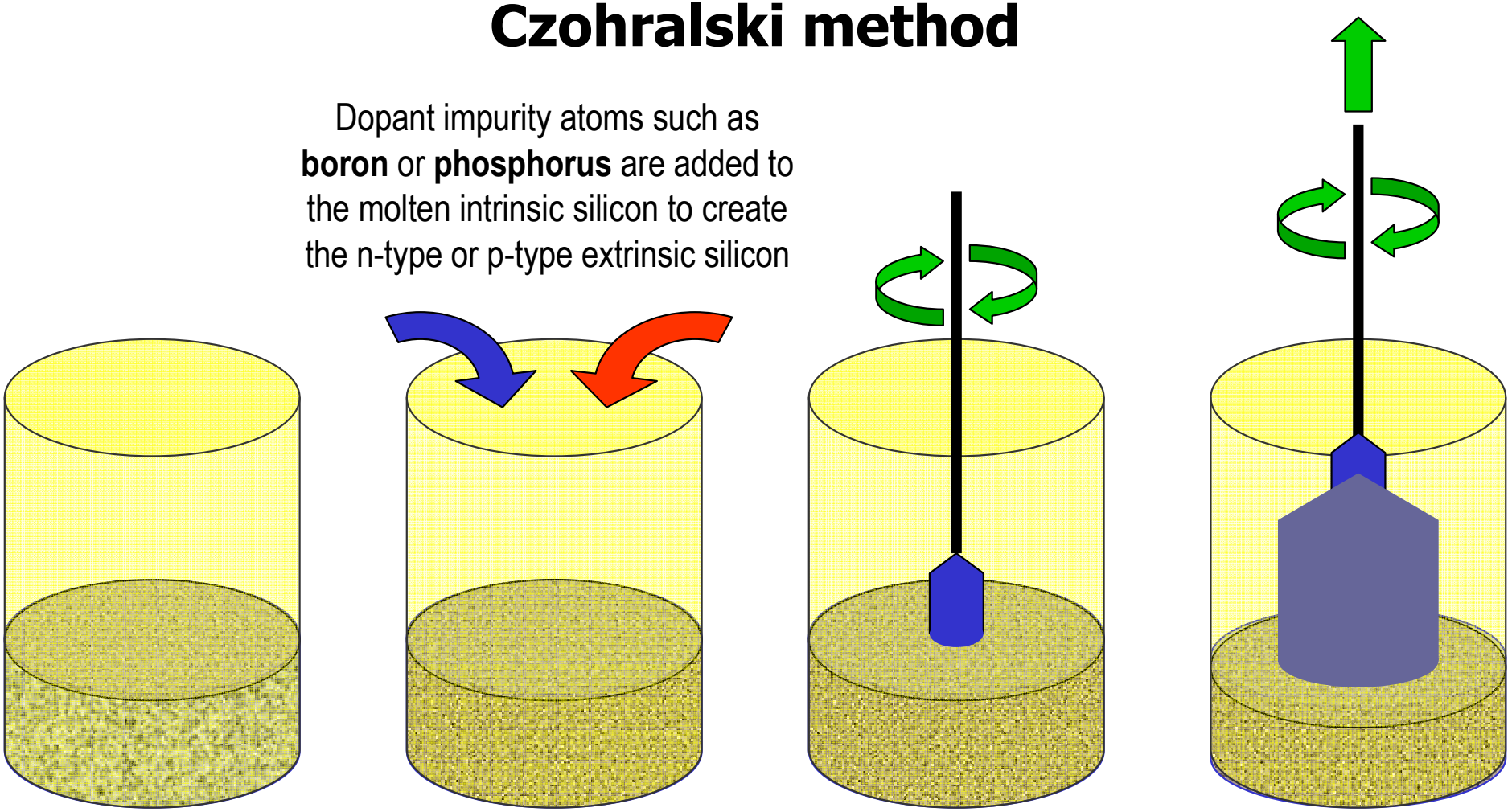
$$SiO_2 + C \rightarrow Si + CO_2.$$
$$SiO_2 + 2C \rightarrow Si + 2CO.$$

Crystal growing techniques:

- **Bridgman technique**
- **Czohralski technique (the most common)**
- **Float-zone silicon technique**

Czohralski method

Dopant impurity atoms such as **boron** or **phosphorus** are added to the molten intrinsic silicon to create the n-type or p-type extrinsic silicon



Silicon chunks with silica

Molten silicon
1600-1900 °C
Si melting point 1414 °C

Seed silicon monocrystal insertion

Silicon ingot creation

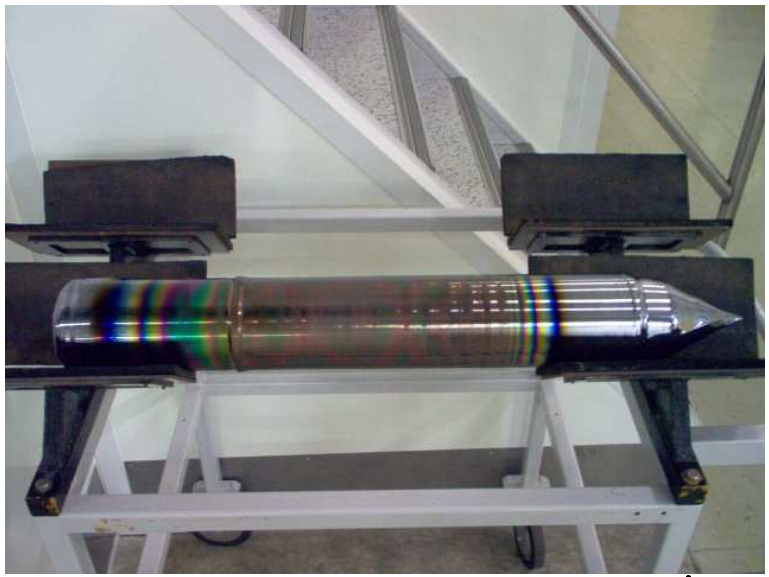
Whole process is done in the inert atmosphere, such as argon

Czohralski method

The process is named after Polish scientist Jan **Czochralski**, who discovered the method in **1916** while investigating the crystallization rates of metals

The ingots might be up to **1 to 2 metres** long and the diameter is around **200 mm and 300 mm**.

The largest silicon ingots produced today are **400 mm** in diameter.

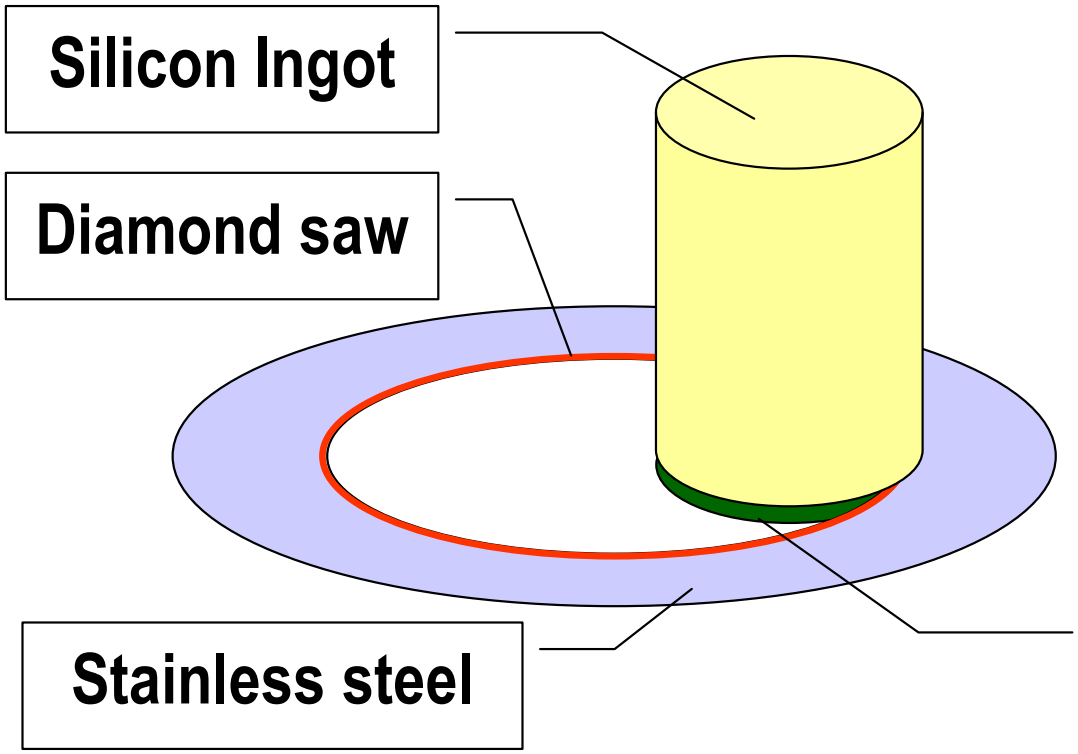


Monocrystalic silicon fabricating

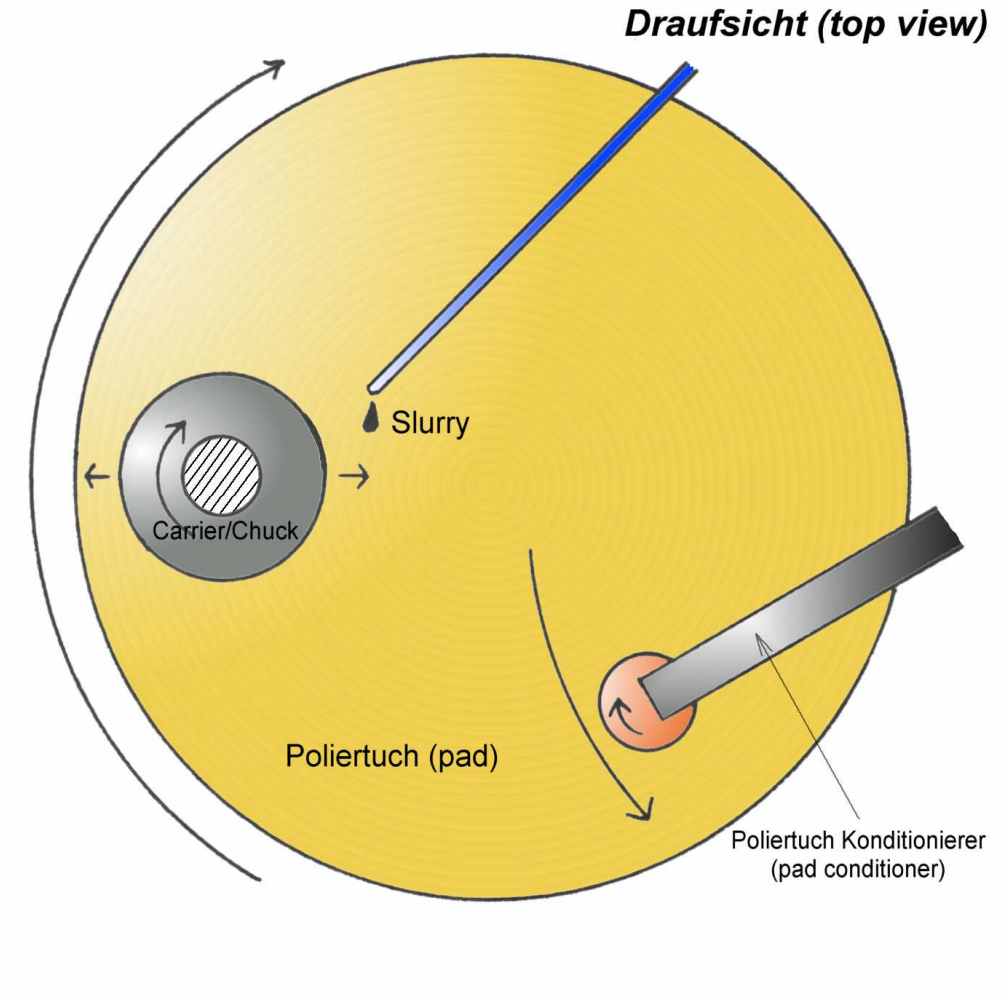
- Impurity atom concentration - less than 10^{13} at/cm^3
- One impurity atom per 10 billion atoms of silicon

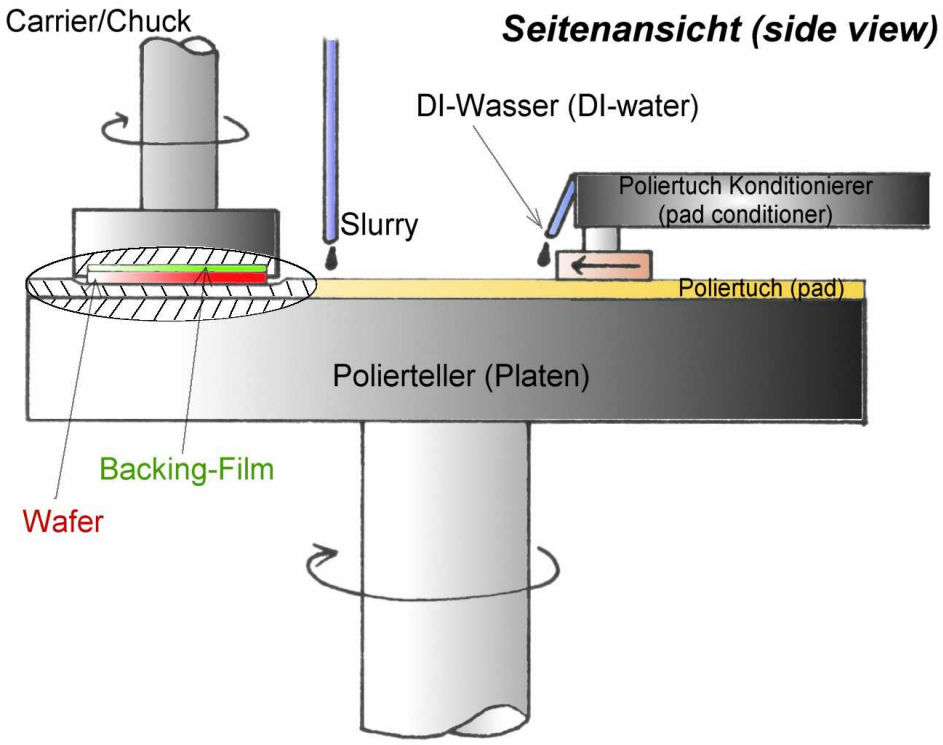
Monocrystal cutting

The ingot is cut into the wafer using the diamond saw.
(slices thickness around 0,5-1mm).
The wafer surface has many crystal net damages.
Mechanical and chemical polishing is needed.



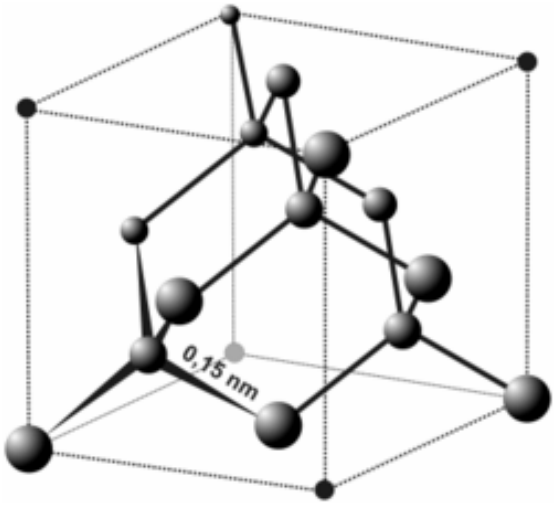
Mechanical and chemical polishing (CMP)

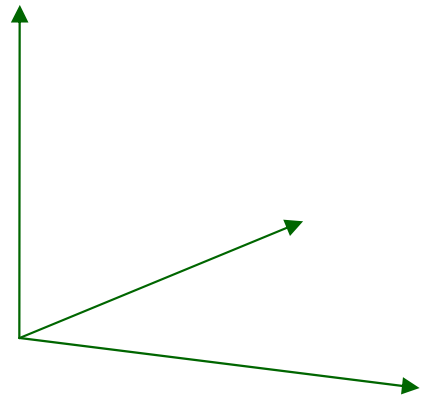


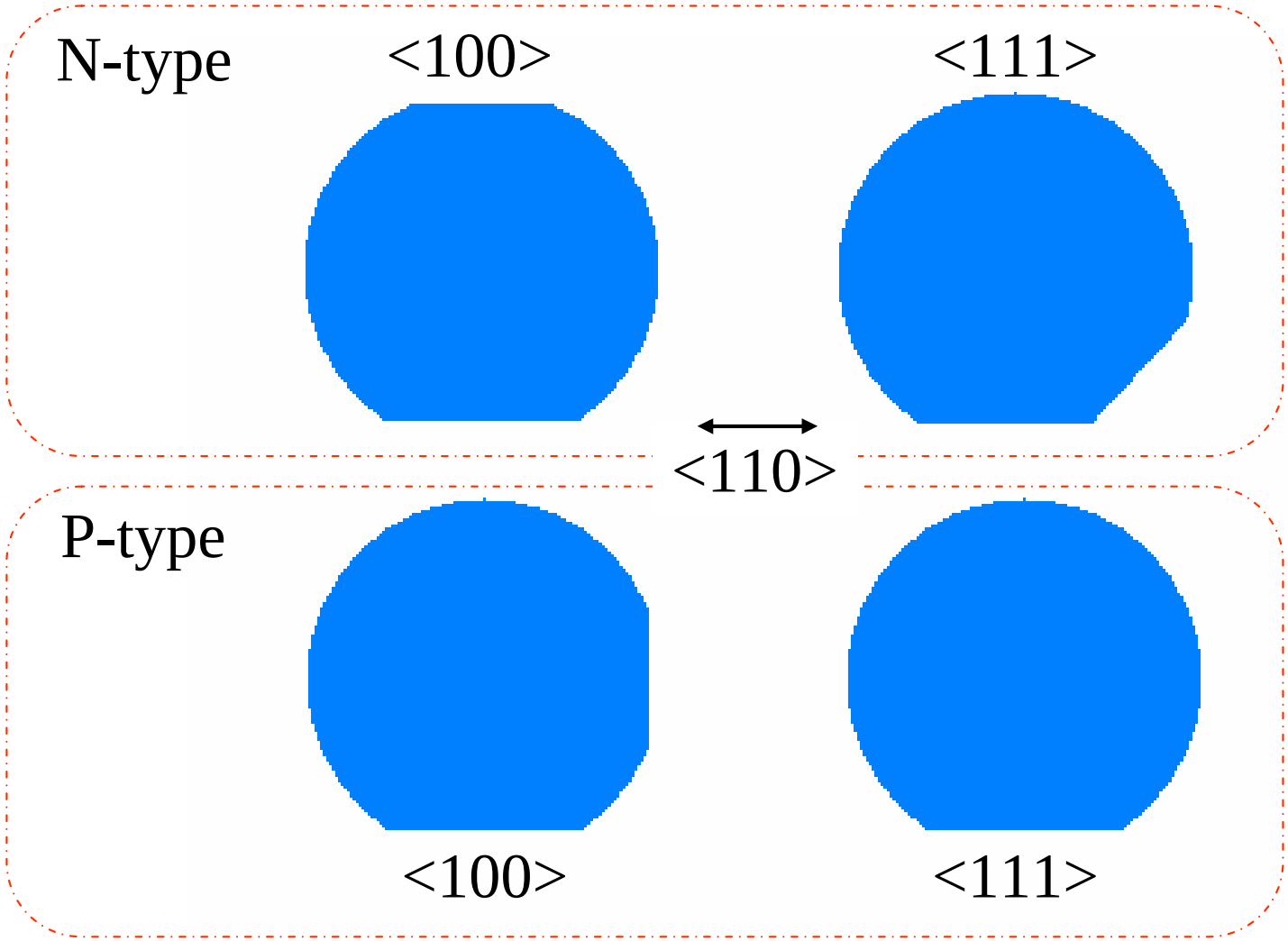


from wikipedia

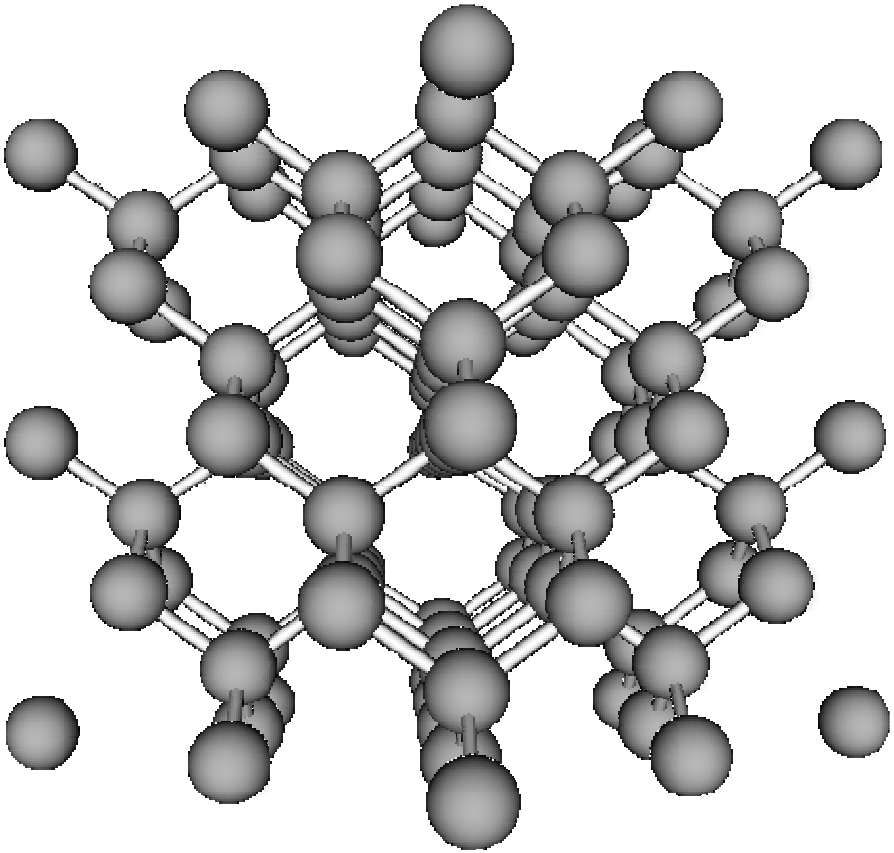
Crystal orientation markers



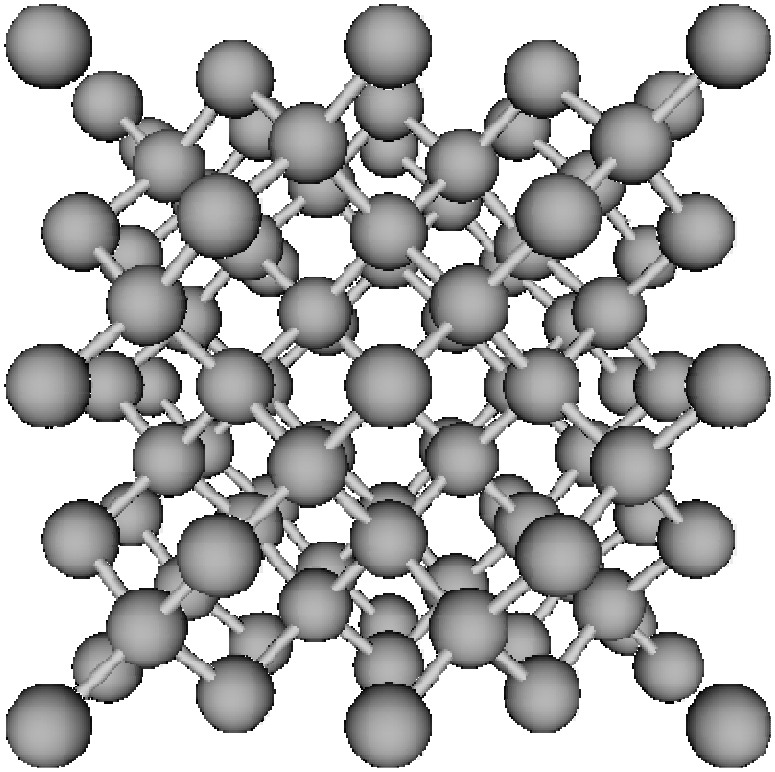




Some crystallography

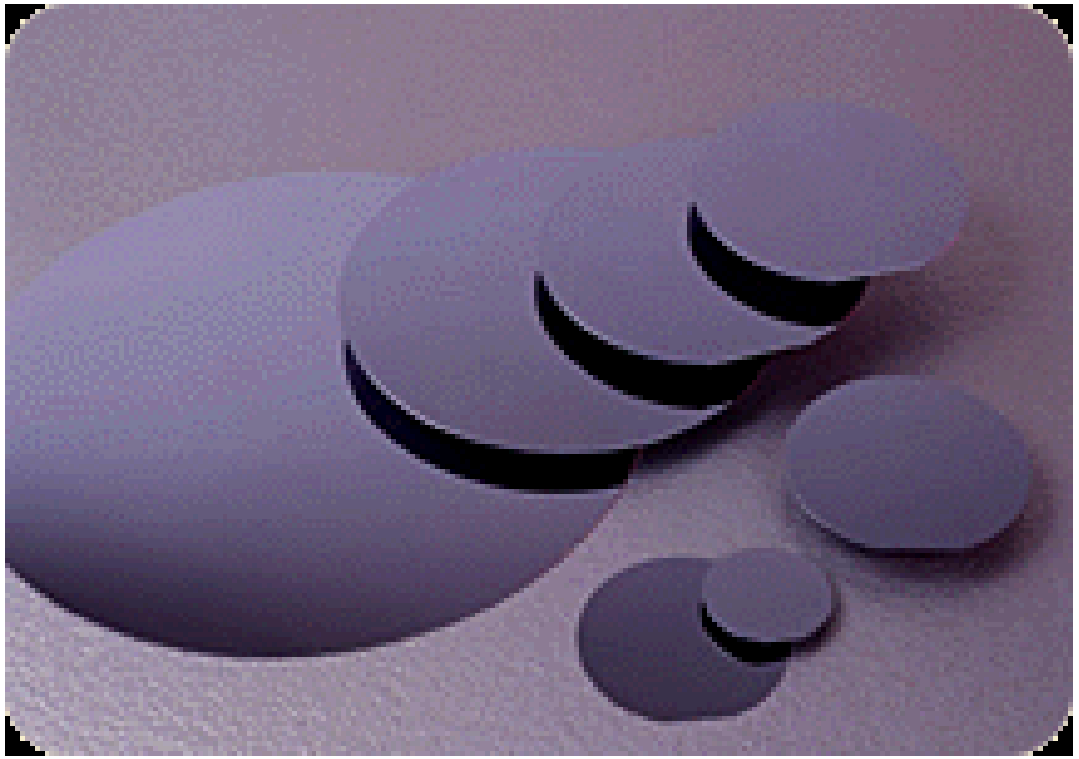


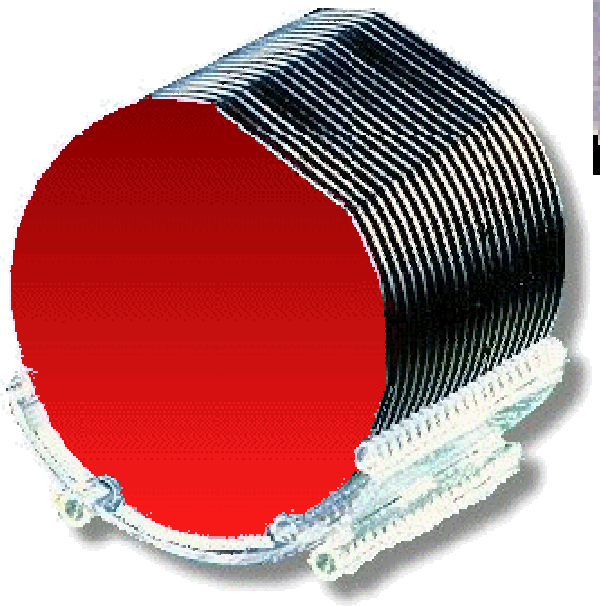
Silicon crystal seen along the <110> direction



Silicon crystal seen along the <100> direction.

Till now we have …
wafers





Technology Process Steps

initial oxide
first nitride deposition
NTUB mask
well etch (nitride)
NTUB implant
well oxidation
self aligned P-well implant
well drive-in
pad oxide
second nitride deposition
active area mask
active area etch (nitride)
N-field mask
N-field implant
field oxide
sacrificial oxide
Vt adjust implant
gate oxide
poly1 deposition
high-resistive implant
high-resistive mask
poly1 doping
capacitor oxide
poly2 deposition
poly2 doping
poly2 mask
poly2 etch
poly1 mask
poly1 etch
N-LDD mask
N-LDD implant
P-LDD implant
spacer formation
N+ implant mask
N+ implant
P+ implant mask
P+ implant
S/D anneal
BPSG deposition/reflow
contact mask
contact etch
plug implant mask
plug implant / anneal
barrier deposition
metal1 deposition
metal1 mask
metal1 etch
IMD / planarisation
via mask
via etch
metal2 deposition
metal2 mask
metal2 etch
passivation deposition
pad mask
pad etch
alloy
back side grinding

Silicon devices and interconnection fabrication

- Changing characteristic of material or new layer applying (deposition)
- (Photo) lithography
- Etching

Changing characteristic of material

- Doping by diffusion
- Doping by ion implantation
- Substrate oxidation

Diffusion

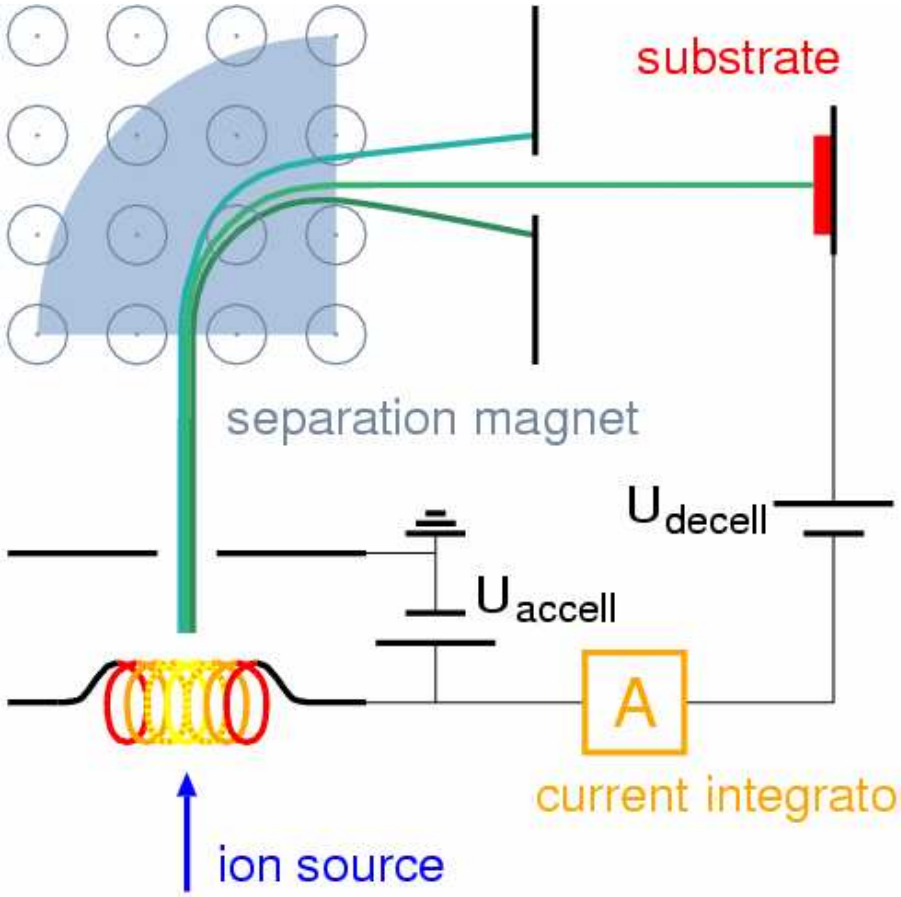
Physical phenomenon where particles such as impurity atoms in a semiconductor tend to flow from high concentration to low concentration

- Temperature 800 - 1200°C
- Boron, phosphor or arsenic atoms tend to penetrate the silicon
- Impurity atoms introduced by implantation, deposition, or epitaxy then diffuse during any high temperature steps in an IC process

Ion Implantation

Process by which ionized atoms are accelerated into semiconductor substrate through high electrical field

- Ion energy: hundreds keV
- Need of post-process heating
- Followed by diffusion
- High accuracy of the process



Substrate Oxidation

Grubość tlenku [nm]	Zastosowanie warstwy	Podstawowa metoda wytwarzania
2 - 6	tlenki tunelowe	utlenianie termiczne w suchym tlenie
15 - 50	tlenki bramkowe oraz kondensatorowe	utlenianie termiczne w suchym tlenie
20 - 50	tlenki "podkładowe" w technologii LOCOS	utlenianie termiczne w suchym tlenie
200 - 500	tlenki maskujące oraz pasywujące powierzchnię	utlenianie termiczne w parze wodnej lub CVD
300 - 1000	tlenki polowe	utlenianie termiczne w parze wodnej

Substrate Oxidation

Process where a layer of silicon dioxide is thermally grown on a silicon wafer

At elevated temperature, a gas containing oxygen or a water vapor flows through a furnace and onto a silicon surface causing a chemical reaction

Substrate Oxidation

- Temperature 950 - 1150°C
- In the growth of the oxide, the thickness of the silicon layer is consumed by 45%
- Speed depends on temperature and pressure
- Dry or wet:

$$Si + O_2 \rightarrow SiO_2$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

New layer deposition

Epitaxy (homo)

The growth of a single crystal semiconductor film on a single crystal substrate of the same semiconductor

Epitaxy (hetero)

The growth of semiconductor layers on substrates of different types

New layer deposition

- Chemical Vapour Deposition (CVD)
  - Low Pressure CVD (LPCVD)
  - Plasma Enhanced CVD (PECVD)
  - Ultrahigh vacuum CVD (UHVCVD)
  - And plenty others…

- Physical Vapour Deposition (PVD)
  - Evaporative deposition
  - Electron Beam Physical Vapor Deposition
  - Sputter deposition
  - Cathodic Arc Deposition
  - Pulsed laser deposition

Chemical Vapour Deposition

- Polycrystalic silicon - epitaxy

  950 - 1250 °C

$$SiCl_4 + SiH_4(silan) \rightarrow 2Si + 4HCl$$

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl$$

- Silicon nitride

  300 °C PECVD, 700 °C LPCVD

$$3SiH_4(silan) + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

- Silicon dioxide

  450-600 °C

$$SiH_4(silan) + O_2 \rightarrow SiO_2 + 2H_2$$

Physical Vapour Deposition

- Thin film technology
- Evaporation or ion bombing (sputtering)
- Metalisation

Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

Lithography

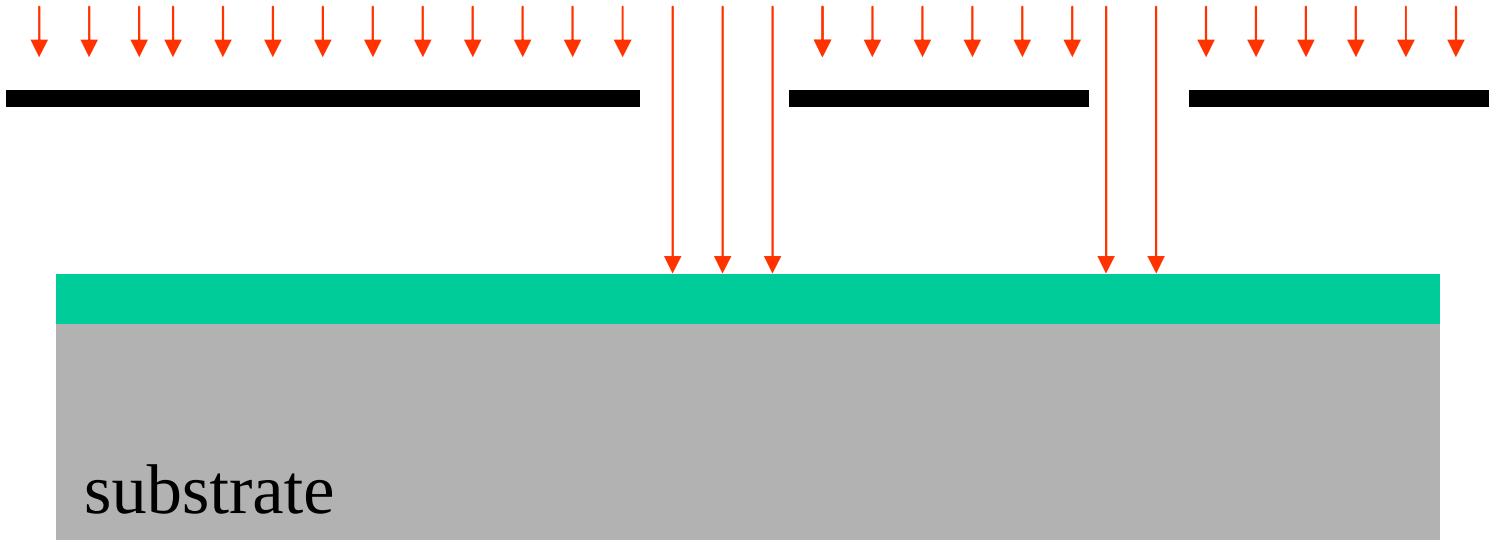
- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

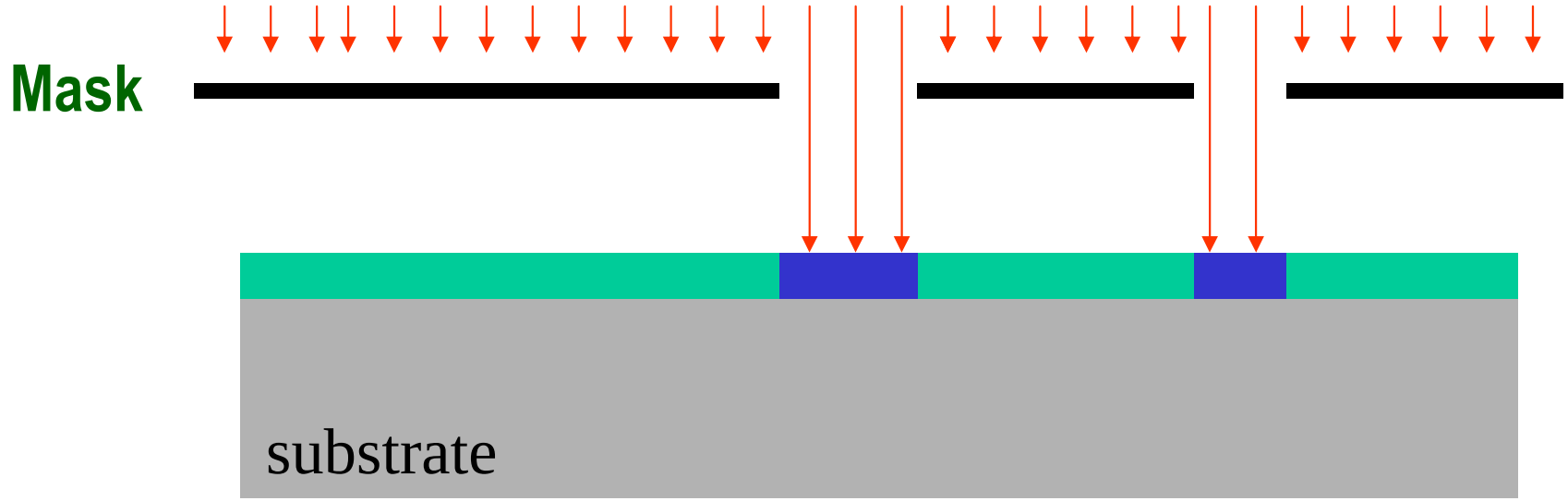
Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist



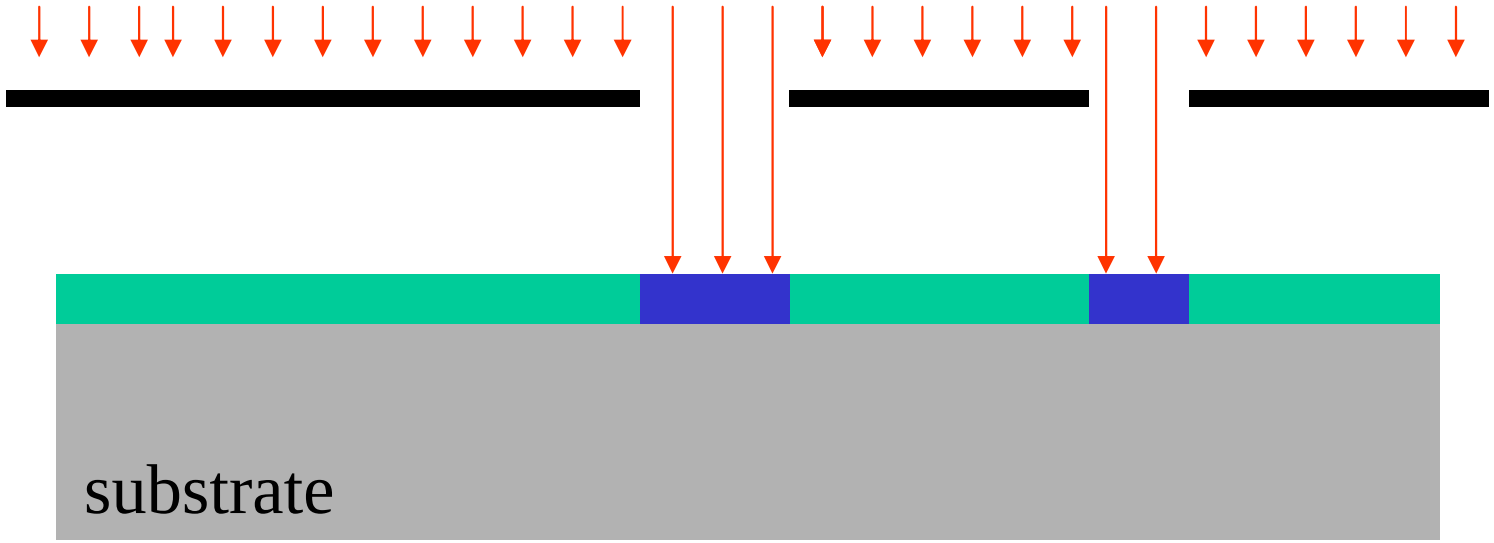
Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist



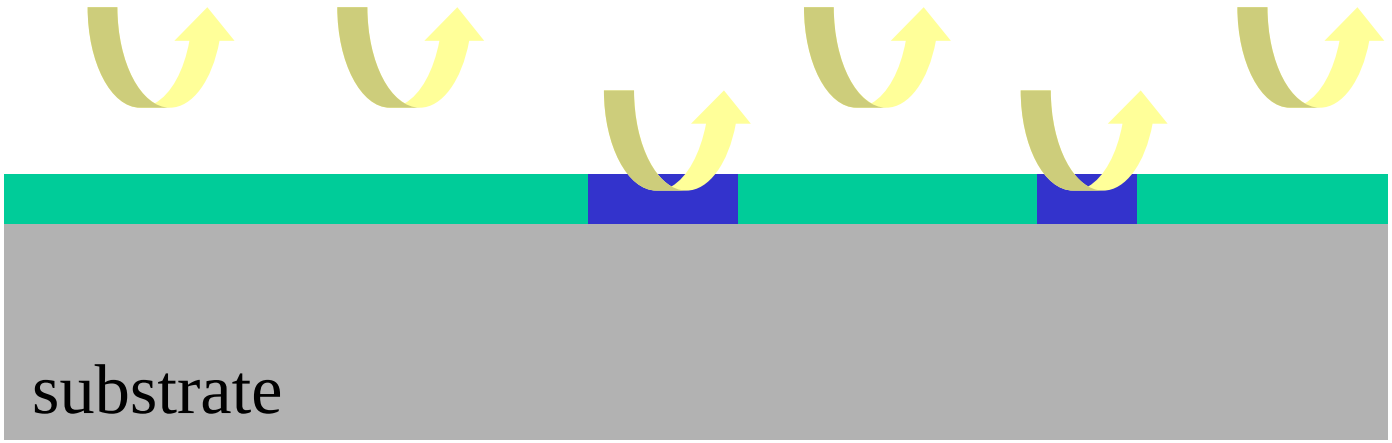
Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist



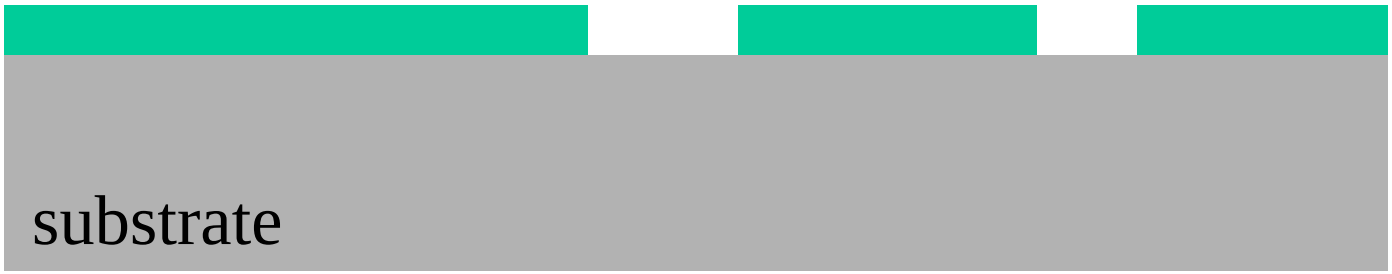
Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist



Lithography

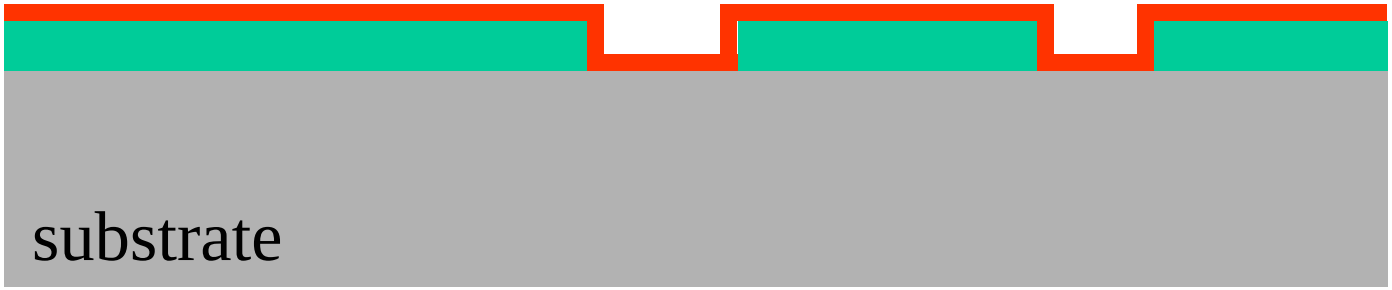
- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist



Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

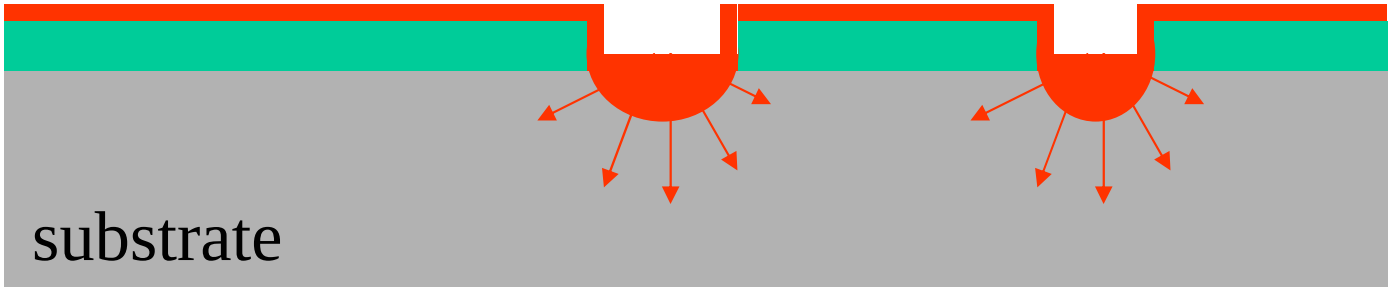
i.e. ion deposition



Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

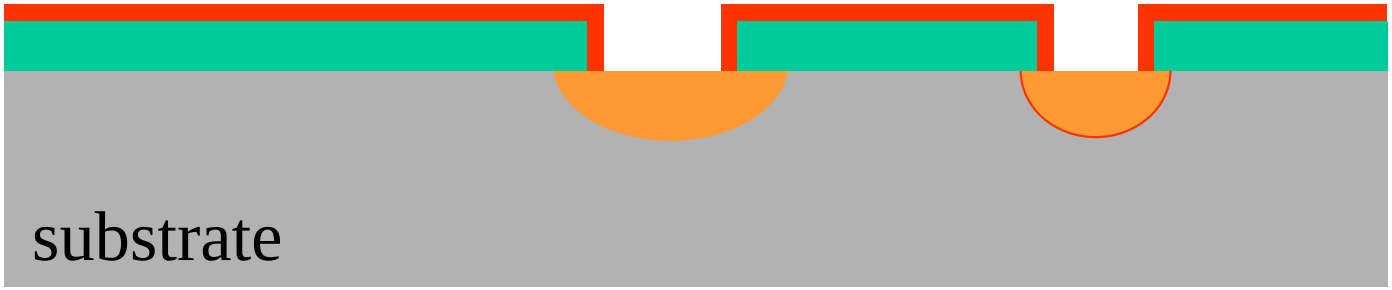
i.e. ion deposition and heating (diffusion)



Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

i.e. ion deposition and heating (diffusion)



Lithography

- Photoresist deposition on silicon wafer
- Exposition to UV light
- Light exposed or unexposed area dissolving (by soaking in a solution - called developer)
- Technological operation on exposed regions
- Chemical removing remaining photoresist

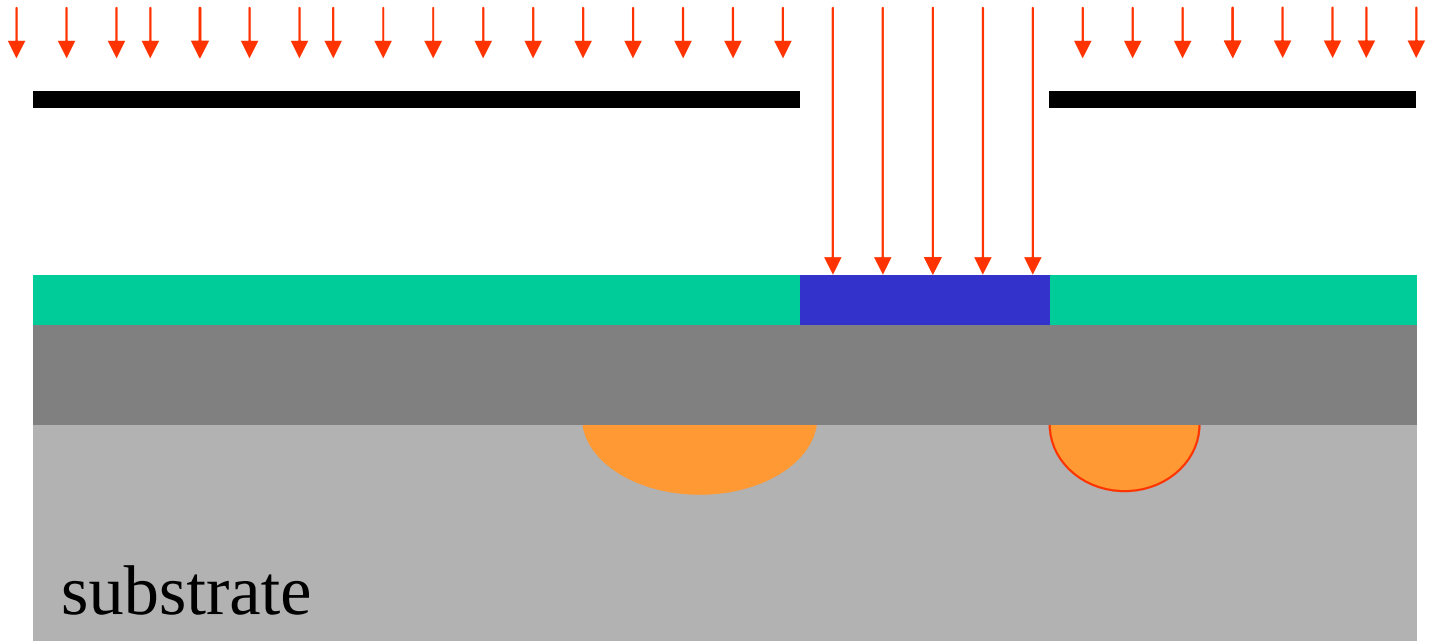
i.e. ion deposition and heating (diffusion)

Lithography

- Thin silicon dioxide deposition

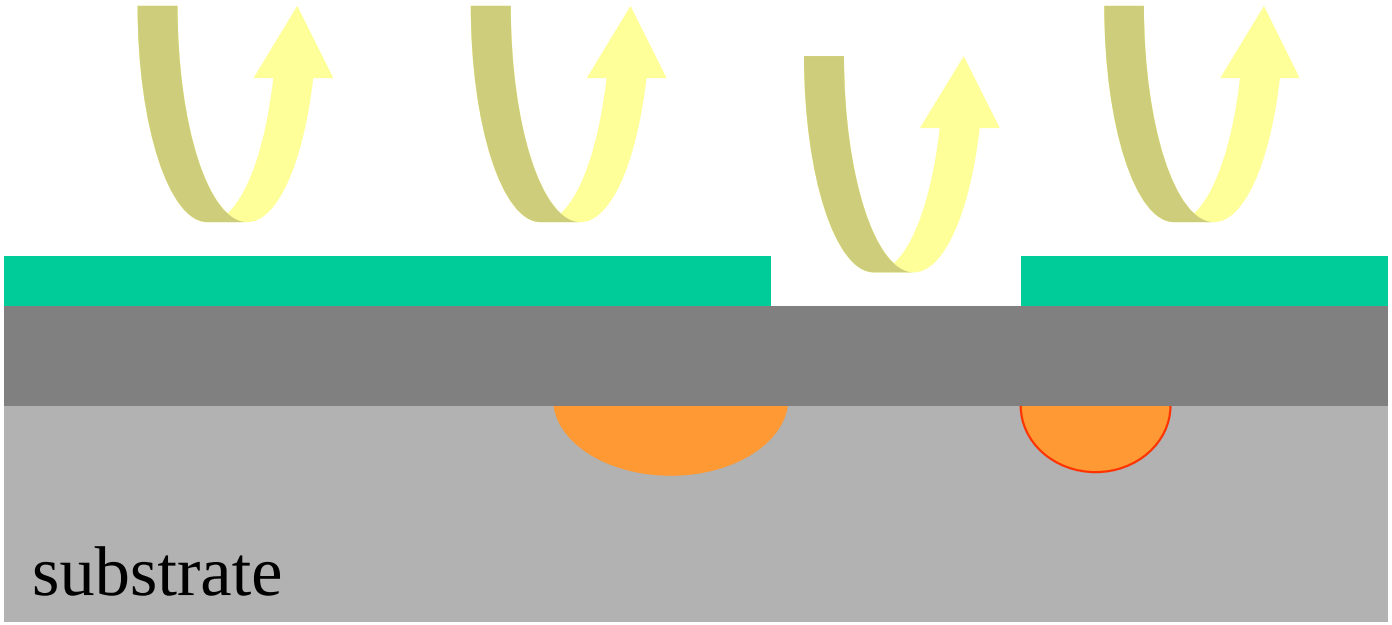
Lithography

- Photoresist deposition and exposition to UV



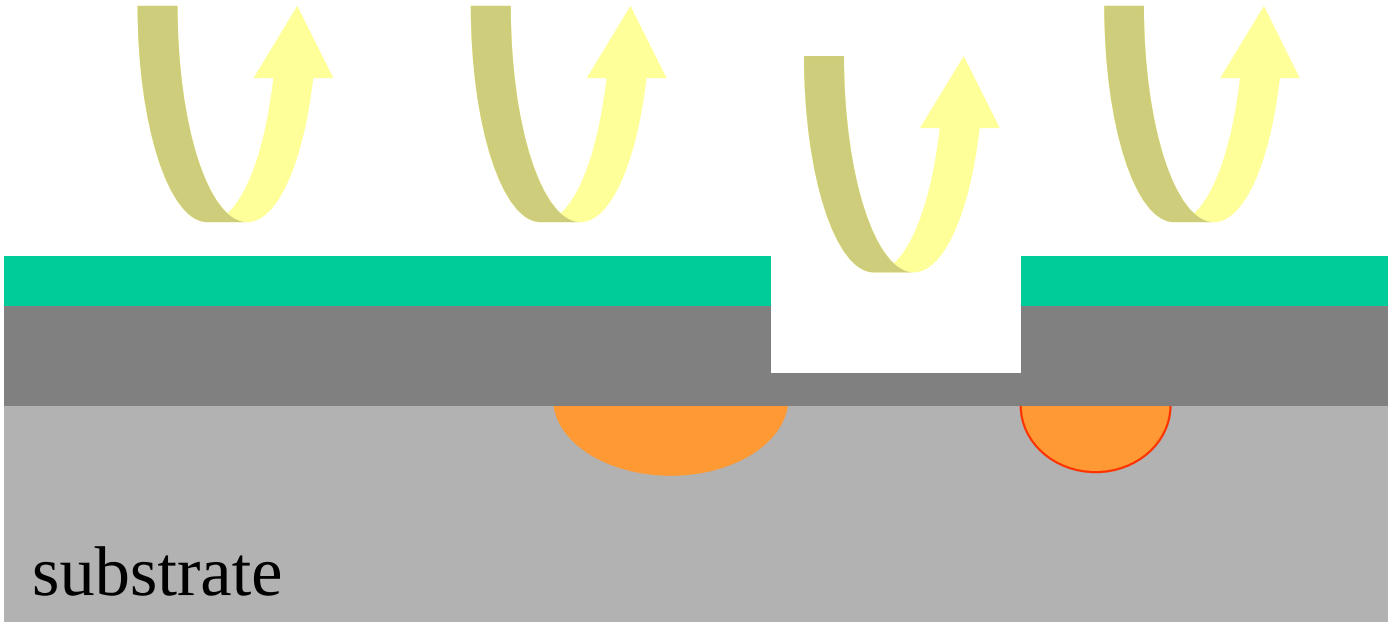
Lithography

- Etching



Lithography

- Etching



Lithography

- Polysilicon deposition

Lithography

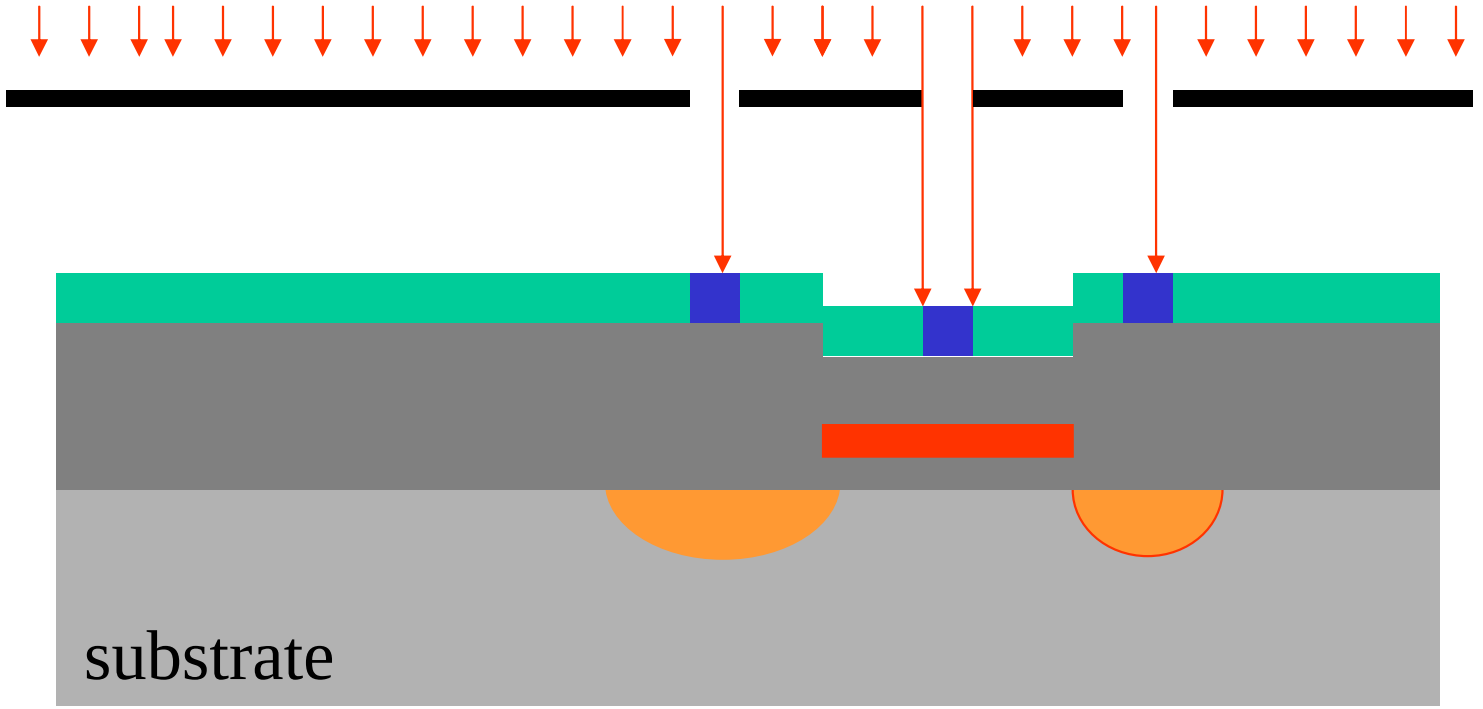
- Photoresist removal

Lithography

- Silicon dioxide deposition

Lithography

- Photoresist deposition and exposition to UV

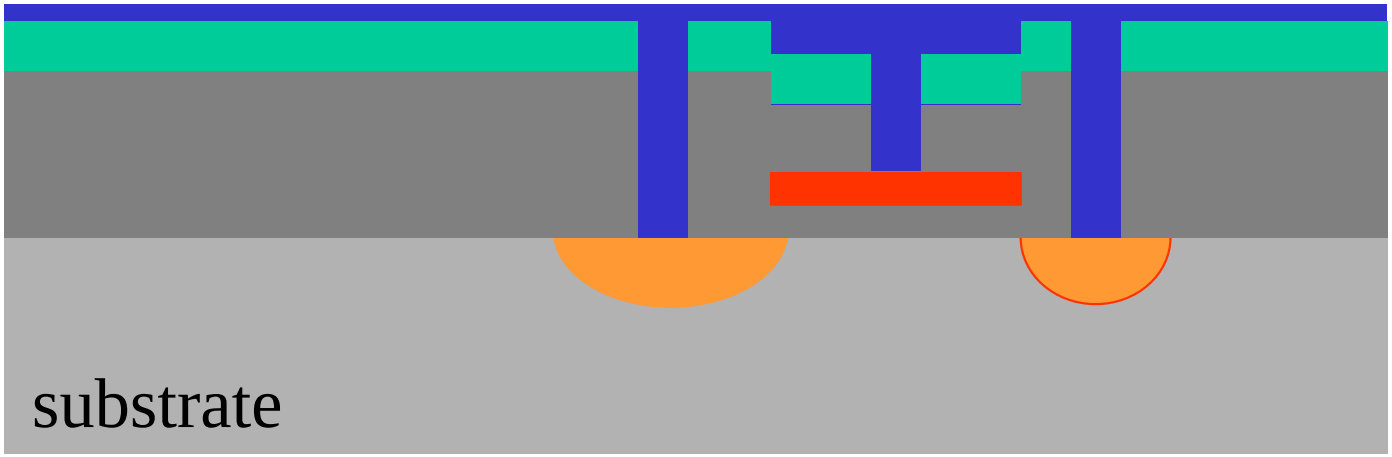


Lithography

- Etching

Lithography

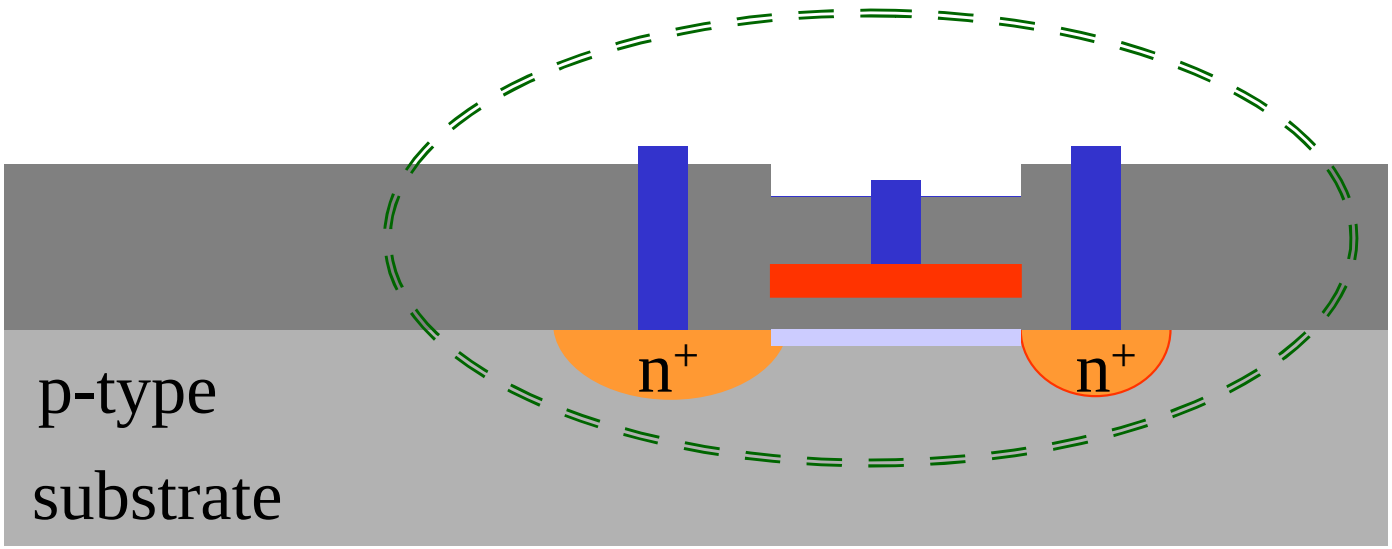
- Metalisation



Lithography

- Photoresist removal

Do you know this structure ?



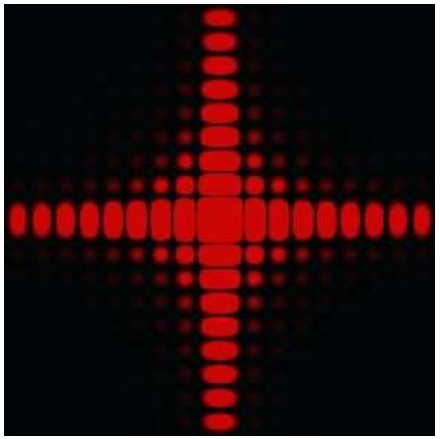
Exposing methods

- Whole-wafer projection lithography
- contact printing
- direct step-on-wafer (multiply wafer exposition)

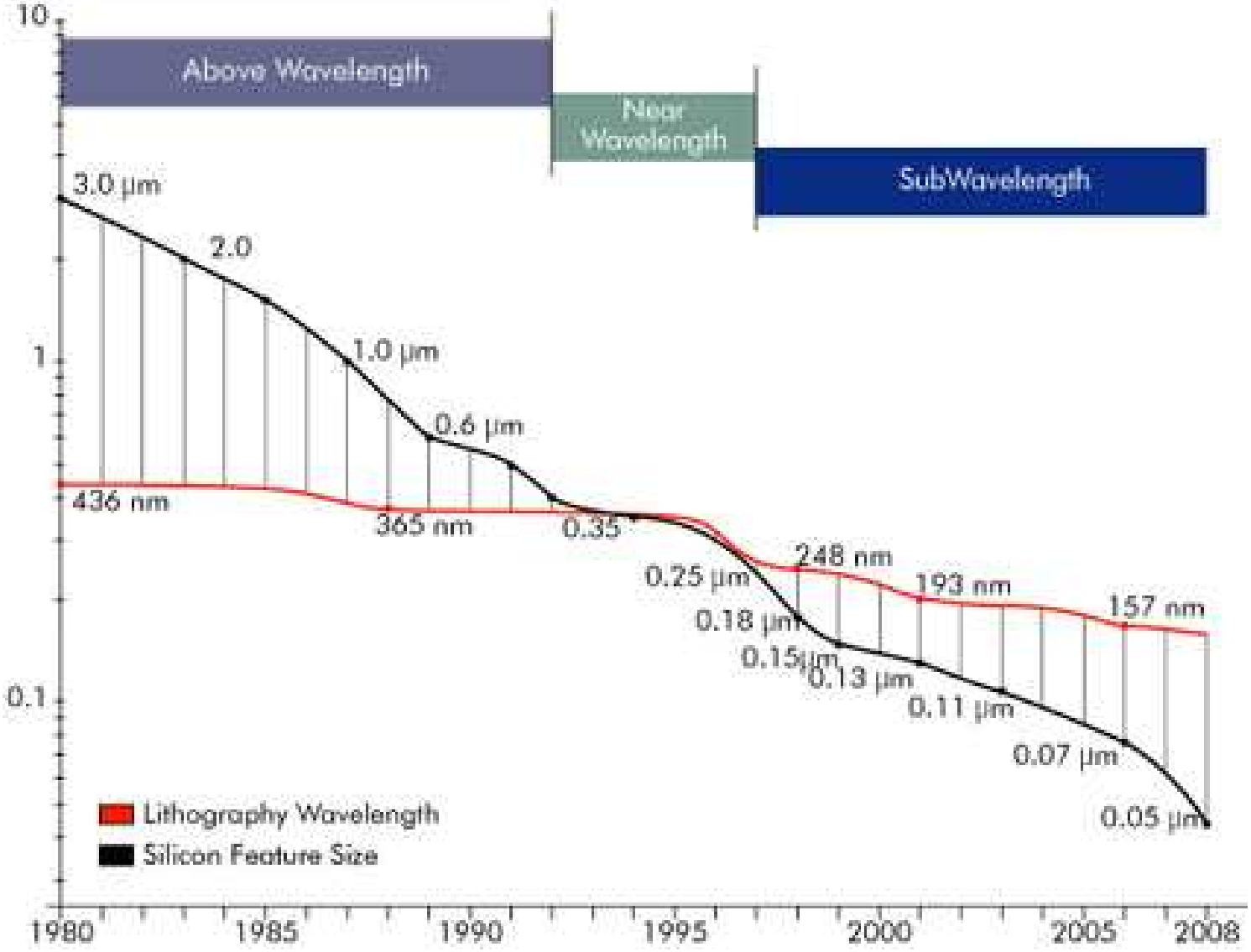
Lithography types

- Optical (mostly UV)
- Roentgen
- Electron
- Ion

The wavelength determine the mask precision (diffraction phenomenon)

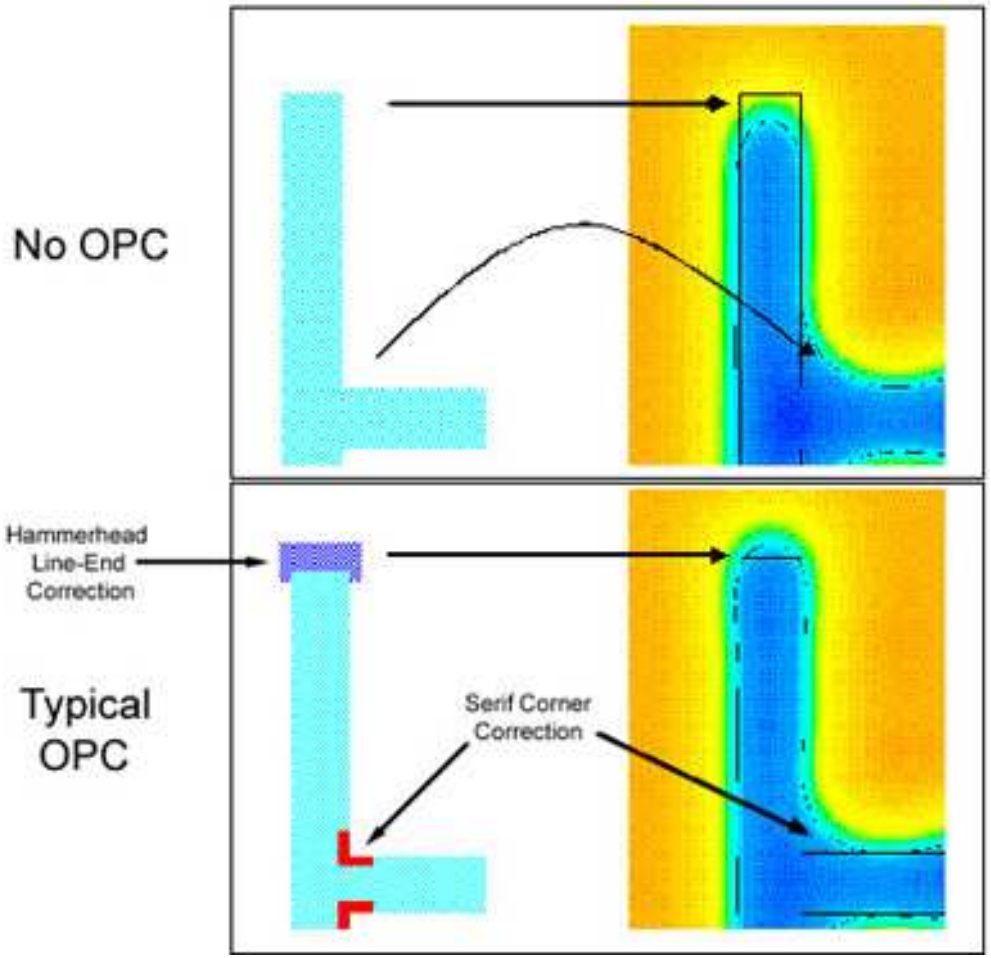


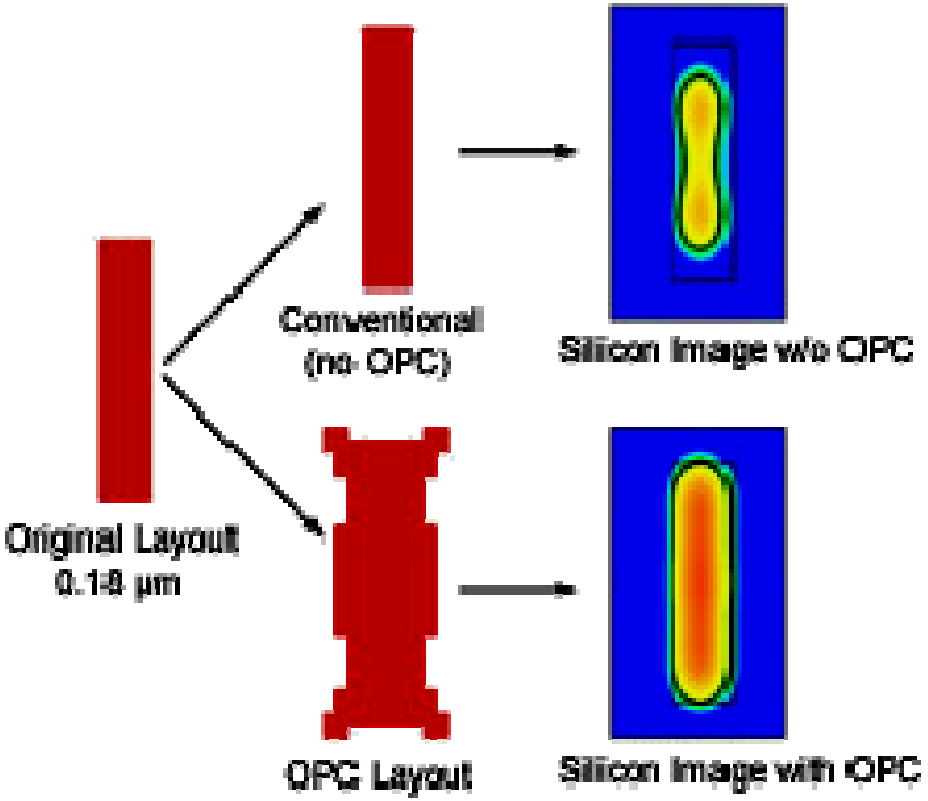
Photolithography and technology vs. wavelength



Source: Numerical Technologies http://www.numeritech.com

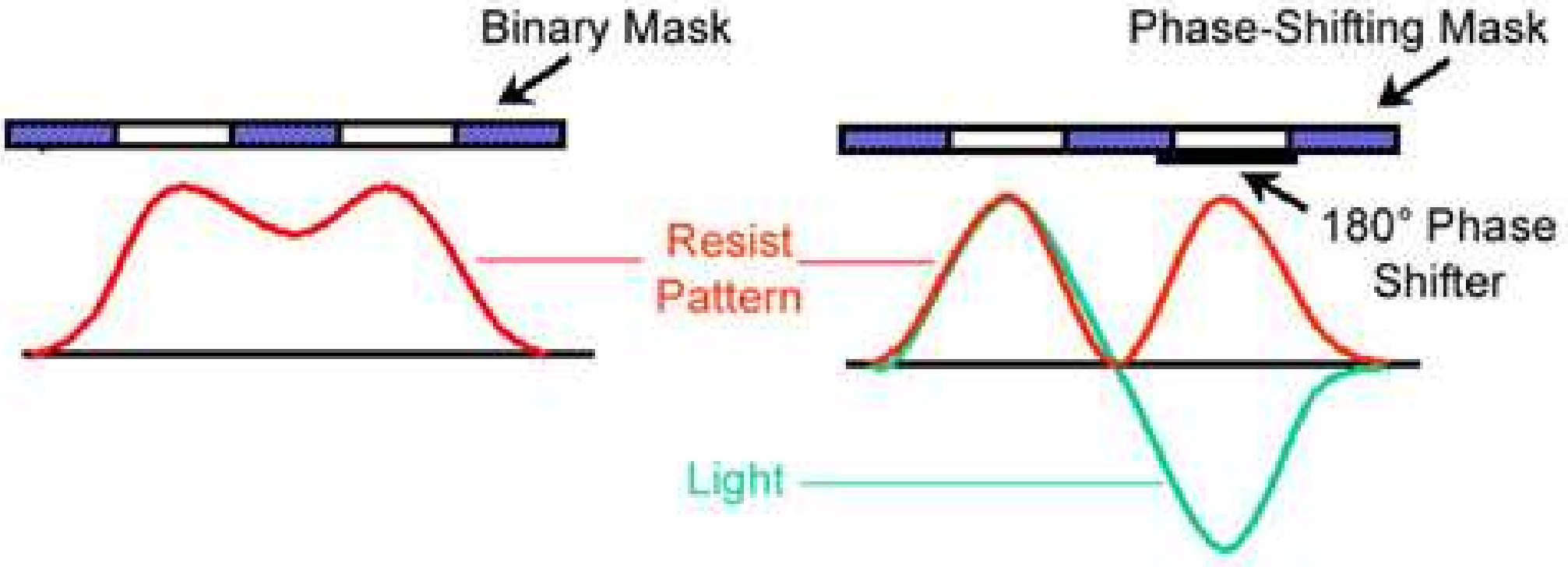
Optical Proximity Correction





Source: Numerical Technologies http://www.numeritech.com

Phase-Shifting Masks



Source: Numerical Technologies http://www.numeritech.com

Etching

Photo-resist patterns printed by lithography must be transferred onto layers that comprise the integrated circuit

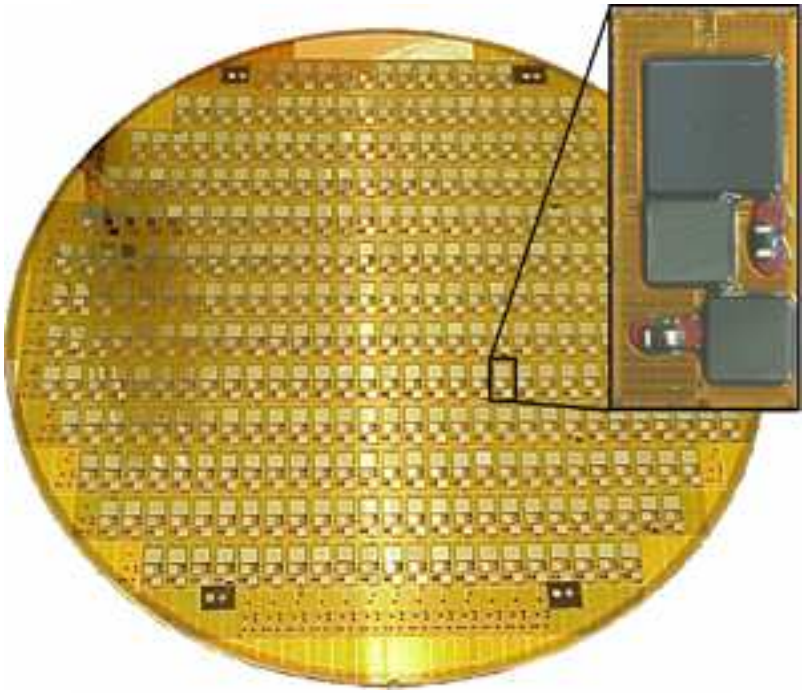
A common process is to selectively etch away the layer material no covered by resist.

The etching process can be used to etch contacts holes in an oxide layer or etch most polysilicon materials away to leave narrow islands for MOSFET gates

Etching

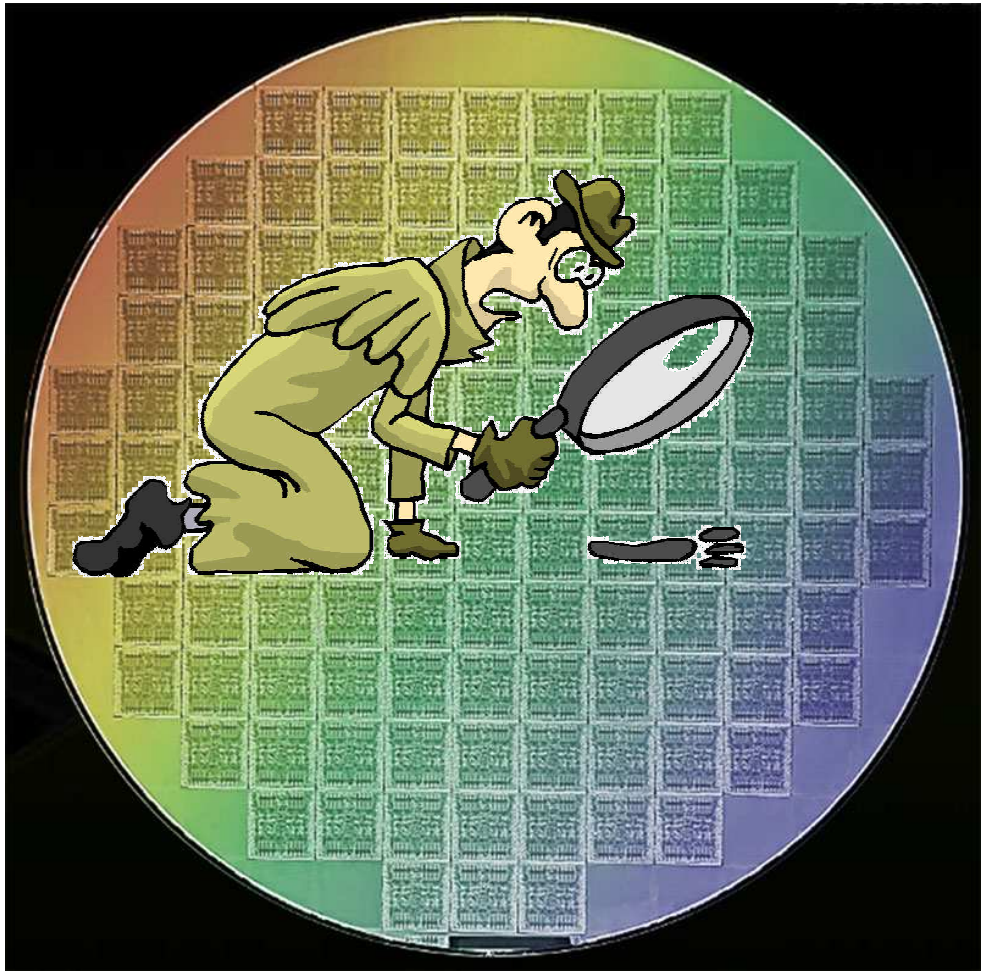
- Wet and dry
- Dry etching
  - physical (i.e. sputtering: high accelerated ions bombard the etched material)
  - chemical (etching compound)
  - mixed
  - photochemical
- Dry etching method advantages:
  - Selectivity - high resolution
  - High anisotropy

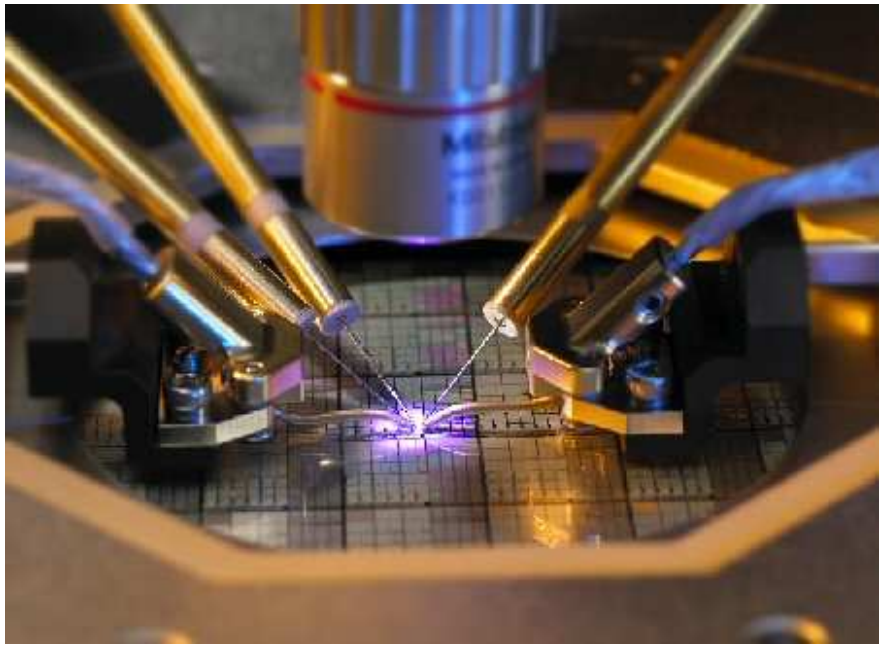
Lithography, deposition, implantation, etching



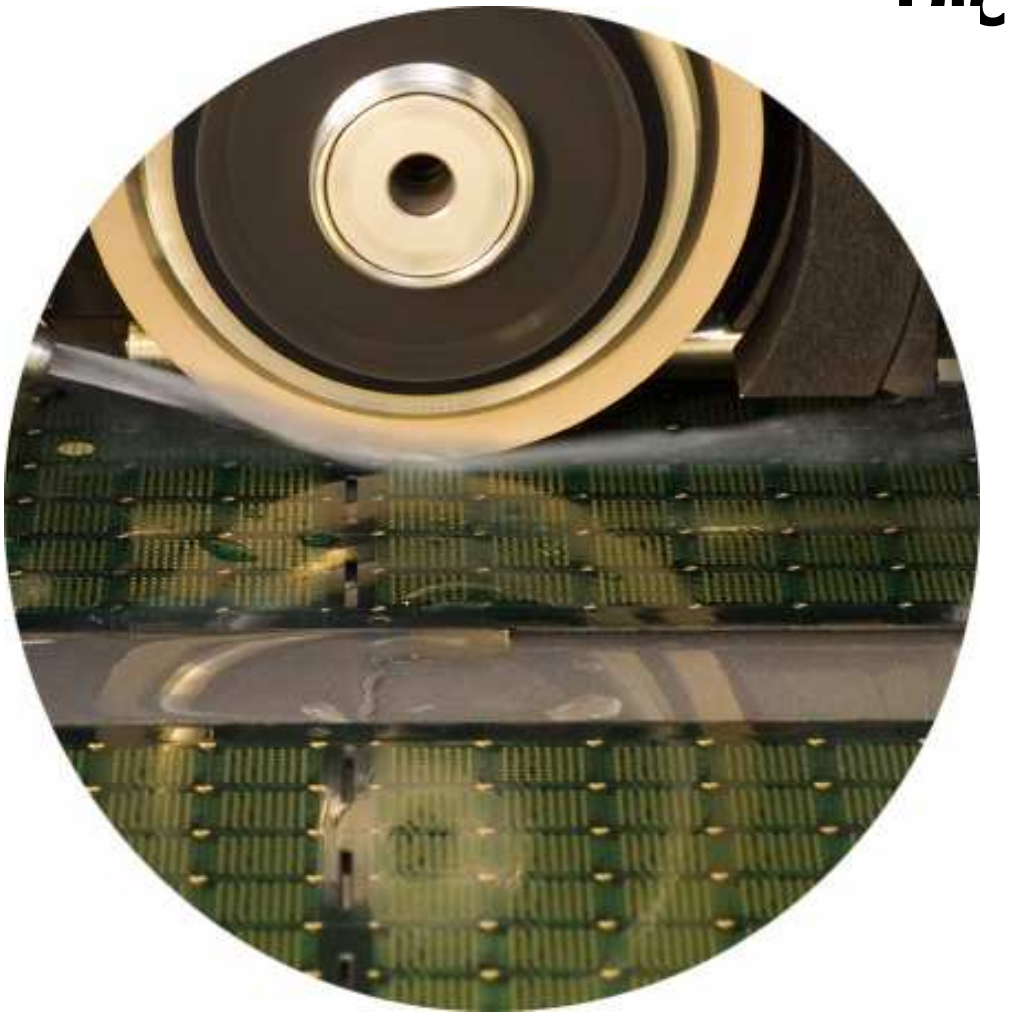
And finally the wafer with many devices on board

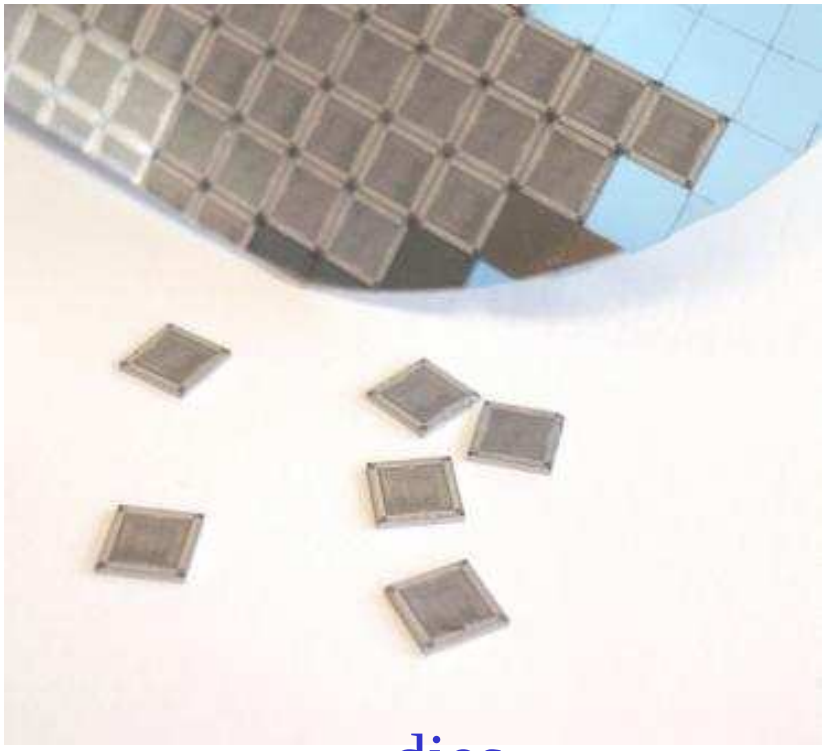
On-wafer testing





Dicing

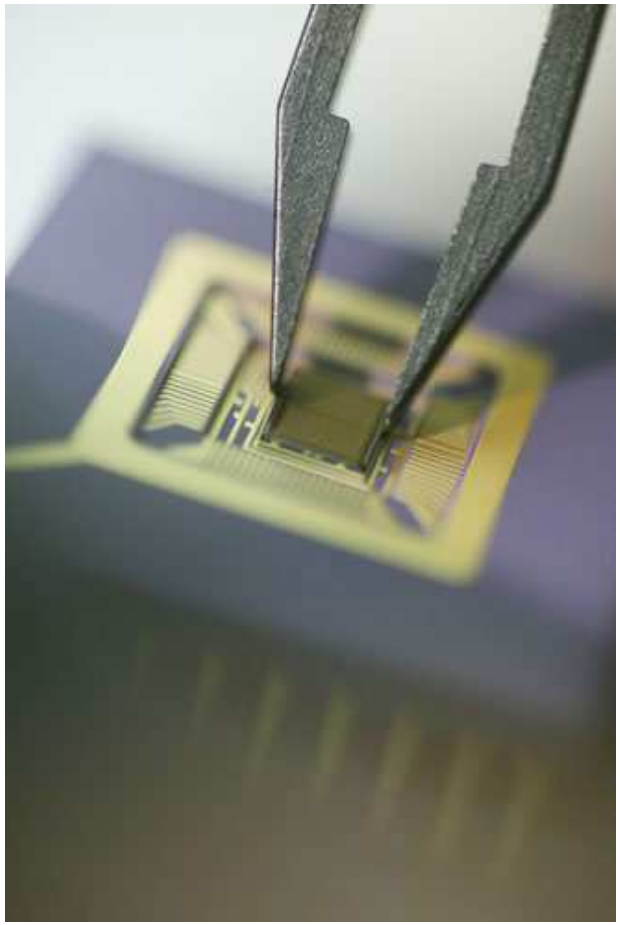


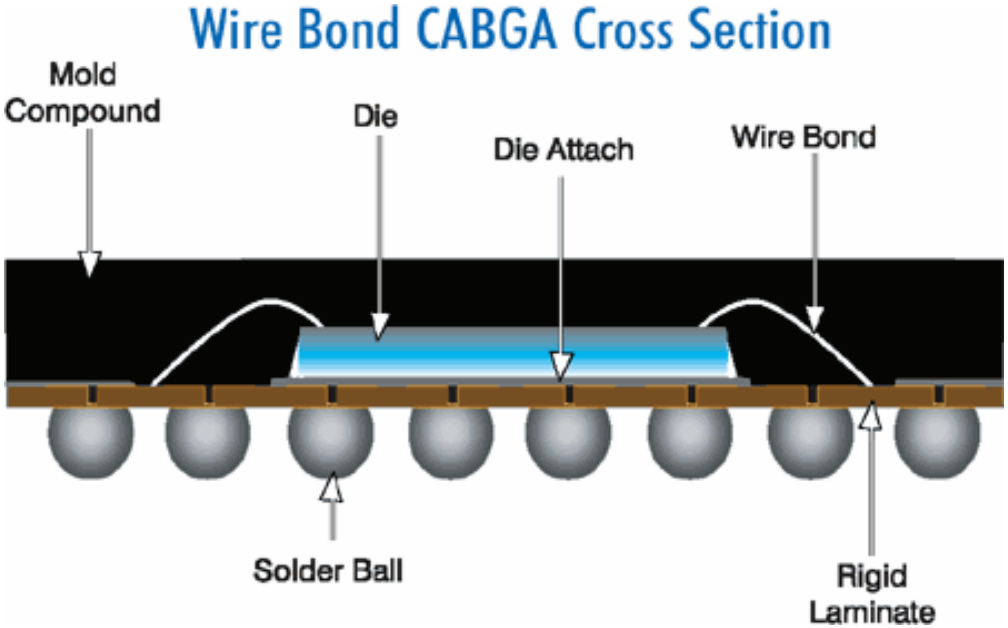


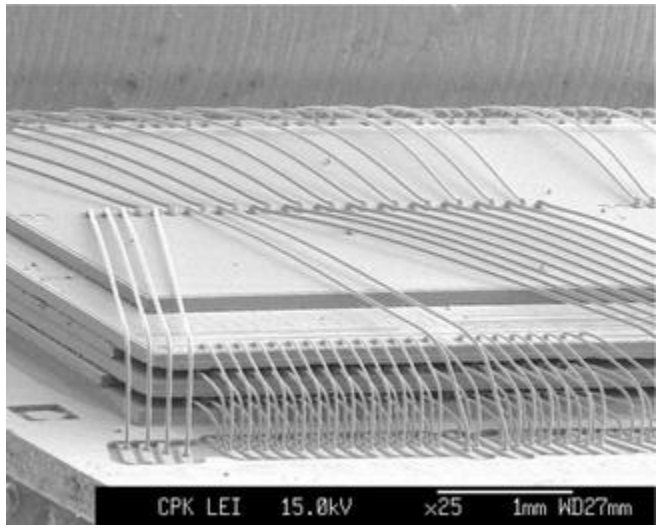
dies

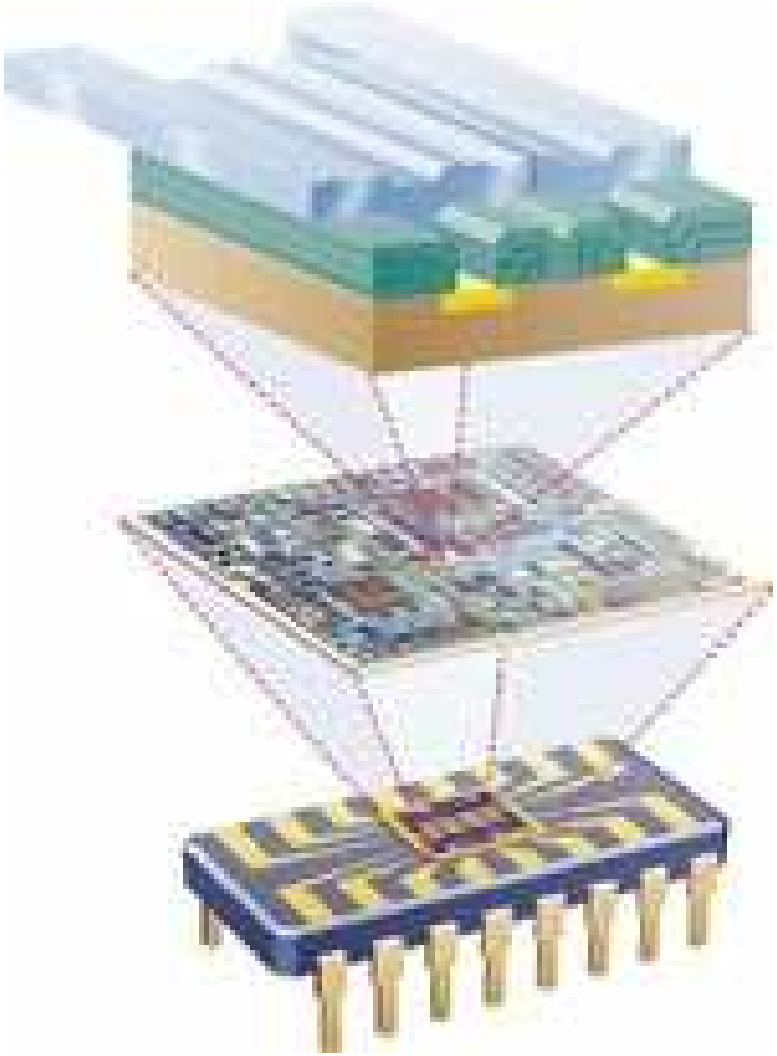
Dice packaging

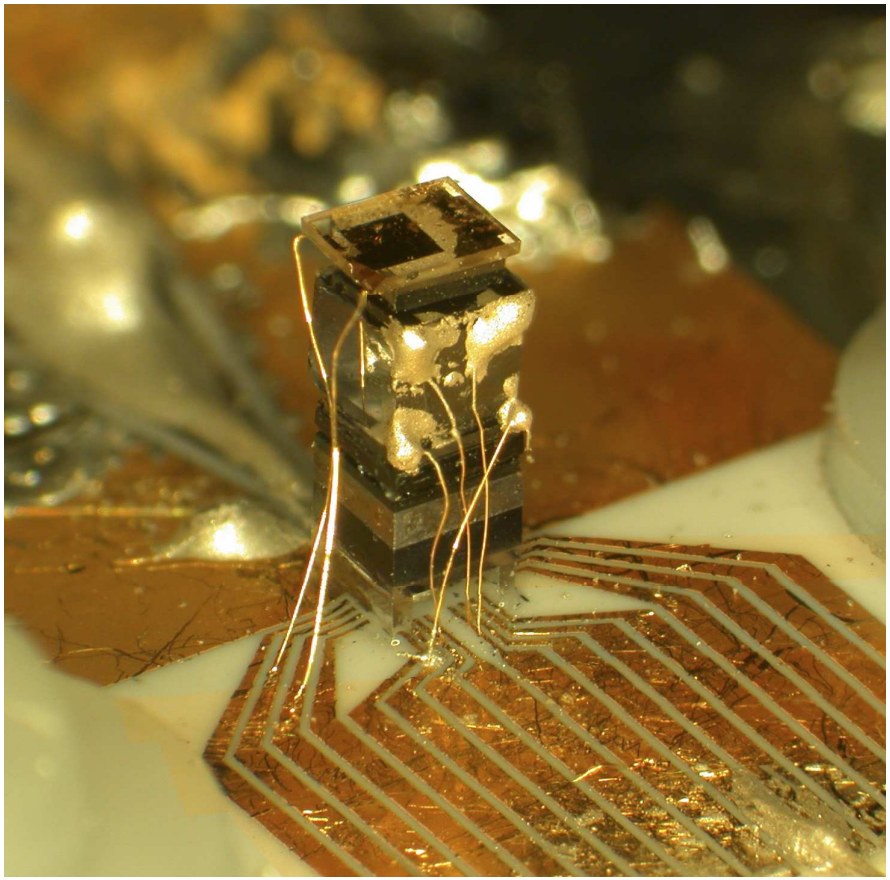
Packaging



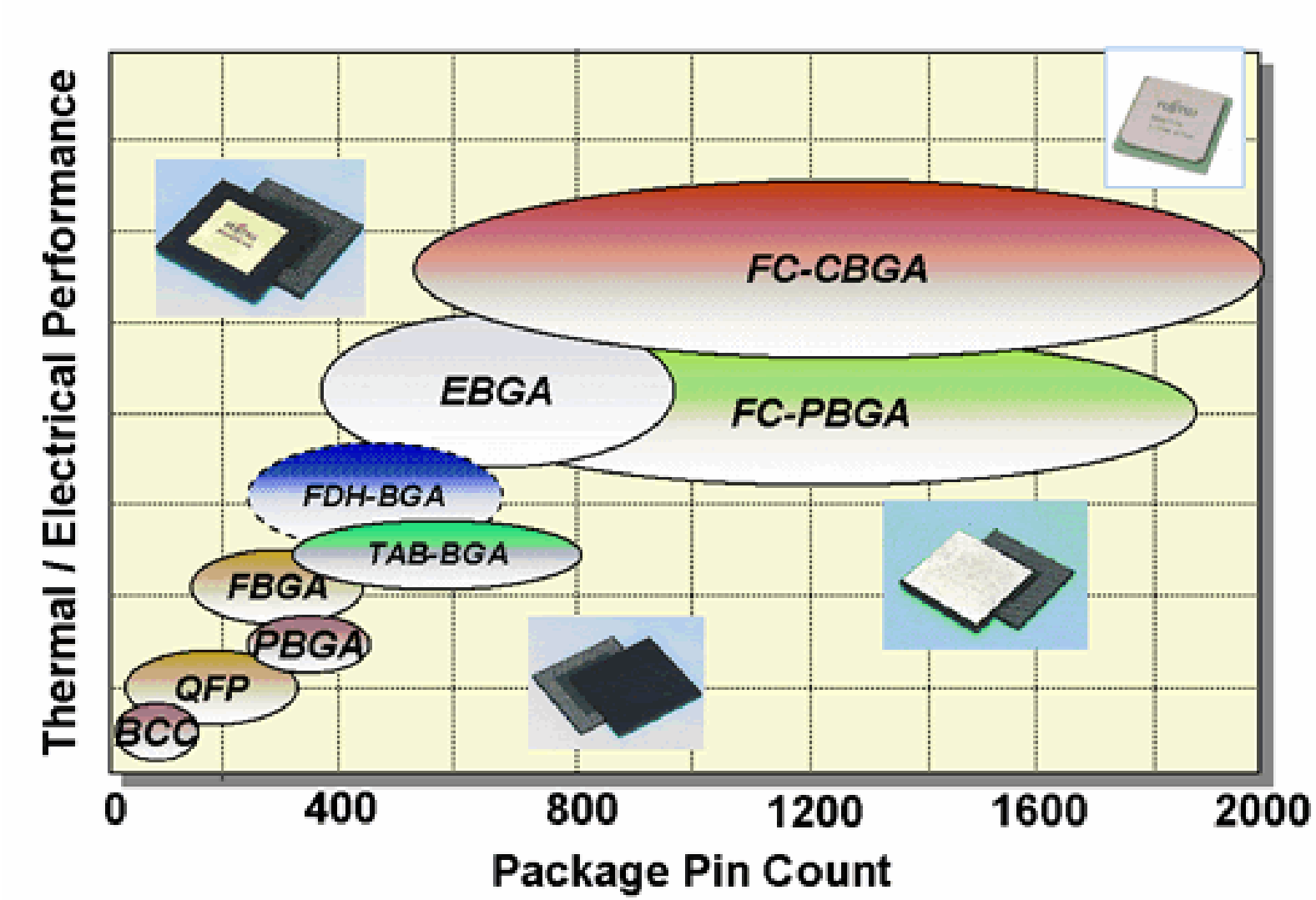

Wire Bond CABGA Cross Section
Mold Compound
Die
Die Attach
Wire Bond
Solder Ball
Rigid Laminate


CPK LEI 15.0kV ×25 1mm WD27mm





Pins number is growing



Next lecture

More complex devices : MUX, flip-flops

Thank you for your attention