Electronic Technology Design and Workshop

Presented and updated by

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DMCS room 2

2007

Electronic Technology Design and Workshop

Lecture 4

Microelectronics - elementary gates

ETDW course road map

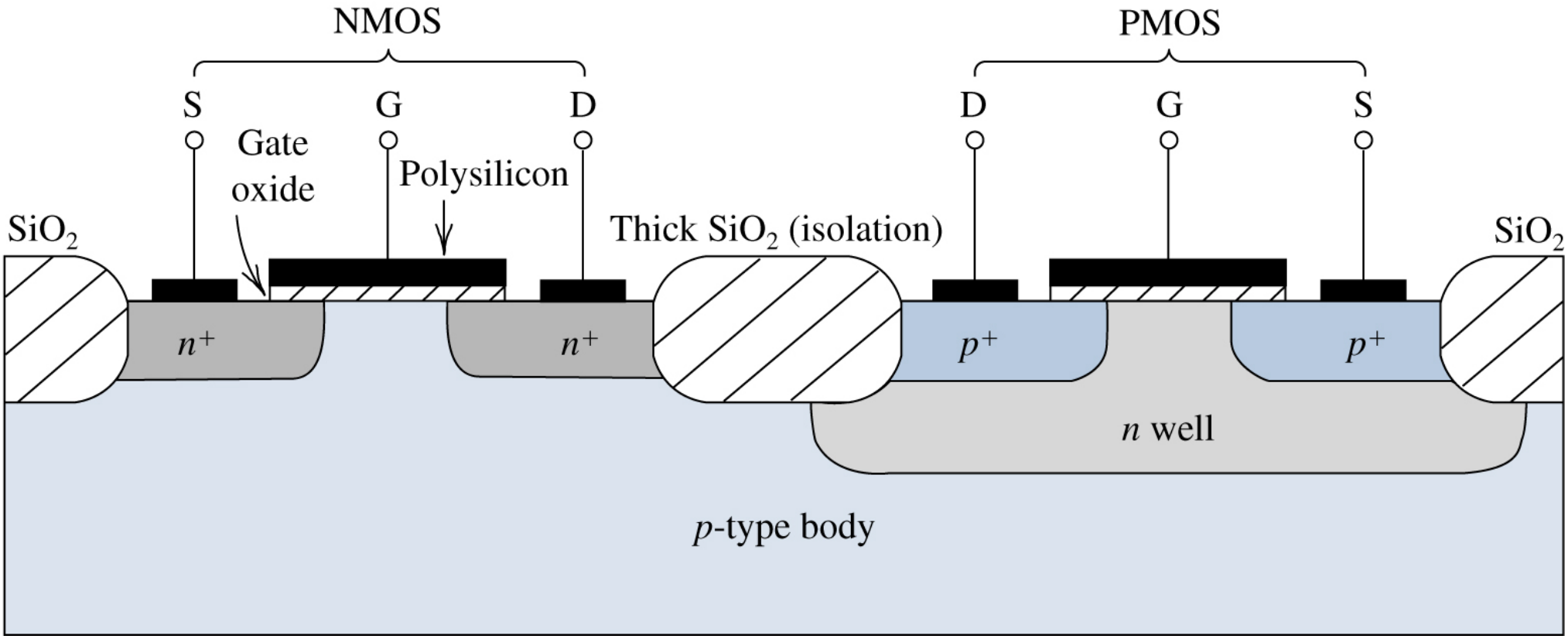
- ✓ Schematic edition, libraries of elements
- ✓ Circuit simulation & netlist generation
- ✓ **Microelectronics - full custom design and simulation**
- ✓ Microelectronics - simple layout synthesis
- ✓ Hardware description languages - behavioural description
- ✓ Logic & sequential synthesis - programmable logic devices
- ✓ PCB design – auto-routing

- Project - bringing the pieces together

Outline

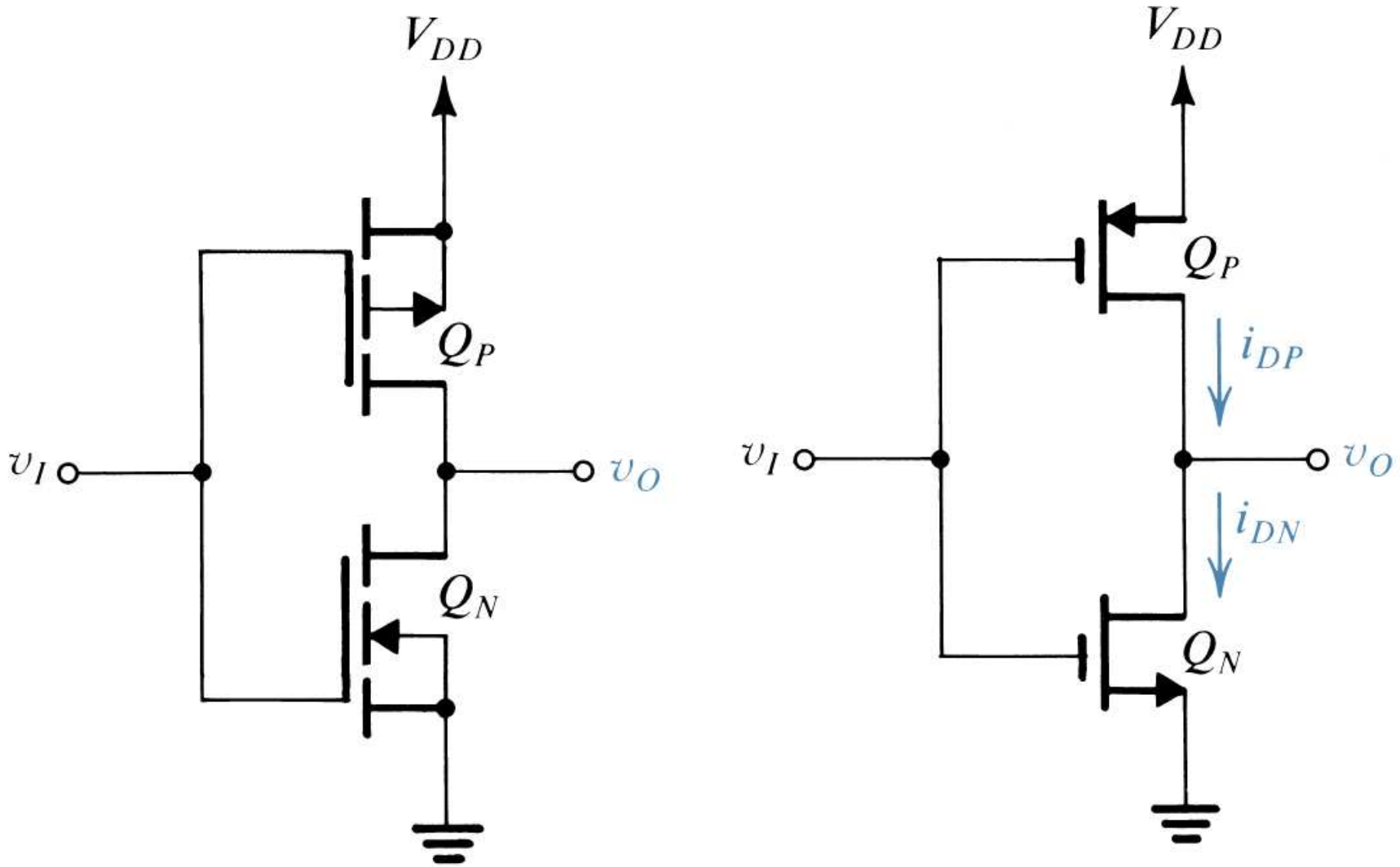
- Inverter (NOT)
- NAND
- NOR
- Transmission gate
- XOR
- Ring oscillator

CMOS inverter cross-section

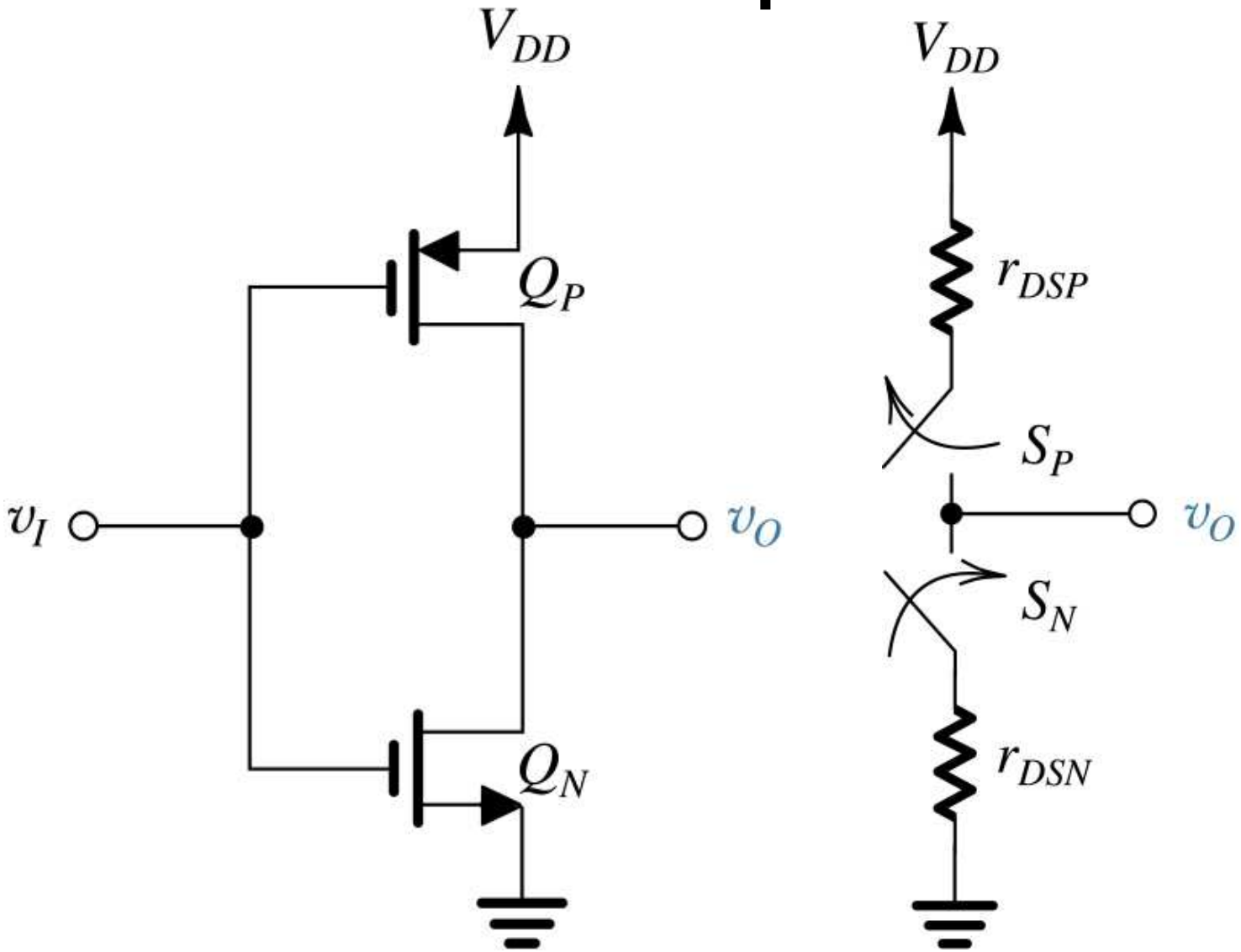


Note that the PMOS transistor is formed in a separate *n*-type region, known as an ***n* well**. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a ***p* well**.

CMOS inverter scheme



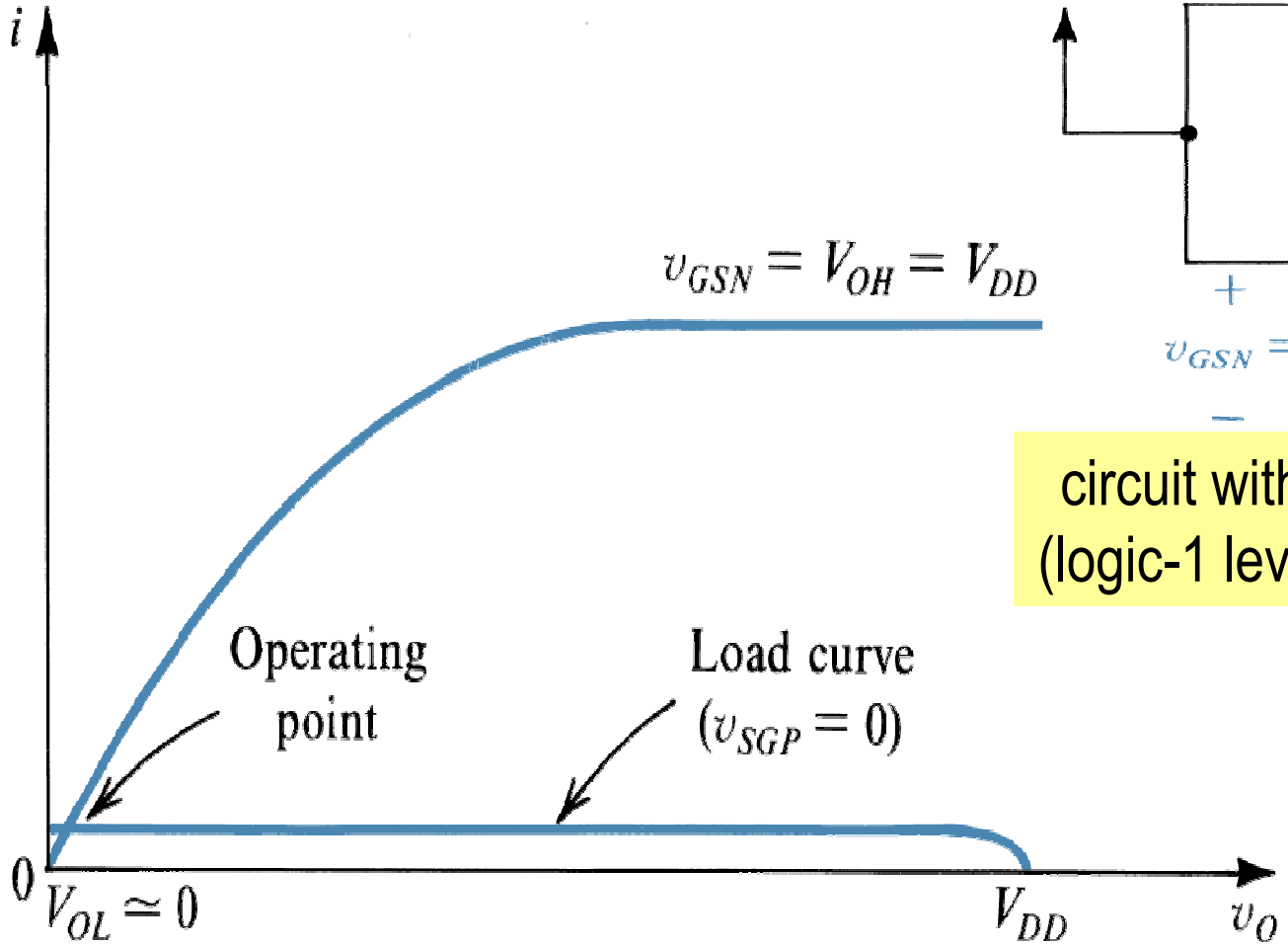
CMOS inverter and pair of switches

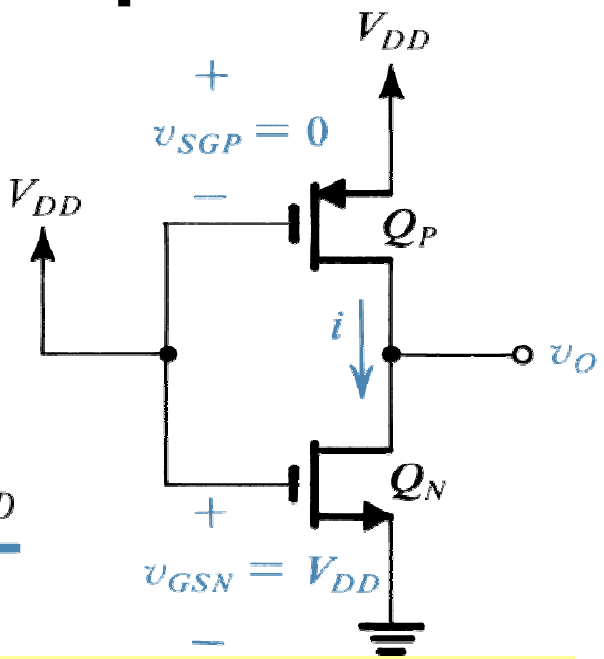


Note: switches must operate in a complementary fashion.

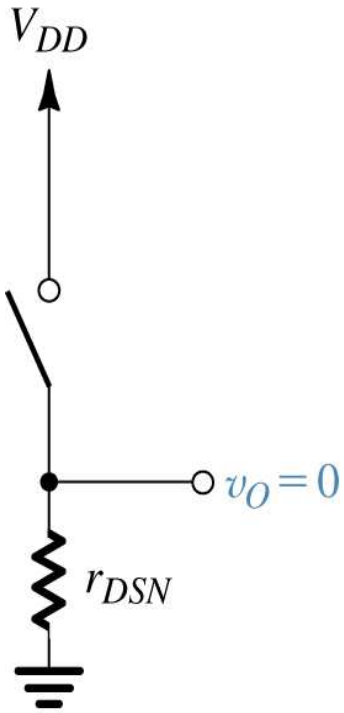
CMOS inverter operation

v_1 is high





circuit with v1 = VDD (logic-1 level, or VOH);

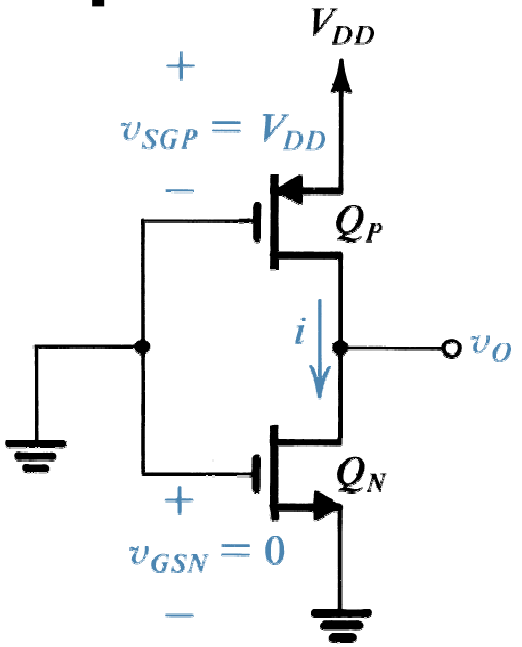


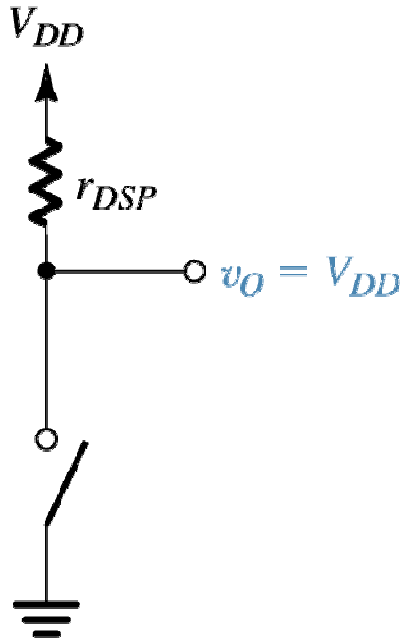
equivalent circuit.

graphical construction to determine the operating point

CMOS inverter operation

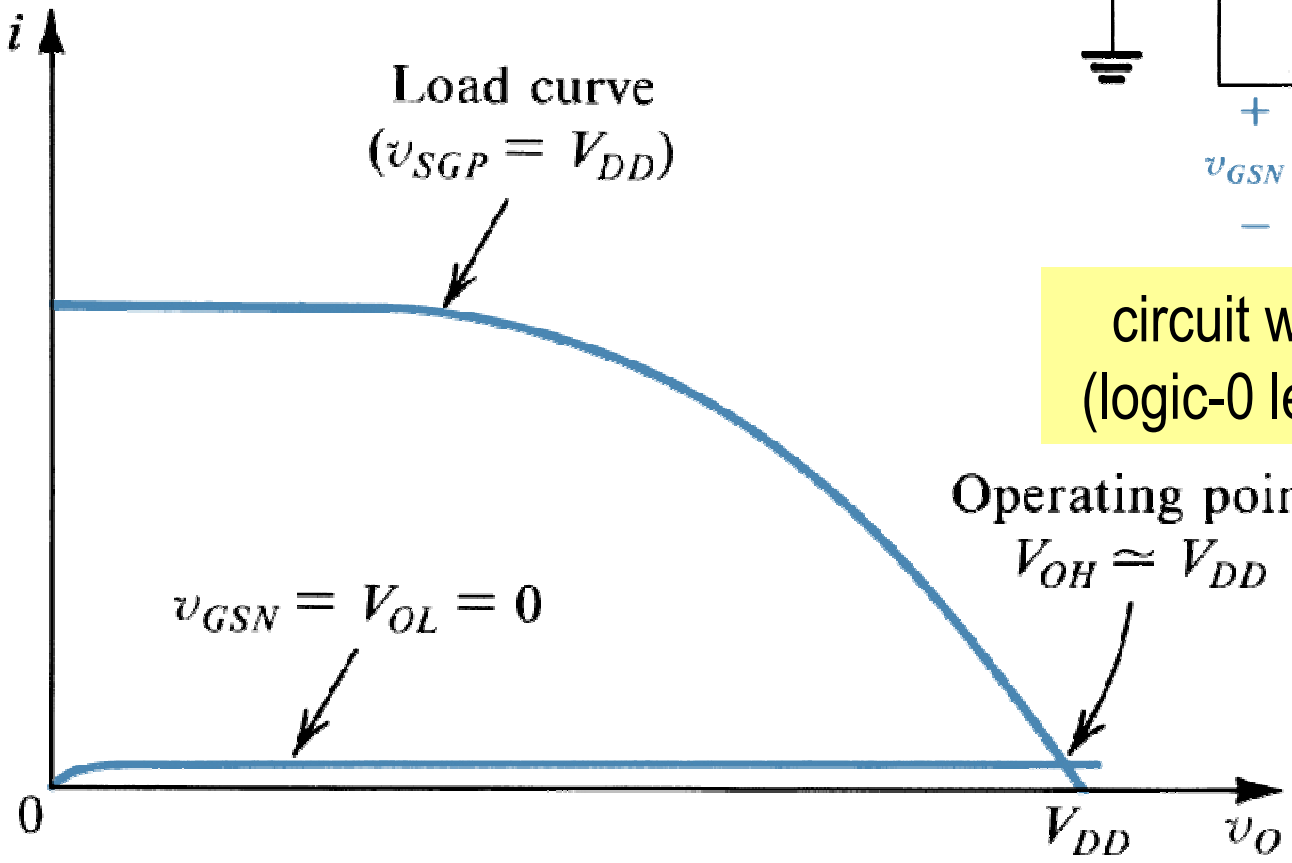
v_1 is low





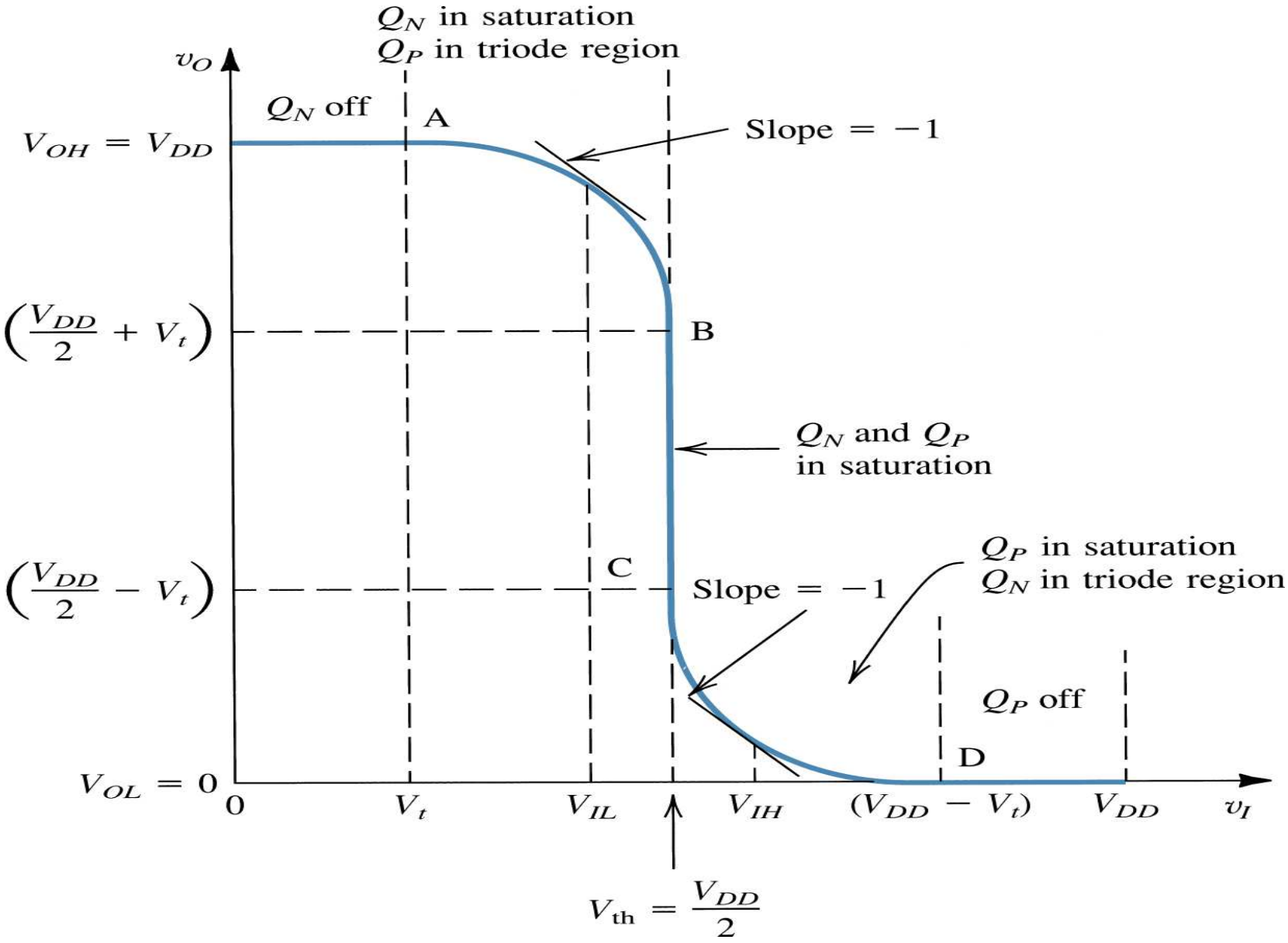
circuit with v1 = 0V (logic-0 level, or V_{OL});

equivalent circuit.

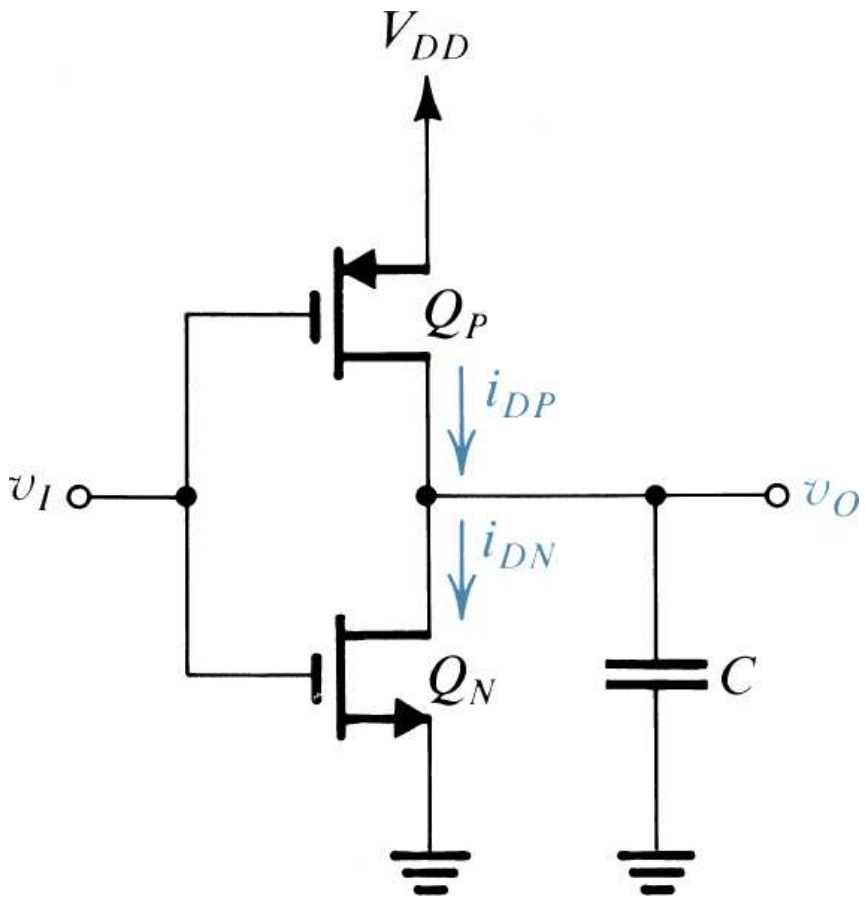


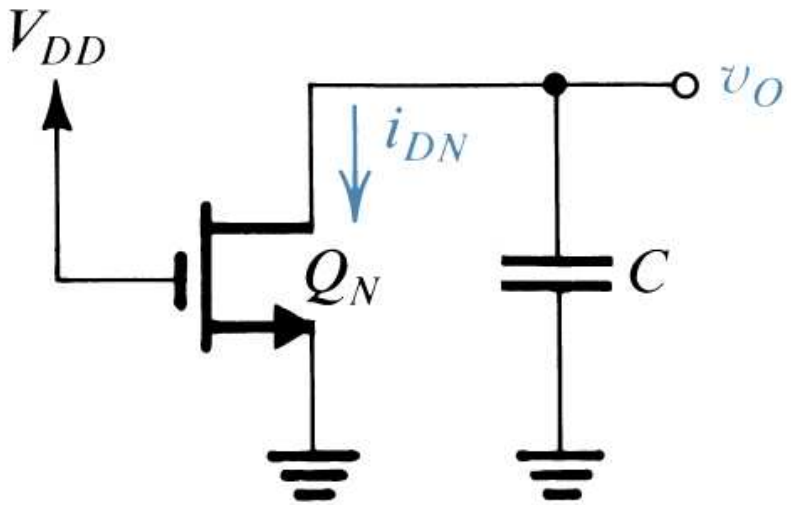
graphical construction to determine the operating point

Voltage transfer characteristic of the CMOS inverter



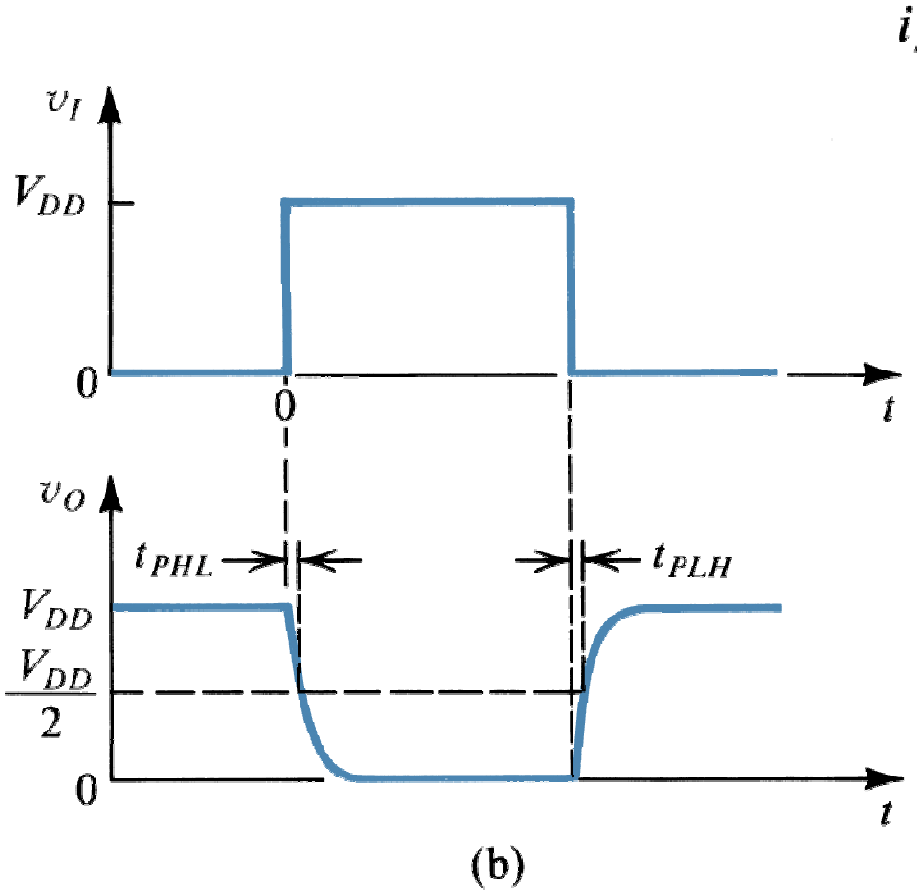
Dynamic operation of a capacitive loaded CMOS inverter



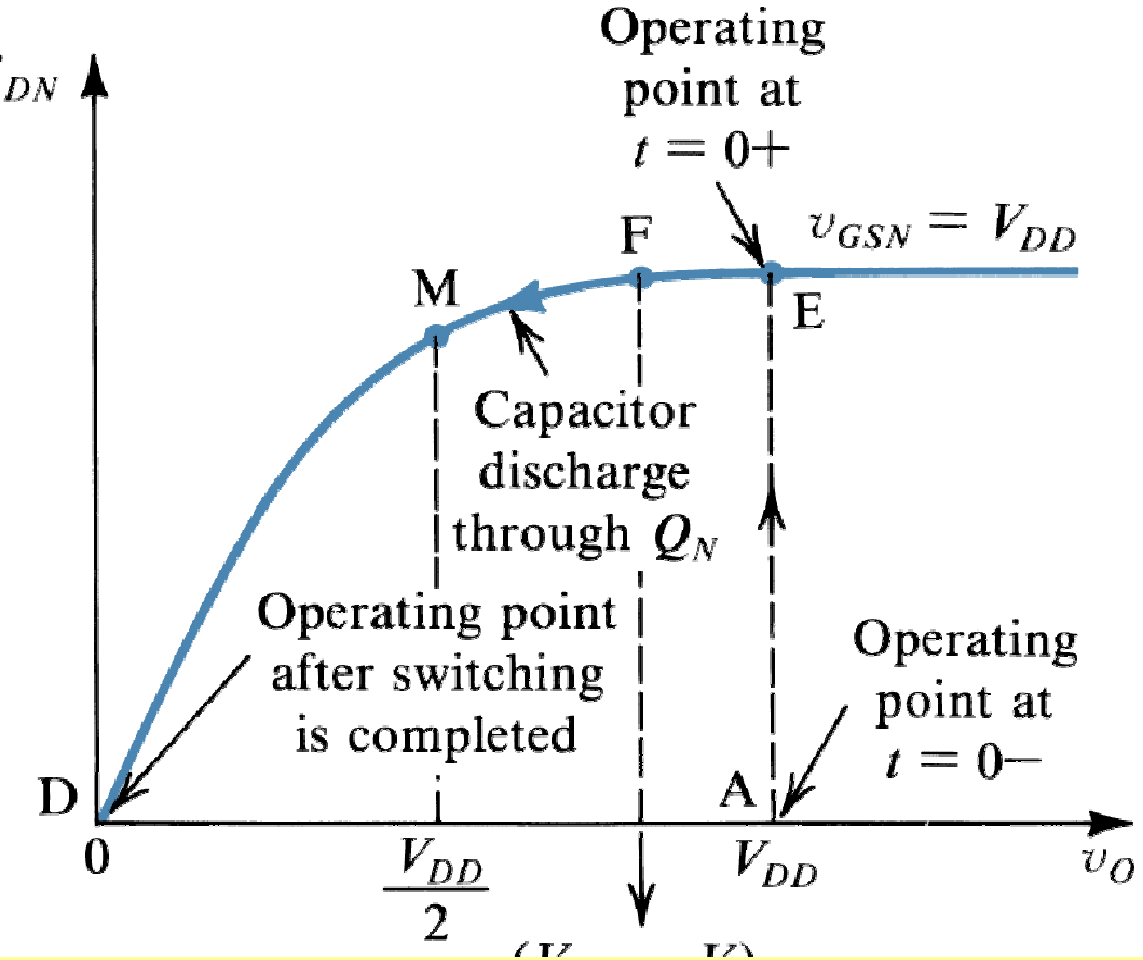


equivalent circuit during the capacitor discharge.

Dynamic operation of a capacitive loaded CMOS inverter

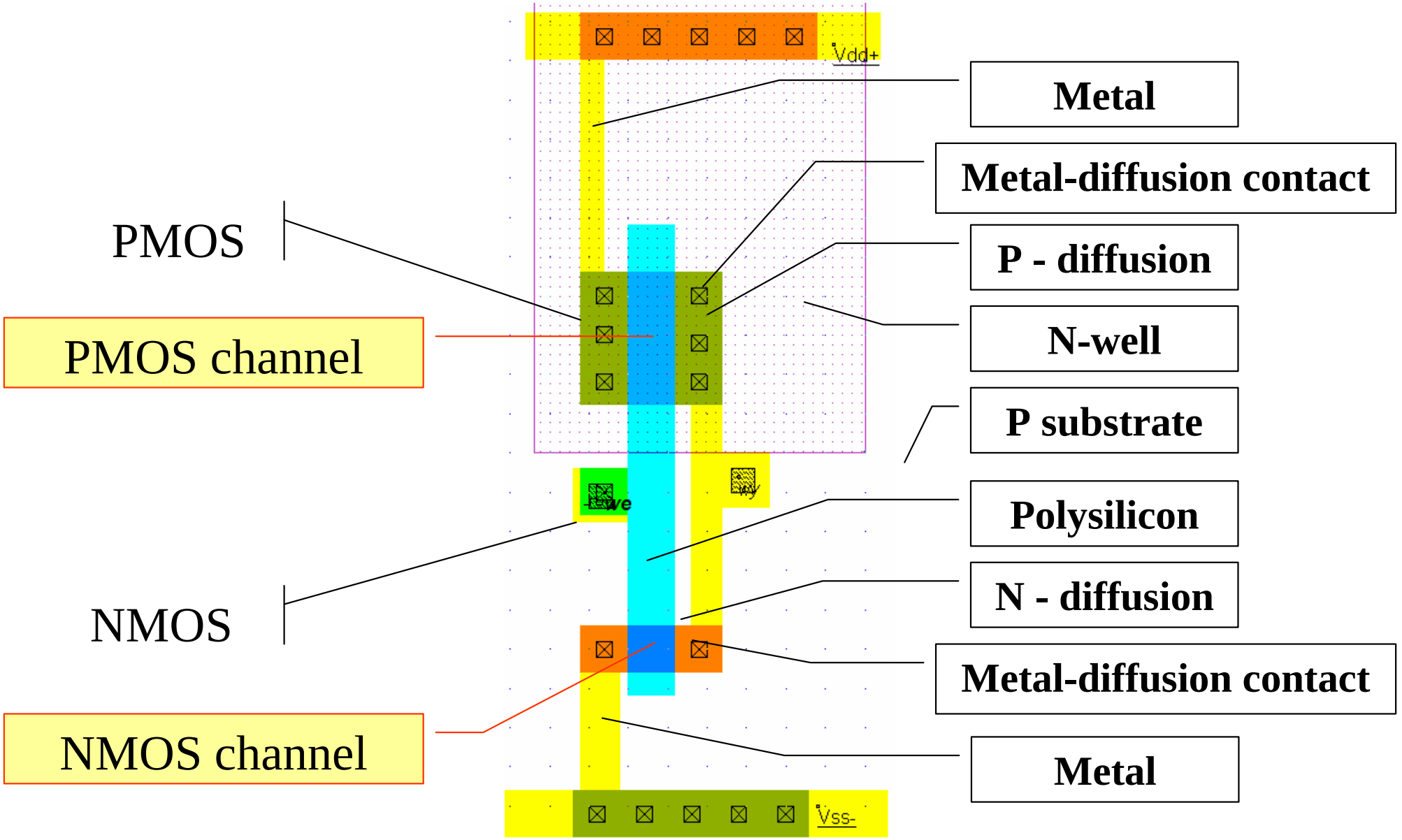


input and output waveforms

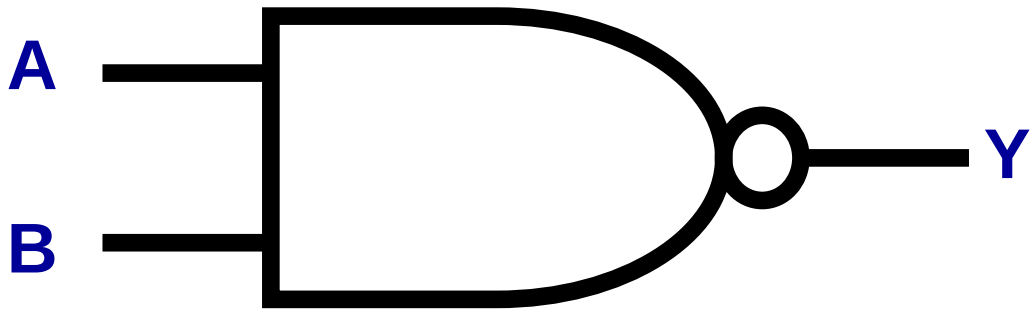


trajectory of the operating point as the input goes high and C discharges through the Q_N

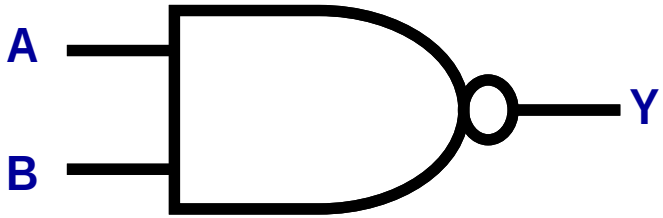
Inverter layout



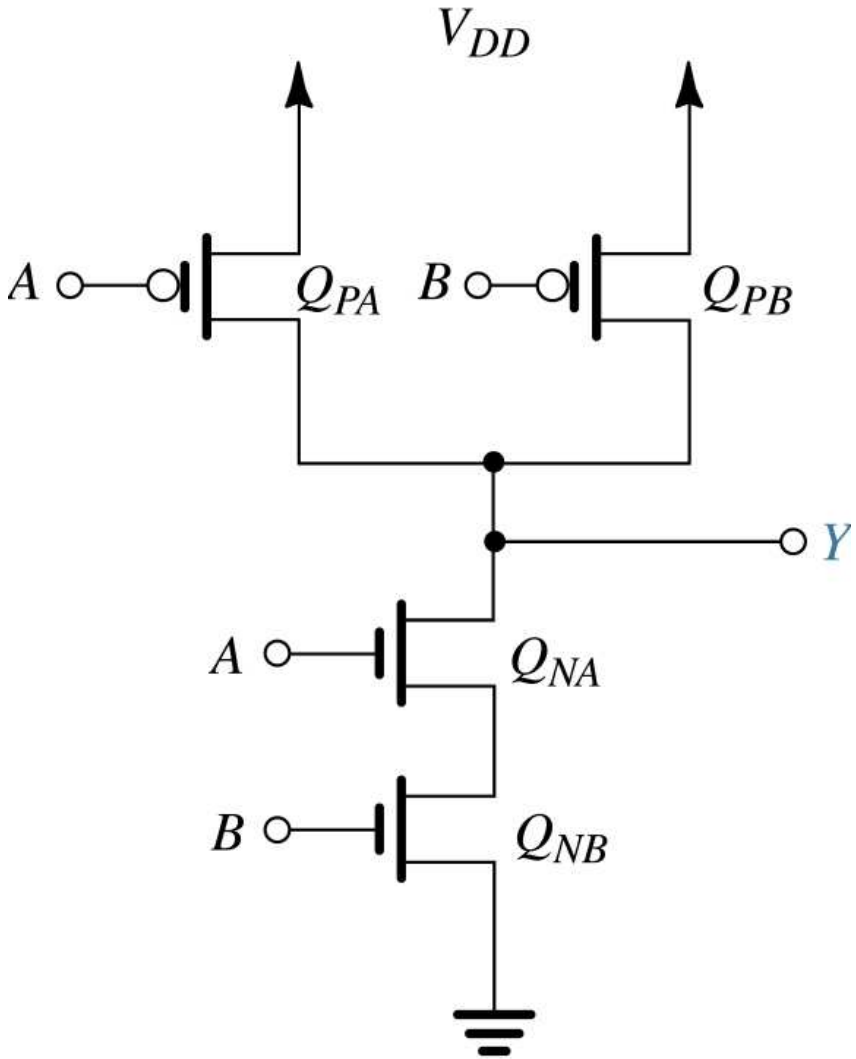
NAND



CMOS NAND gate

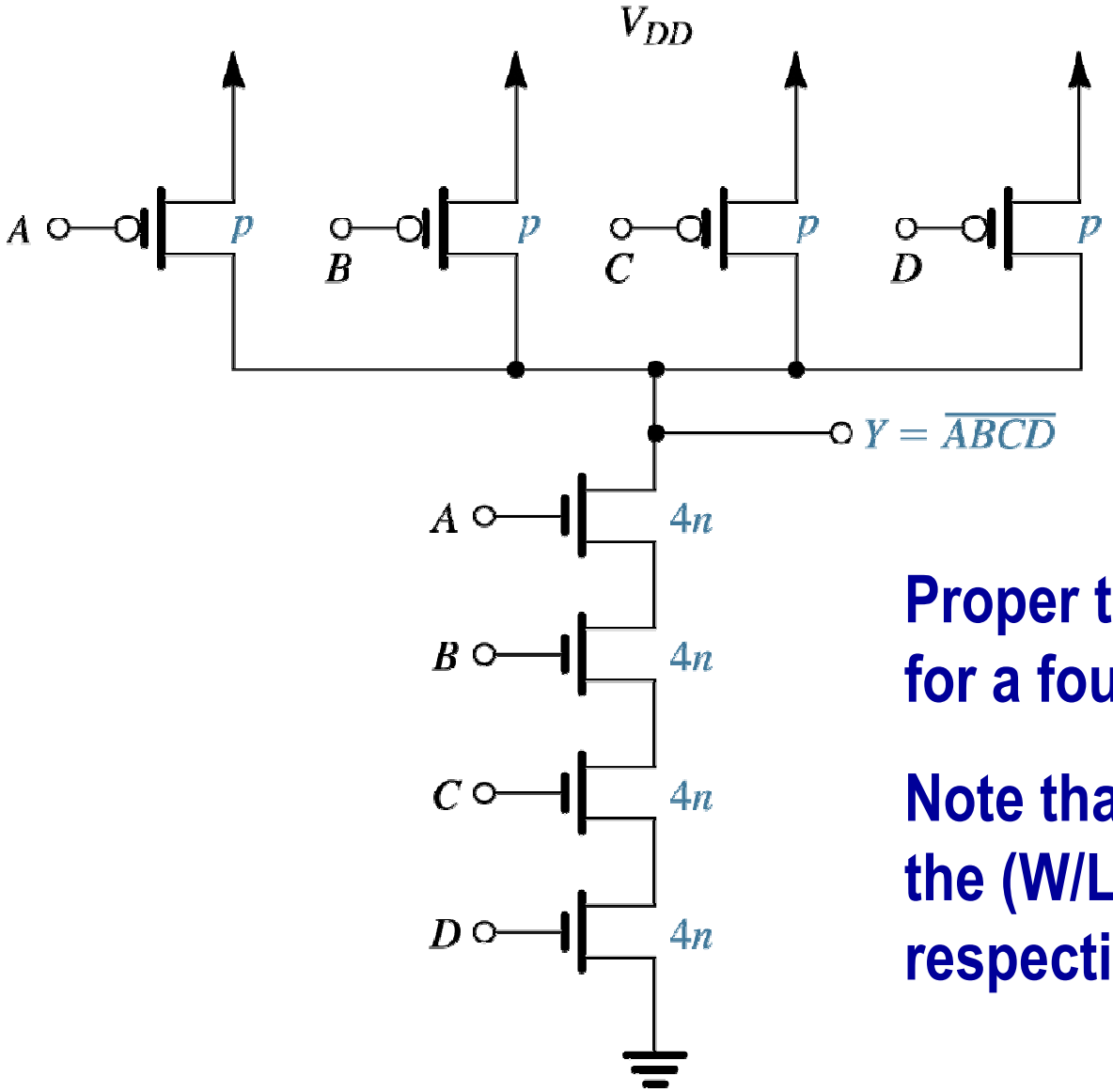


A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



$$Y = \overline{AB}$$

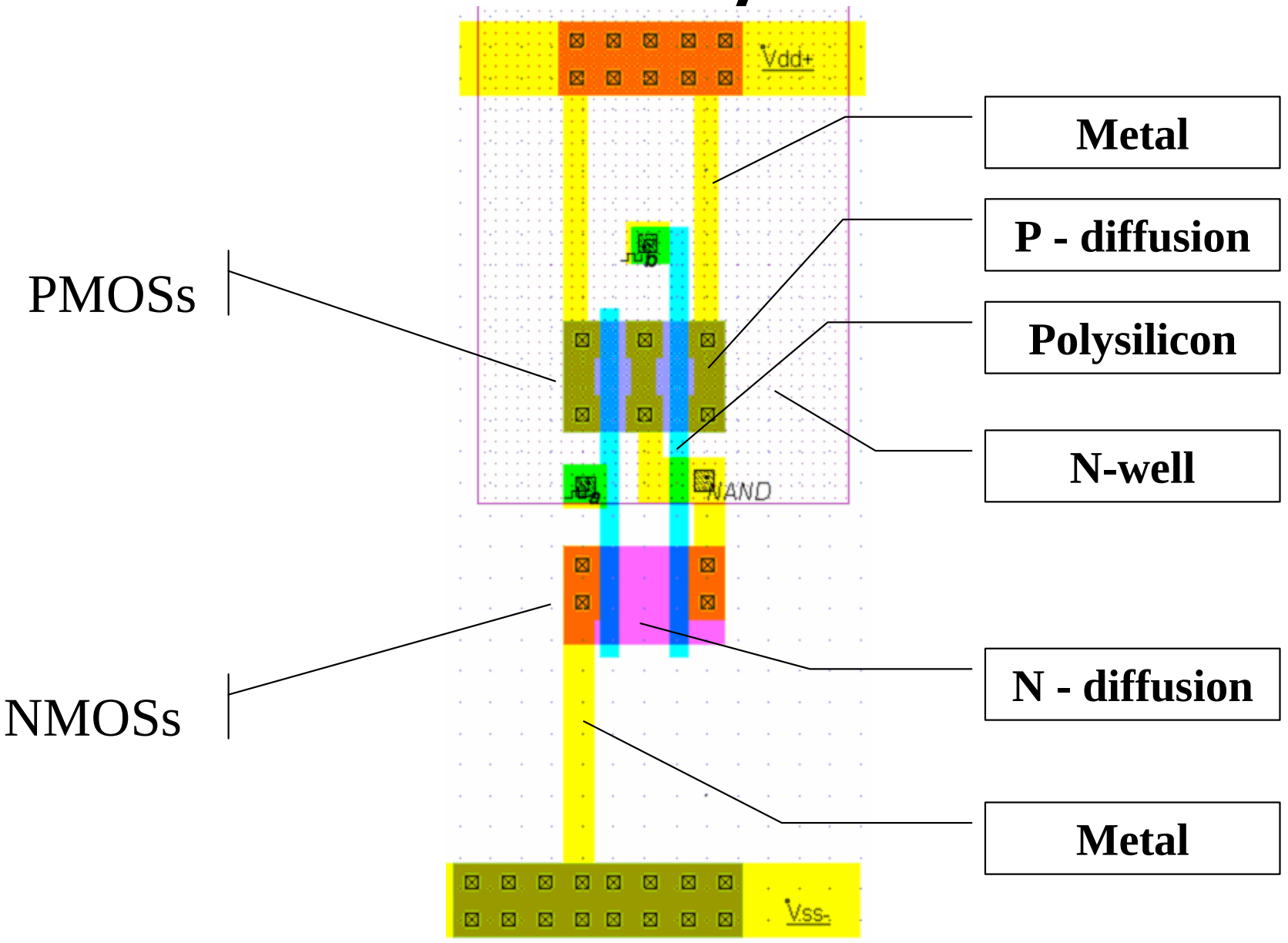
Gate size adjustment for NAND



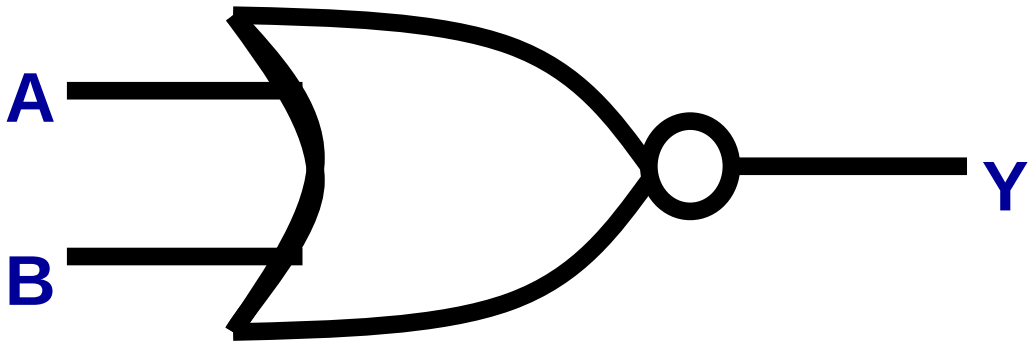
Proper transistor sizing for a four-input NAND gate.

Note that n and p denote the (W/L) rations of Q_N and Q_P, respectively, of the basic inverter.

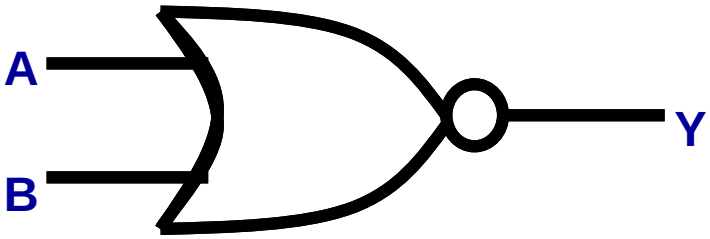
NAND layout


Vdd+
NAND
Vss-
PMOSs
NMOSs
Metal
P - diffusion
Polysilicon
N-well
N - diffusion
Metal

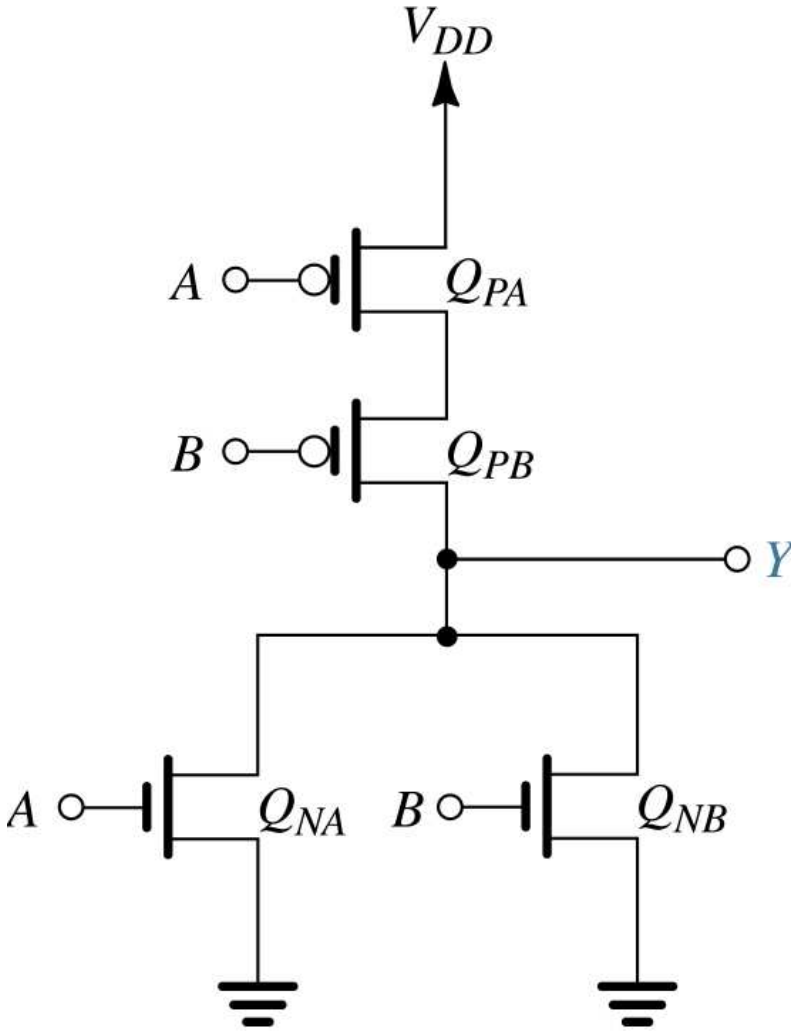
NOR



CMOS NOR gate

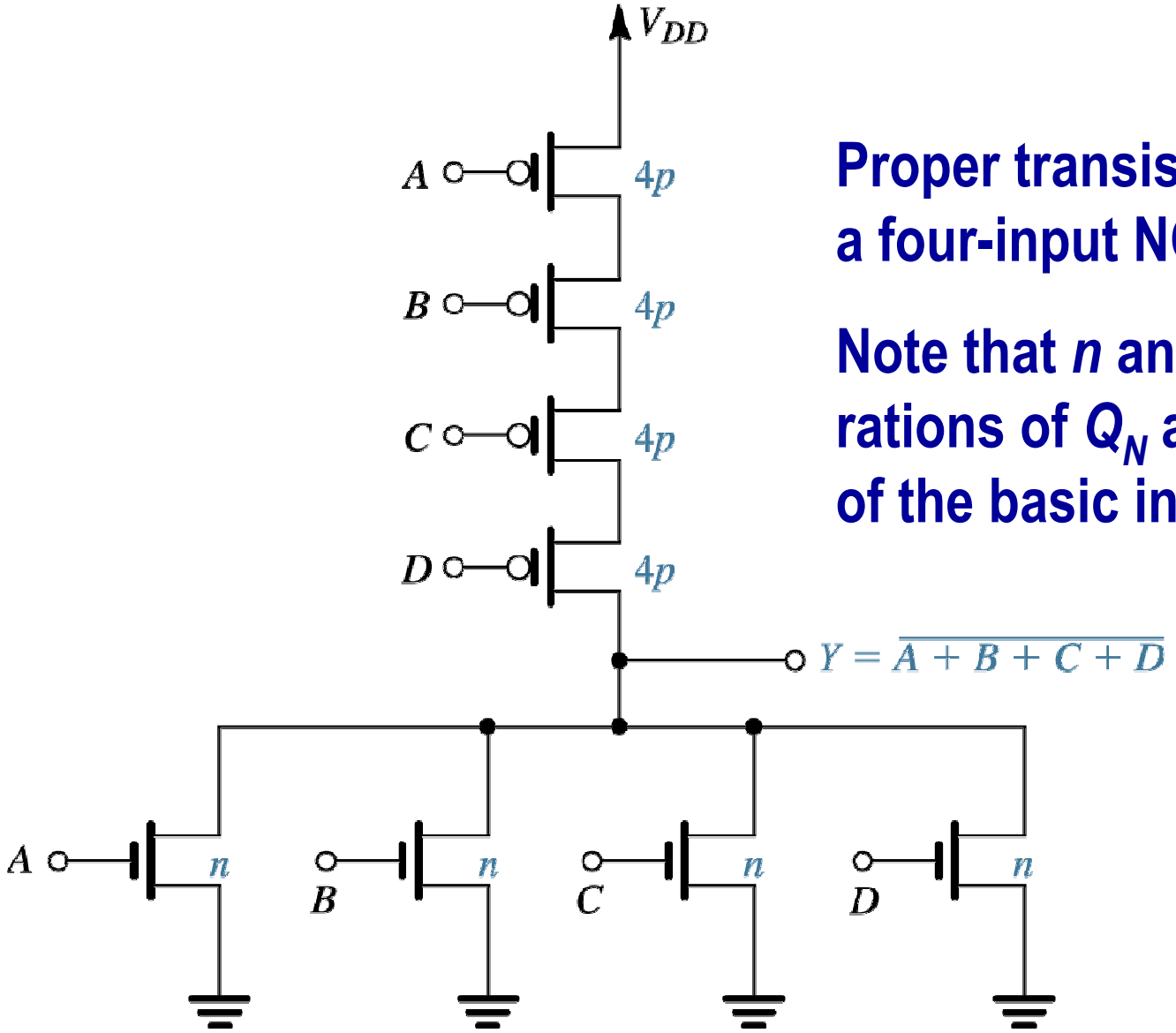


A	B	A nor B
0	0	1
0	1	0
1	0	0
1	1	0



$$Y = \overline{A + B}$$

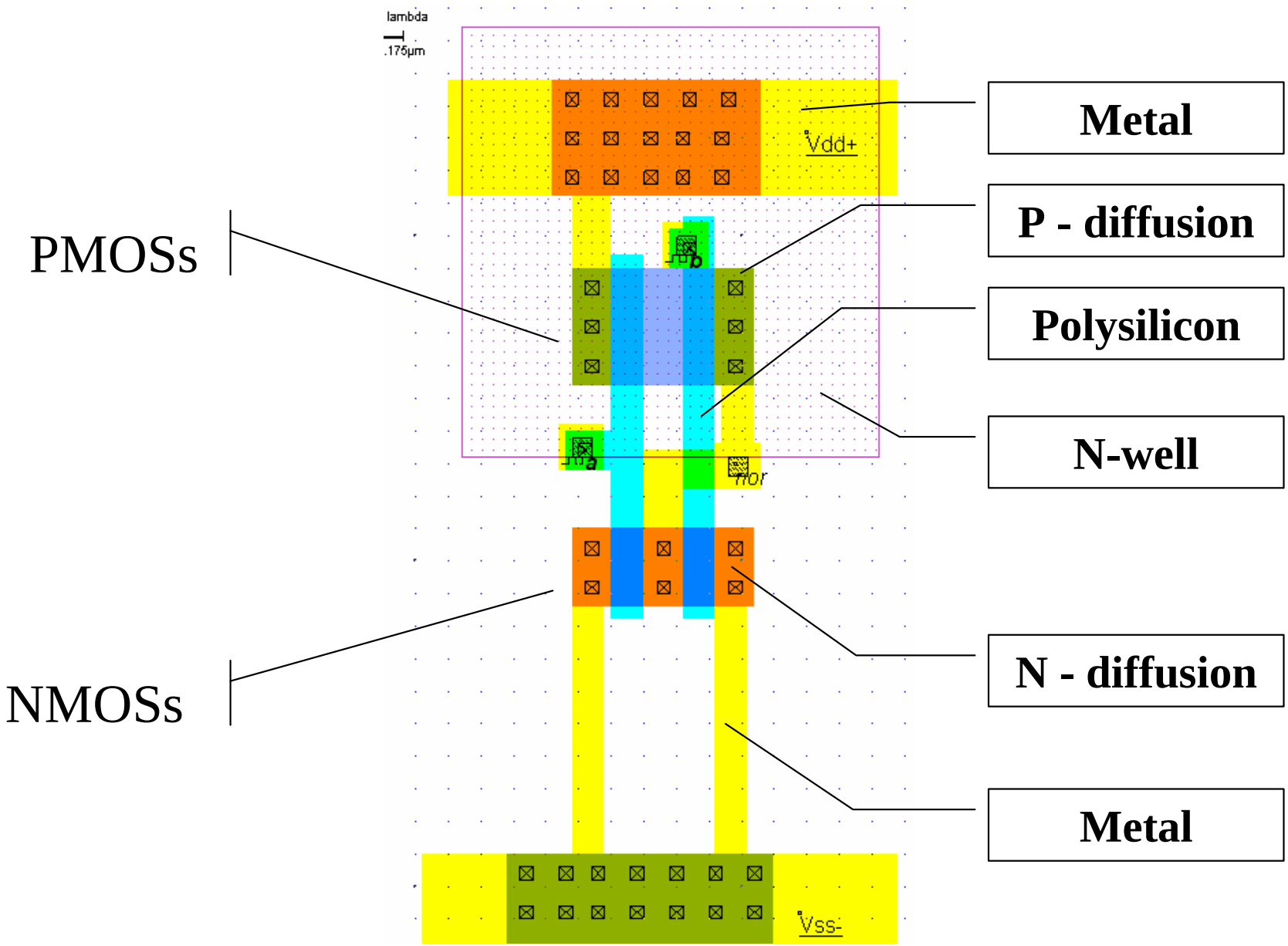
Gate size adjustment for NOR



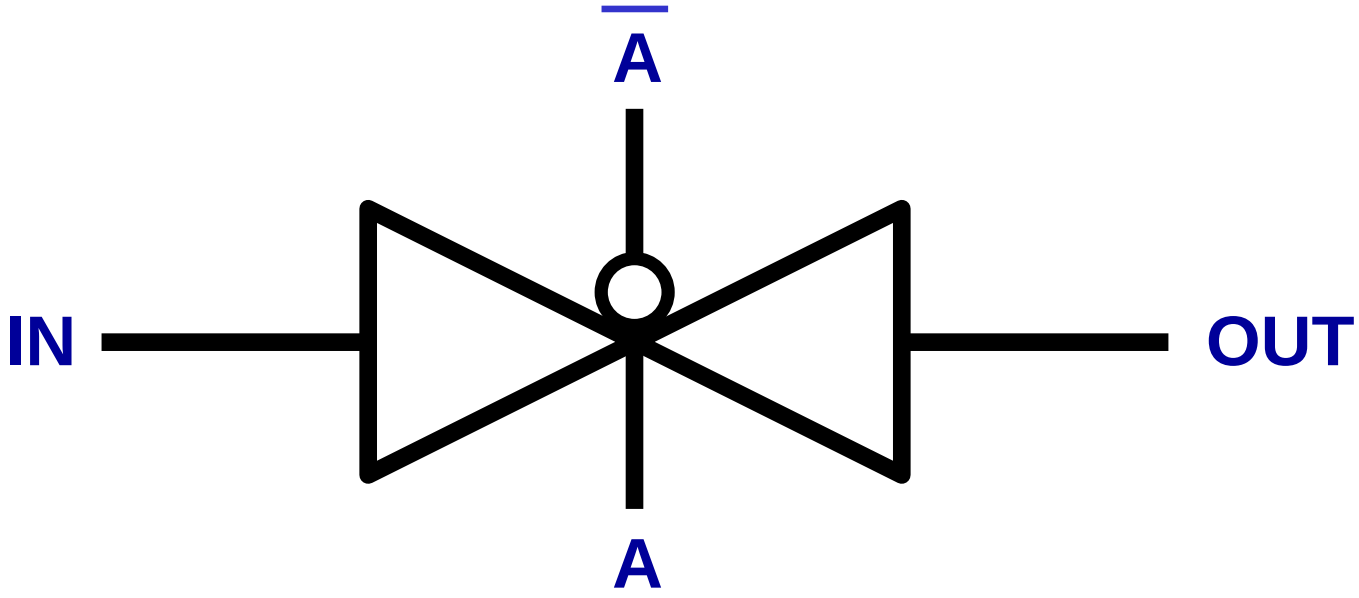
Proper transistor sizing for a four-input NOR gate.

Note that *n* and *p* denote the (*W/L*) rations of Q_N and Q_P, respectively, of the basic inverter.

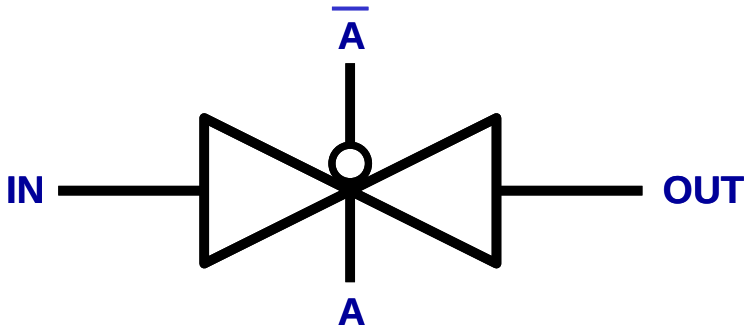
NOR layout


lambda
.175µm
Vdd+
Vss-
nor
PMOSs
NMOSs
Metal
P - diffusion
Polysilicon
N-well
N - diffusion
Metal

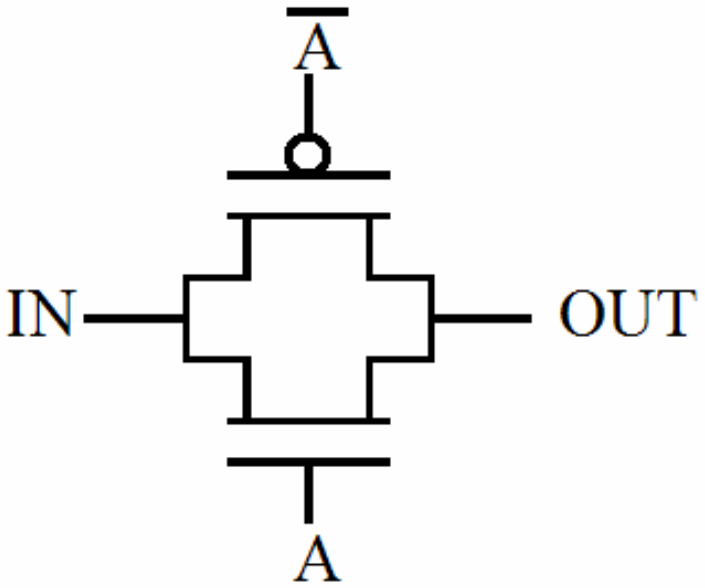
Transmission gate



Transmission gate

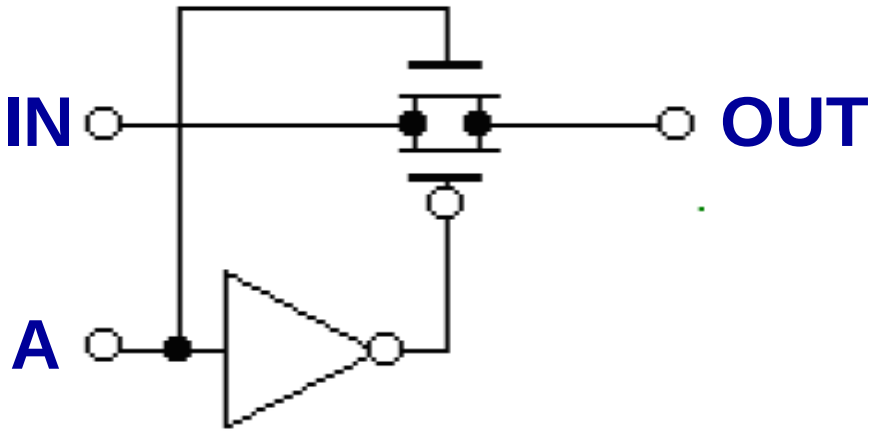


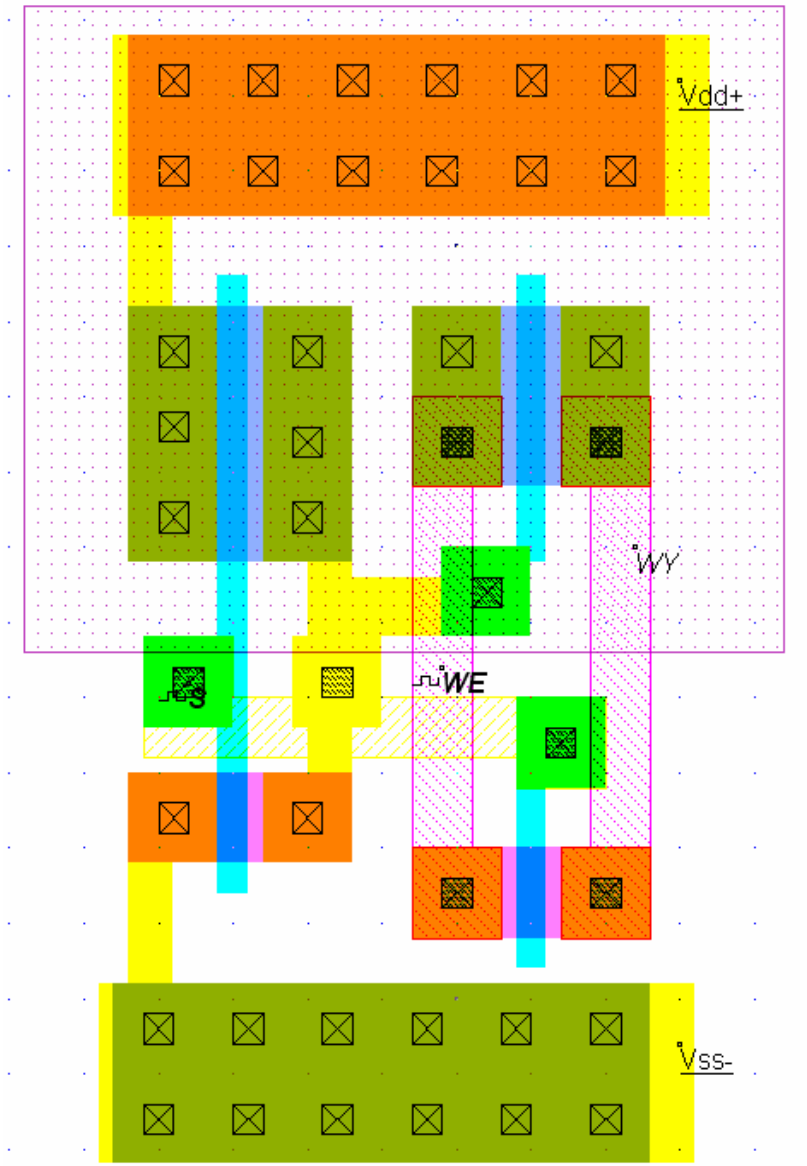
IN	A	OUT
0	0	H
0	1	0
1	0	H
1	1	1



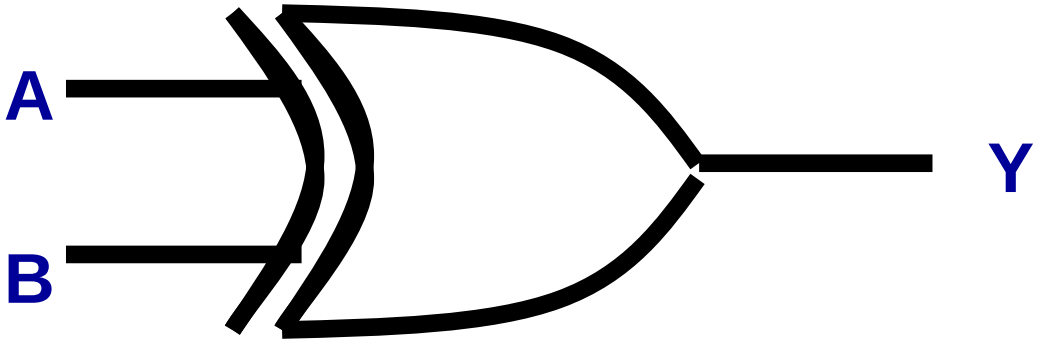
$R_{on} = 100\Omega$ and $R_{off} > 5\ M\Omega$ (high impedance H)

Transmission gate layout

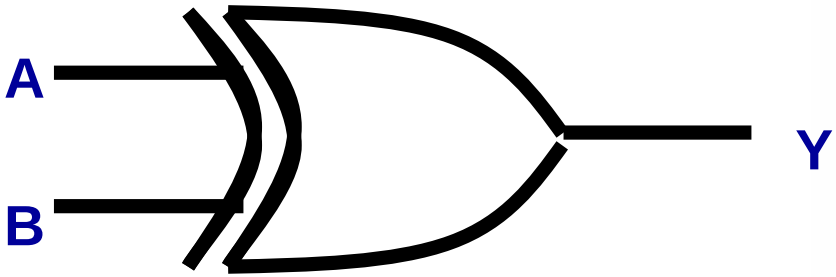


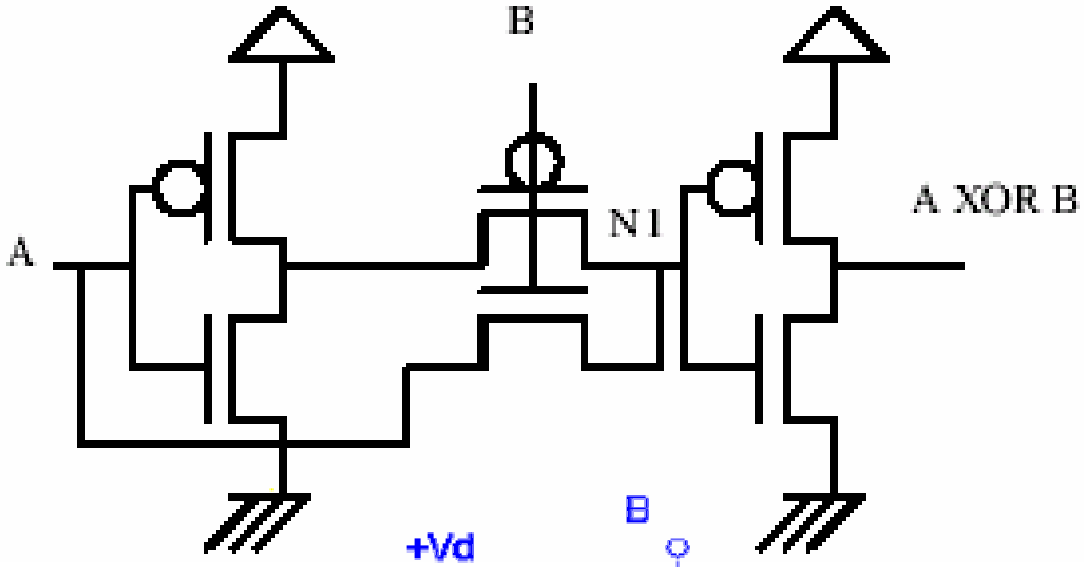


XOR

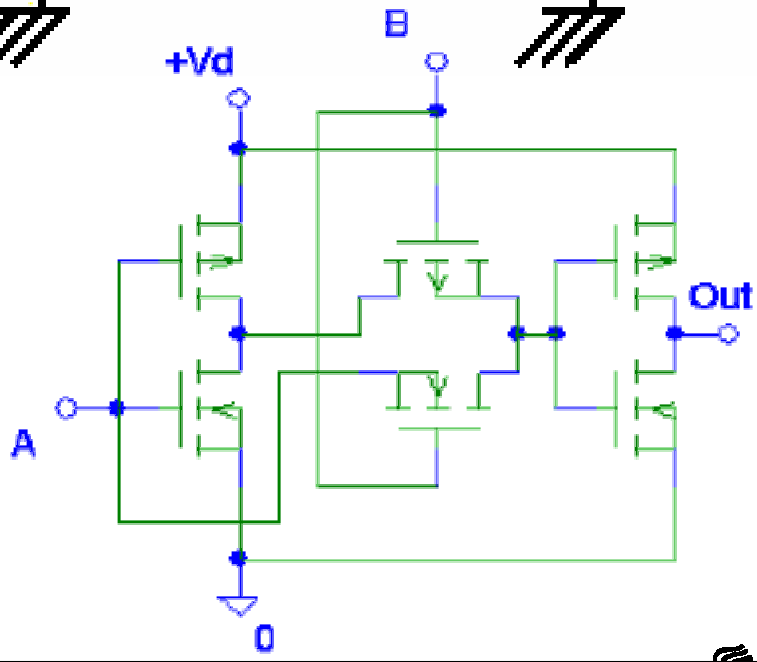


CMOS XOR

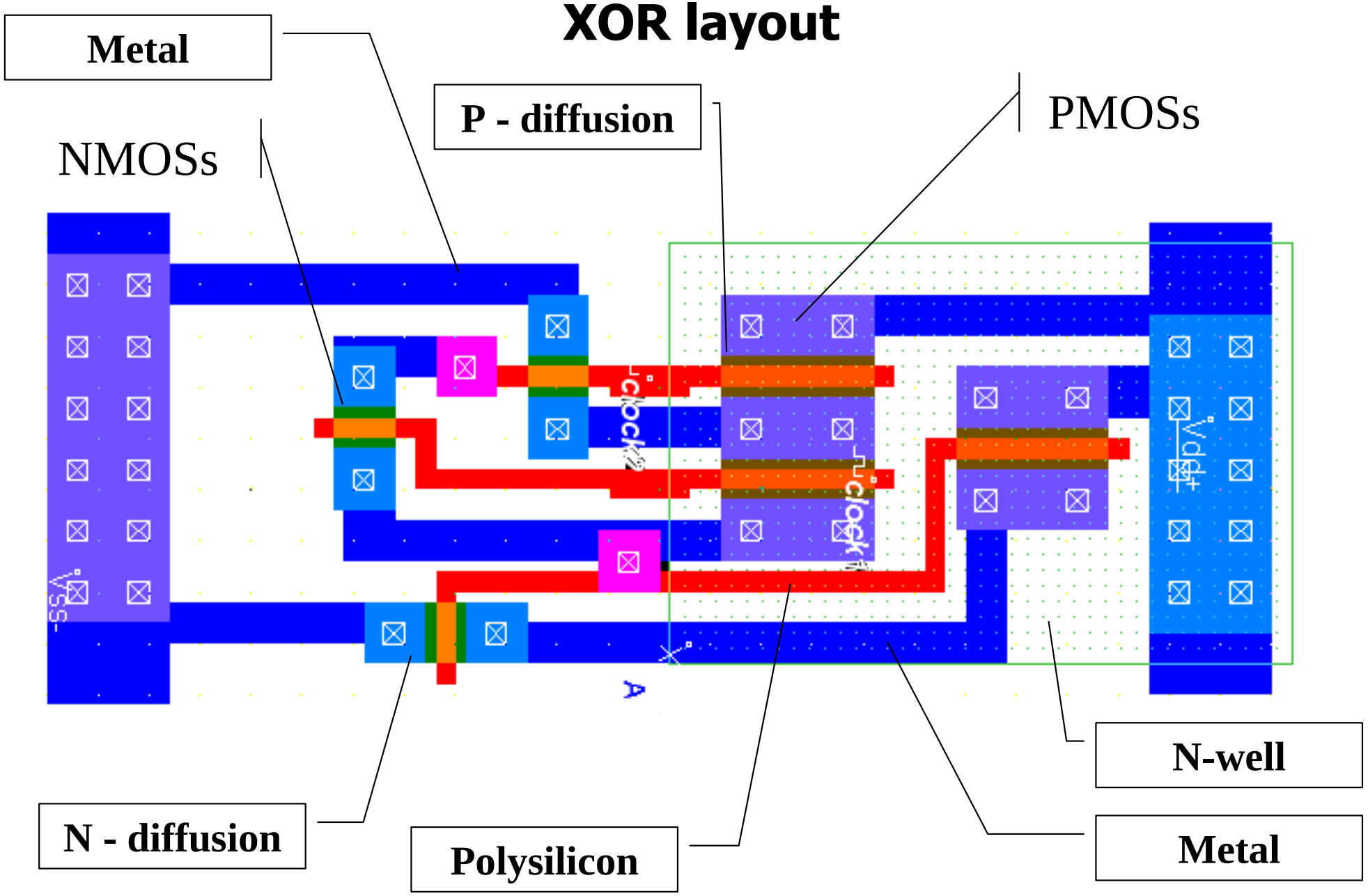




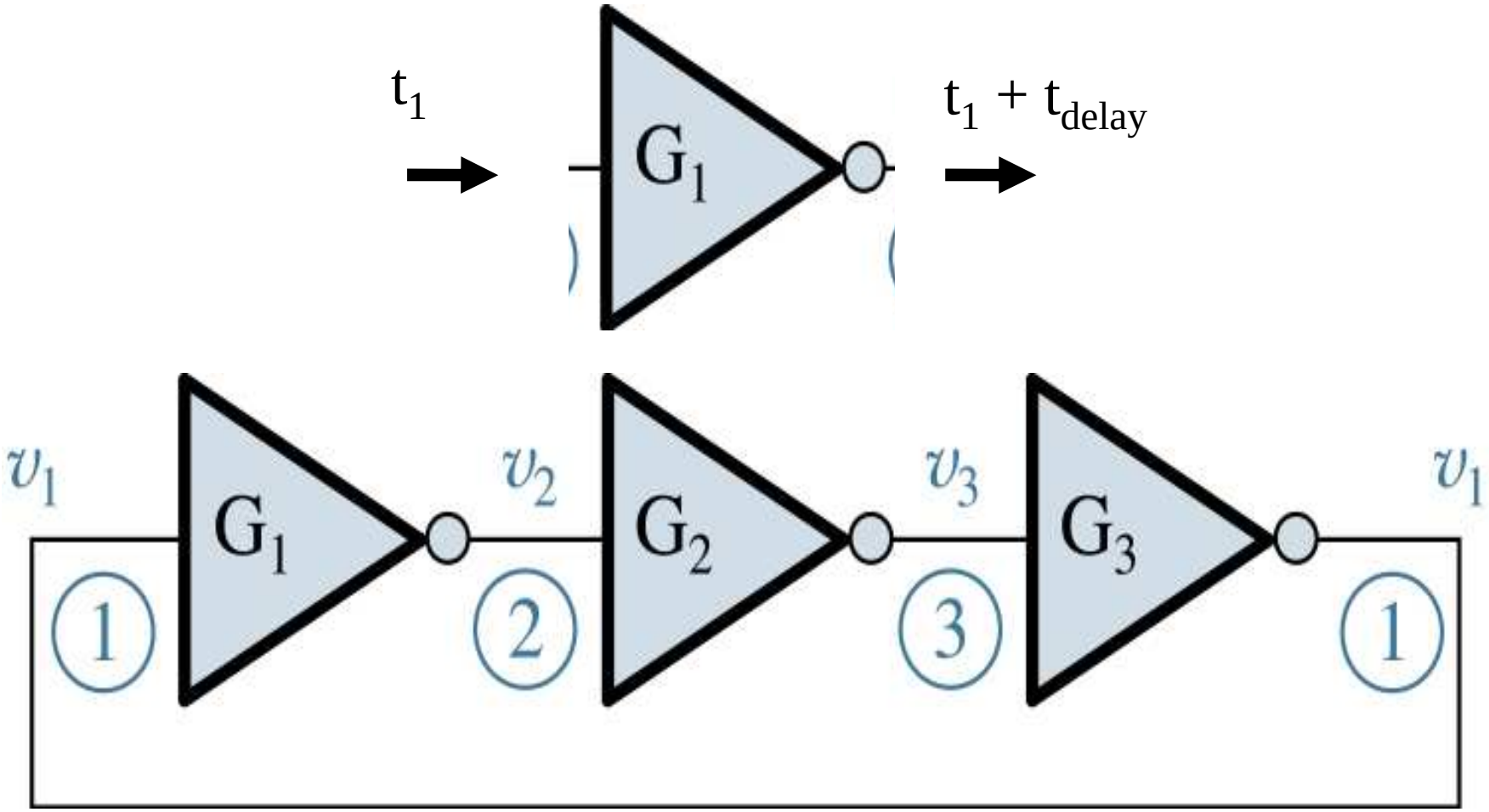
A	B	A xor B
0	0	0
0	1	1
1	0	1
1	1	0



XOR layout


Metal
P - diffusion
PMOSs
NMOSs
clock/2
clock
Vdd
Vss
N-well
N - diffusion
Polysilicon
Metal

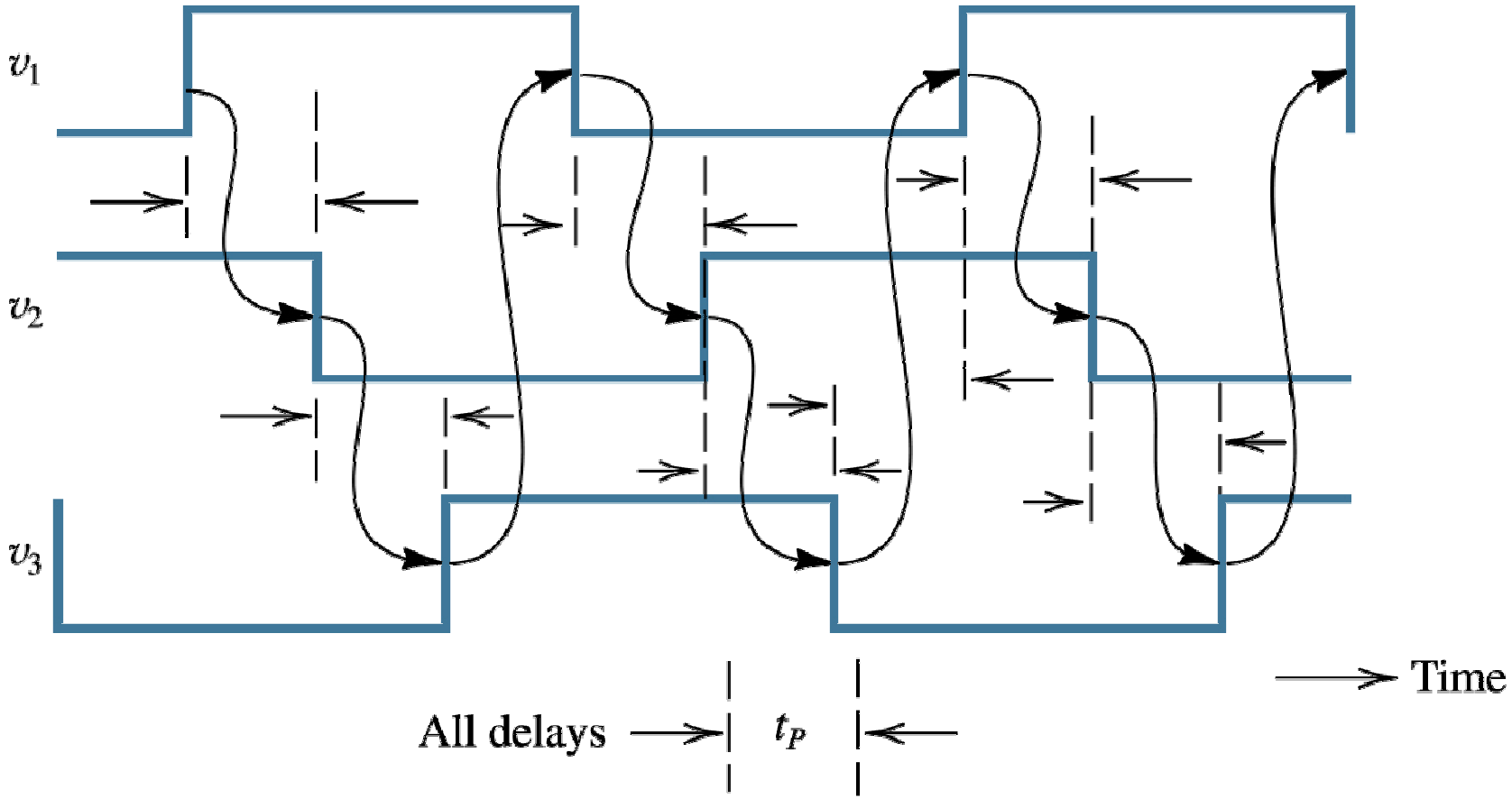
Ring oscillator



Formed by connecting three inverters in cascade

(Normally at least five inverters are used)

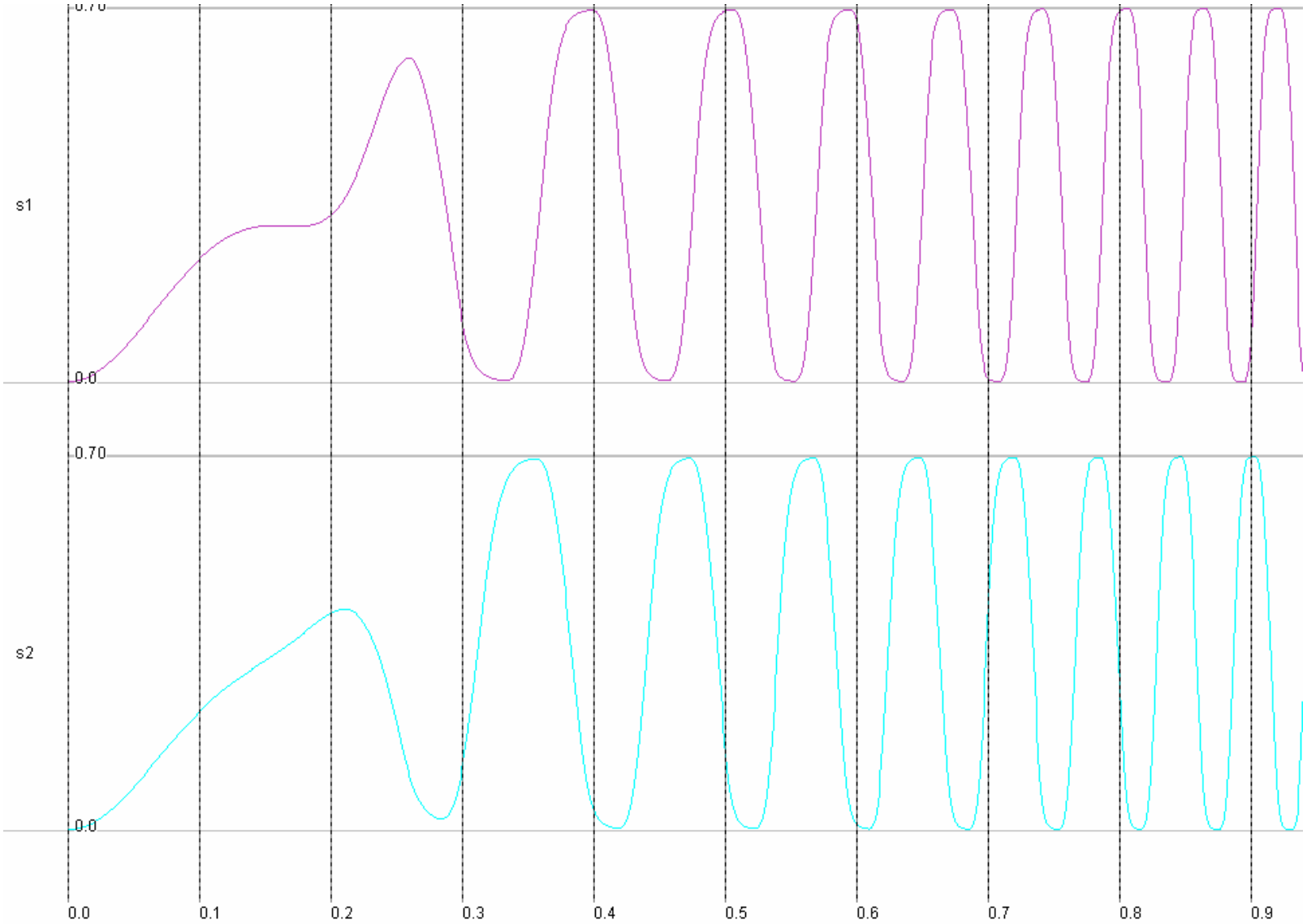
Ring oscillator



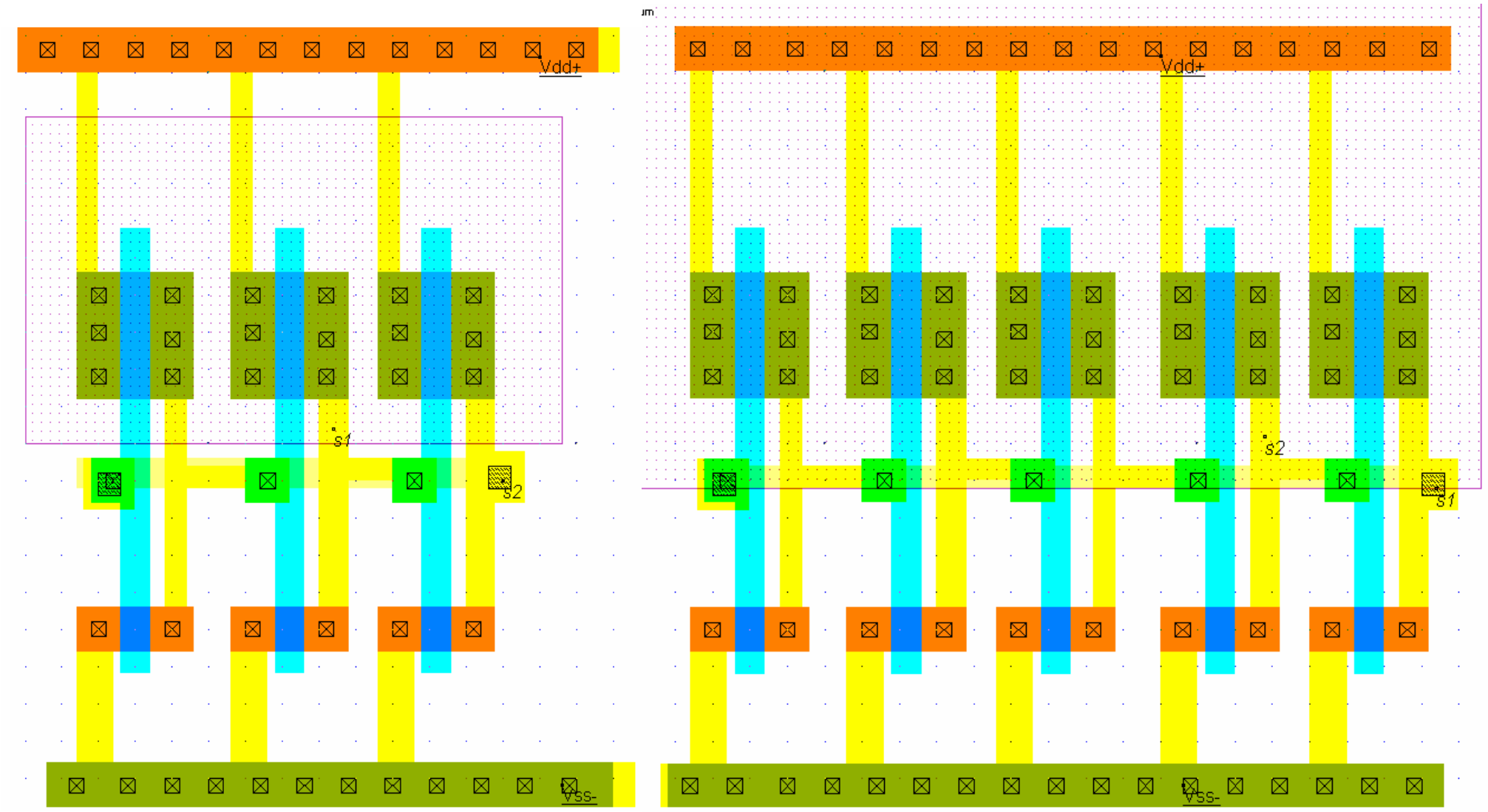
The resulting waveform.

Observe that the circuit oscillates with frequency $1/(6t_p)$.

Waveforms of ring oscillator



Ring Oscillator (3 and 5 NOTs)



Next lecture

More complex devices : MUX, flip-flops

Thank you for your attention