Electronic Technology Design and Workshop

Presented and updated by

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DMCS room 2

2007

Electronic Technology Design and Workshop

Lecture 4

Introduction to Microelectronics

ETDW course road map

- ✓ Schematic edition, libraries of elements
- ✓ Circuit simulation & netlist generation
- ✓ **Microelectronics - full custom design and simulation**
- ✓ Microelectronics - simple layout synthesis
- ✓ Hardware description languages - behavioural description
- ✓ Logic & sequential synthesis - programmable logic devices
- ✓ PCB design – auto-routing

- Project - bringing the pieces together

What is Microelectronics ?

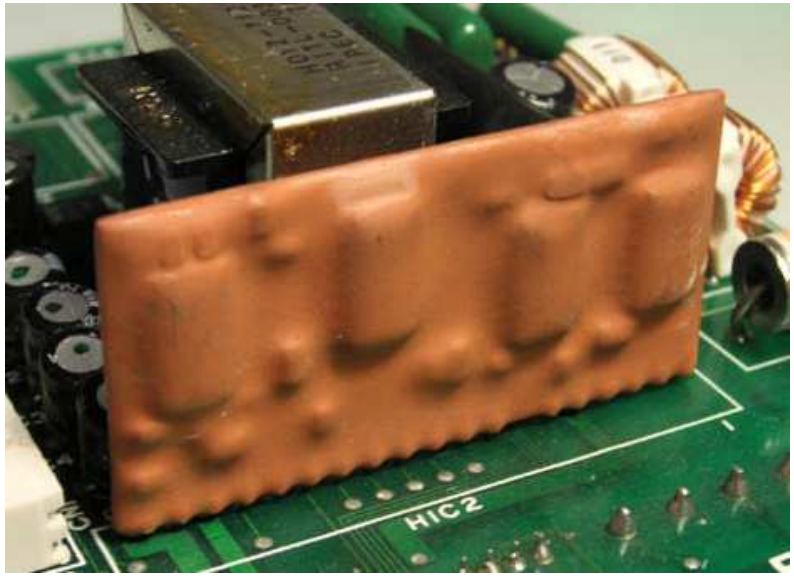
MICROELECTRONICS [gr.], part of electronics considering behavior, constructions and fabrication technology of → integrated circuits

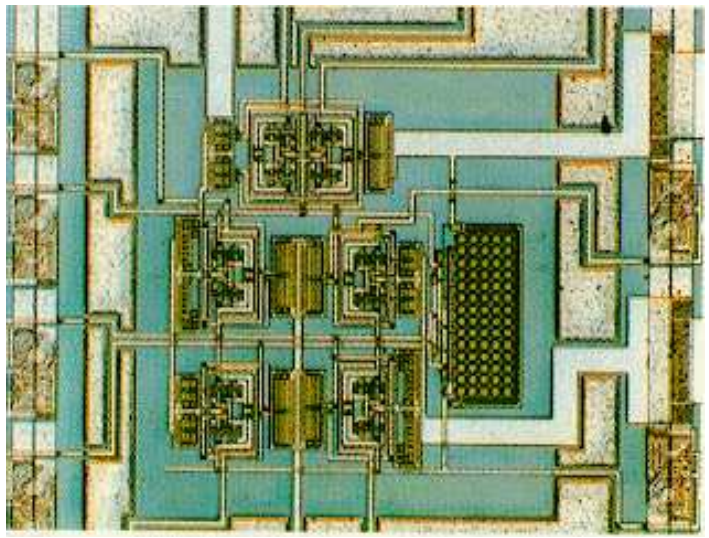
What is integrated circuit ?

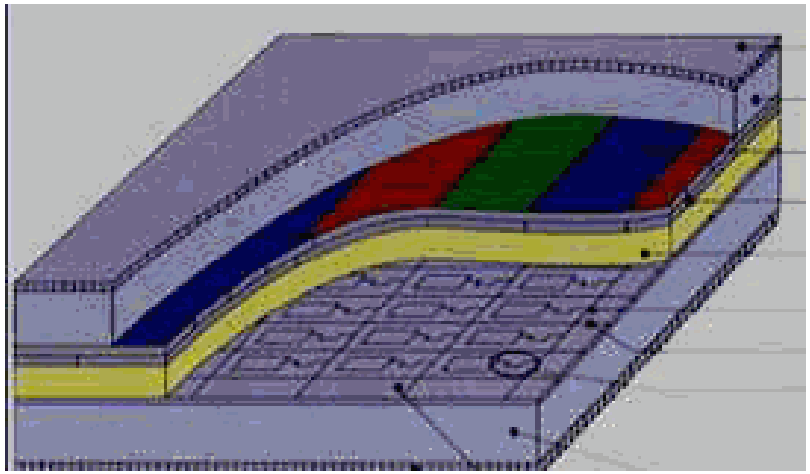
INTEGRATED CIRCUIT, electronic device (microchip), where some or all components including interconnections are fabricated during single technological process in the single silicon substrate.

Integrated Circuit Types

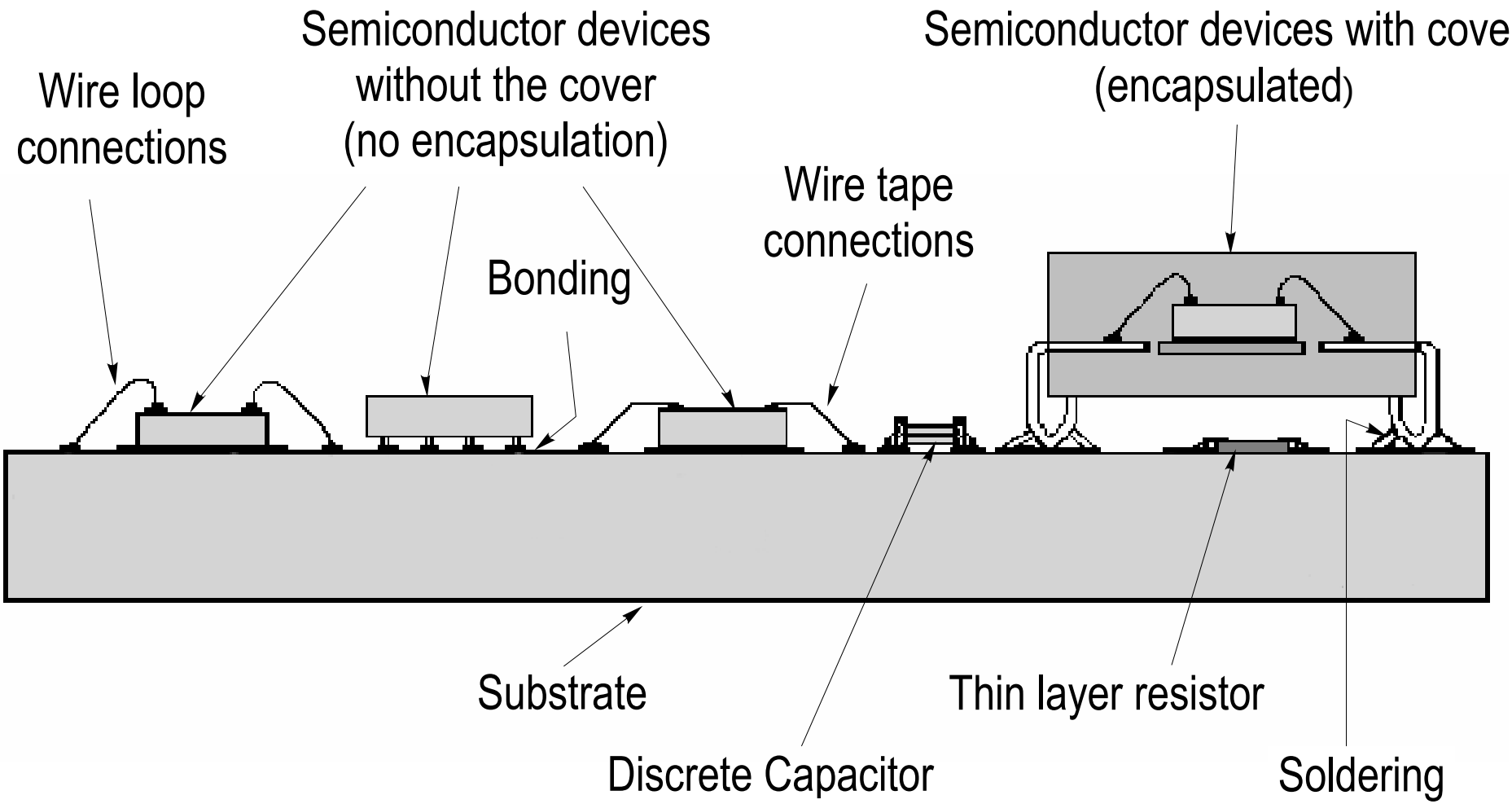
- **Hybrid**
  - Thick Layer
  - Thin Layer
- **Monolithic**



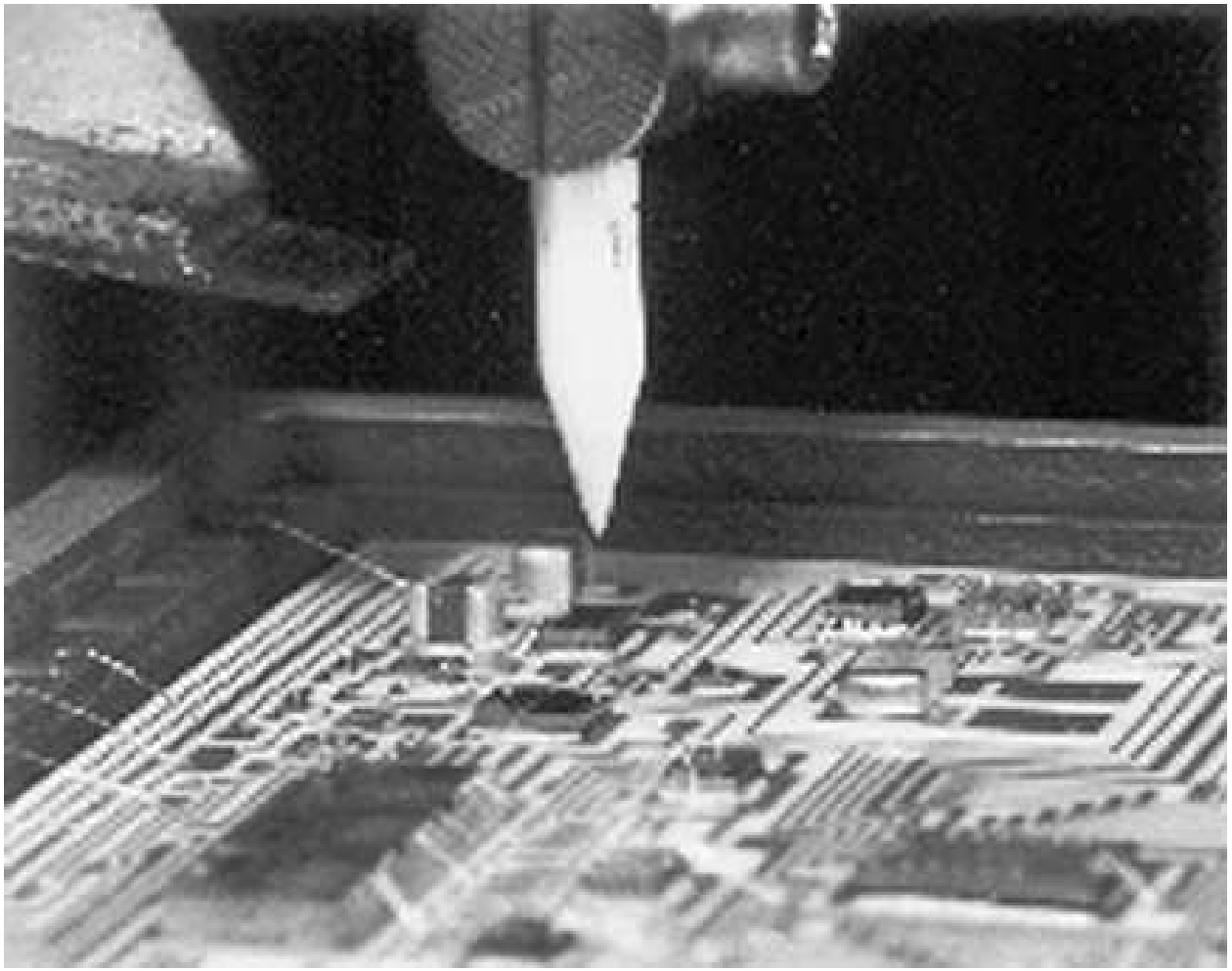




Thick Layer Integrated Circuits

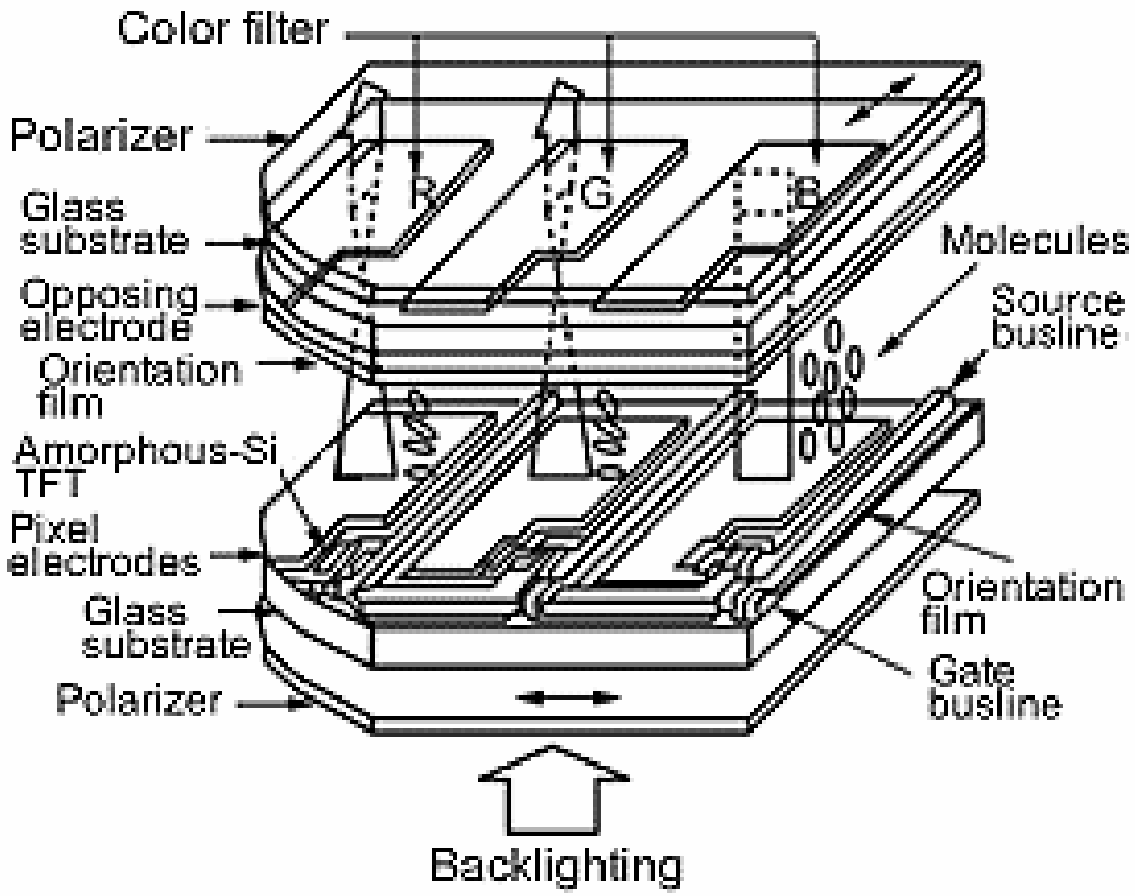


Thick Layer Integrated Circuits

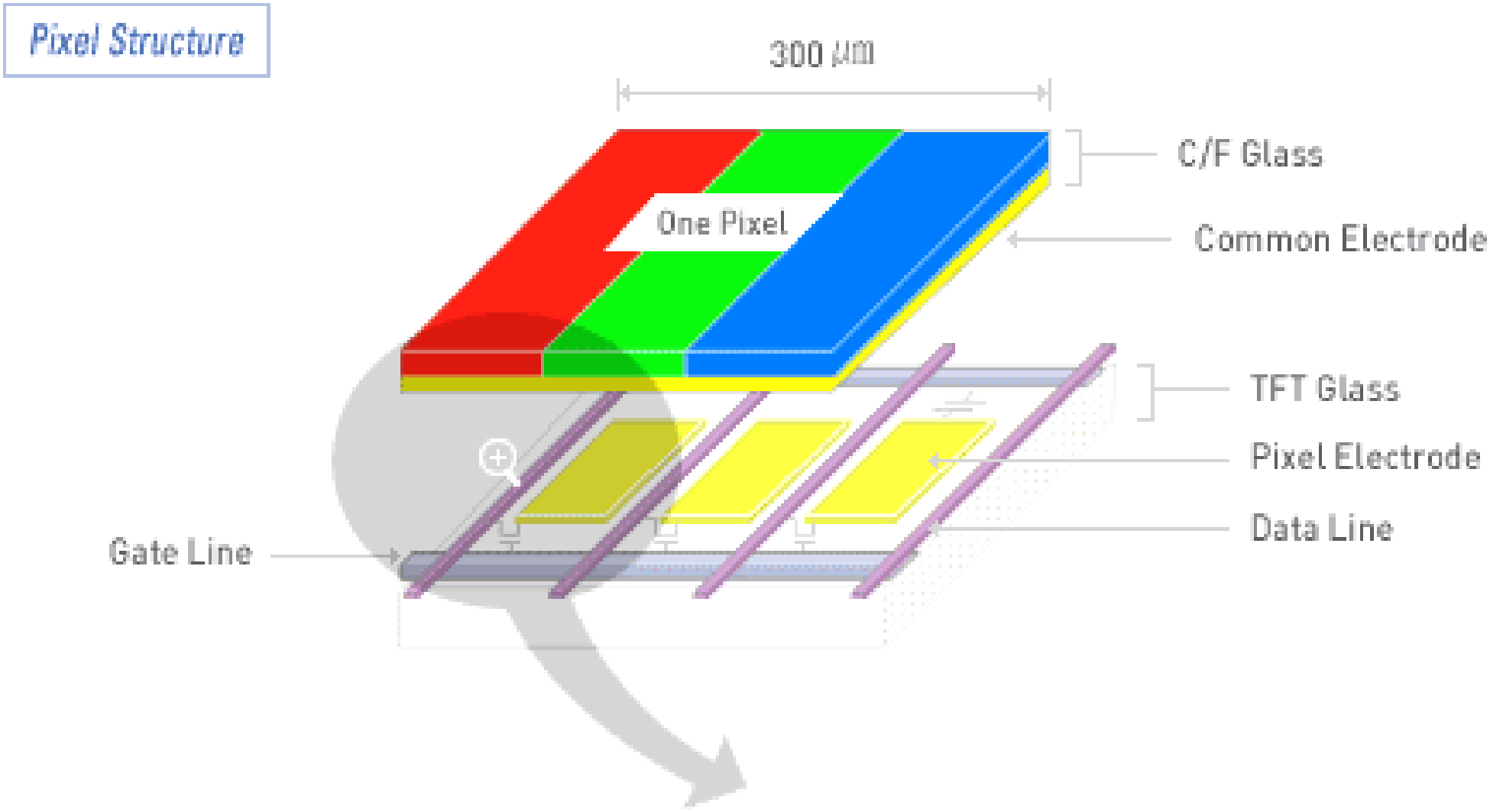


Thin Layer Integrated Circuits

i.e. thin-film transistor (TFT)

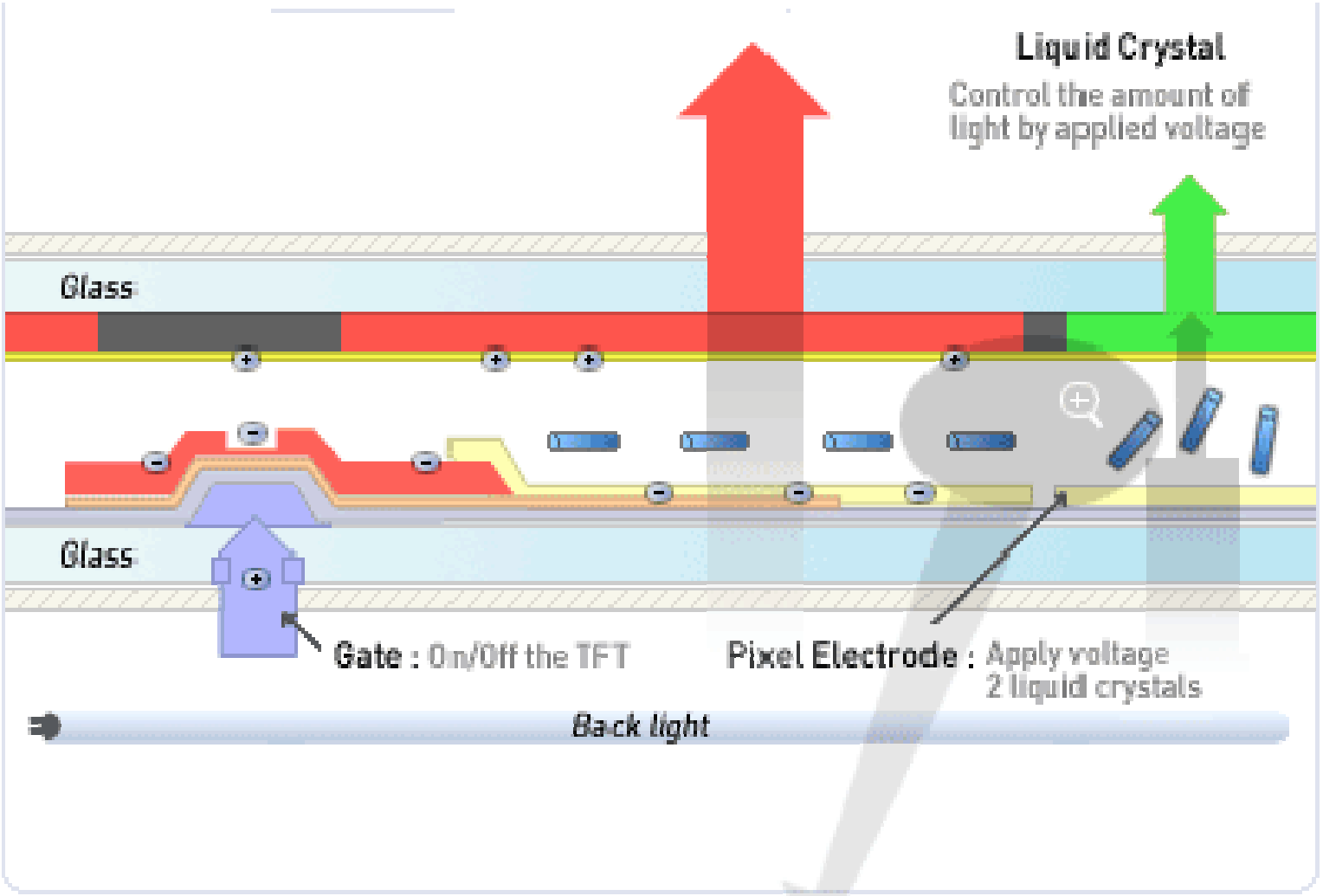


TFT (1)


Pixel Structure
300 μm
One Pixel
C/F Glass
Common Electrode
TFT Glass
Pixel Electrode
Data Line
Gate Line

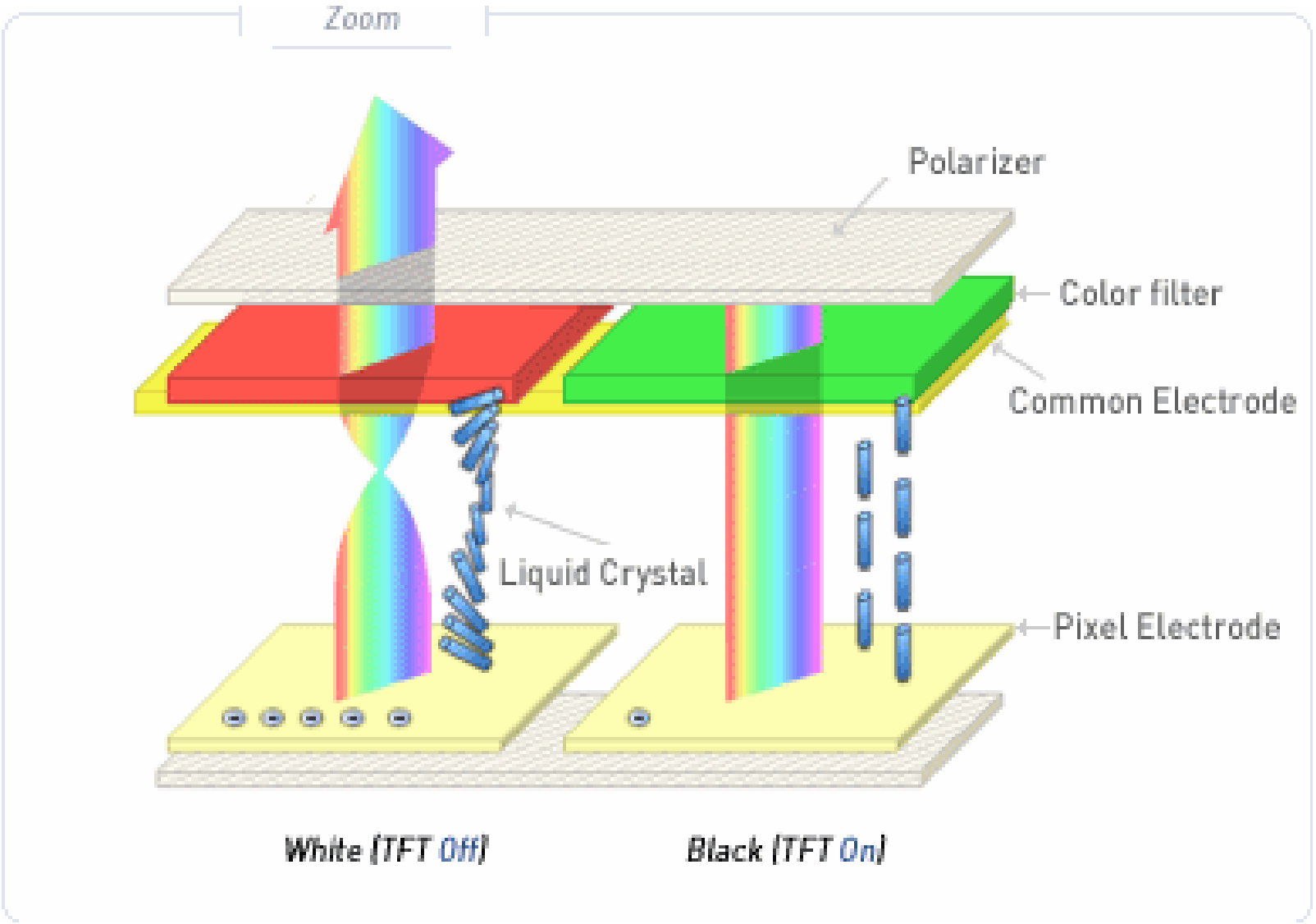
TFT (2)

TFT-LCD Cross Section

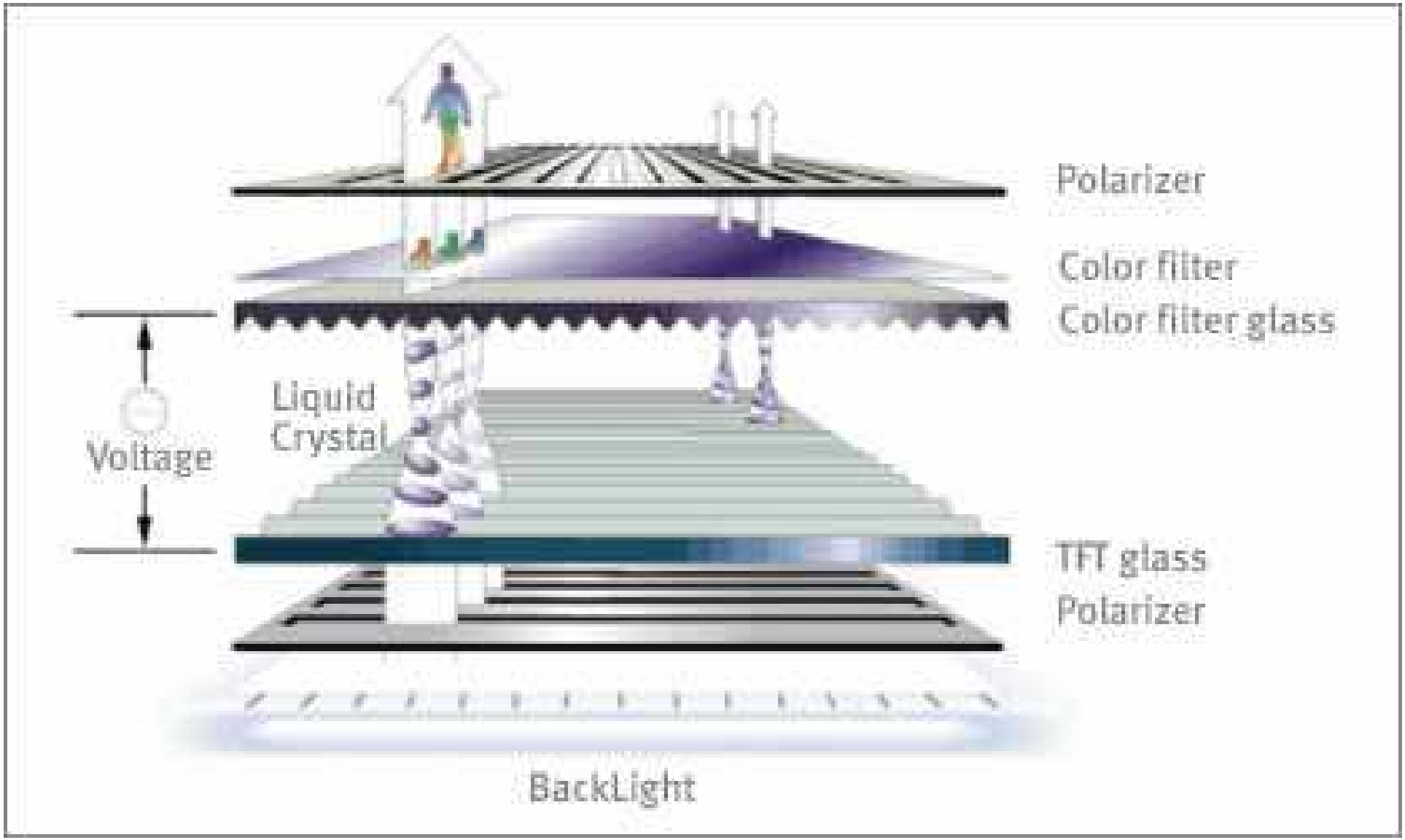


TFT (3)

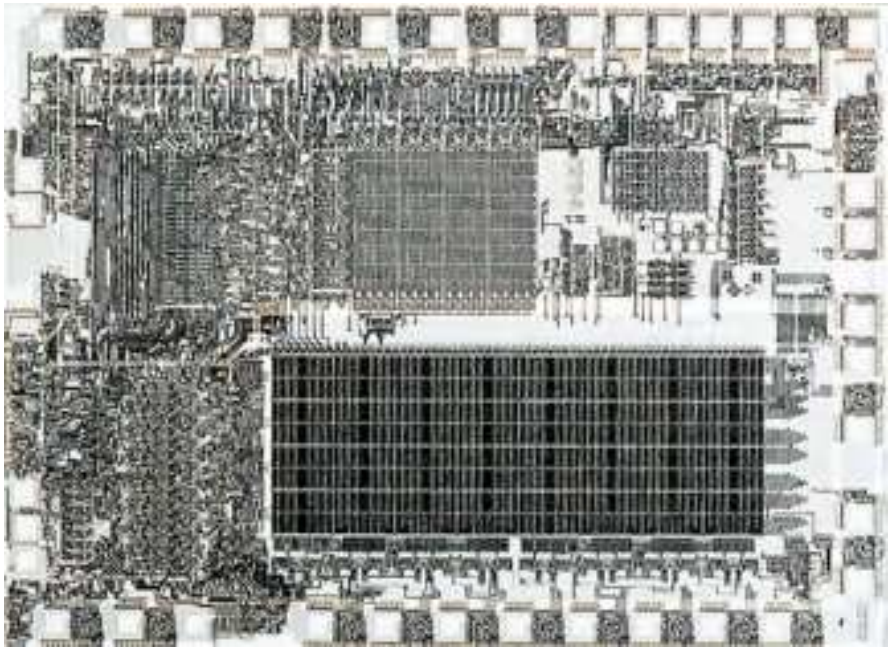
How it works

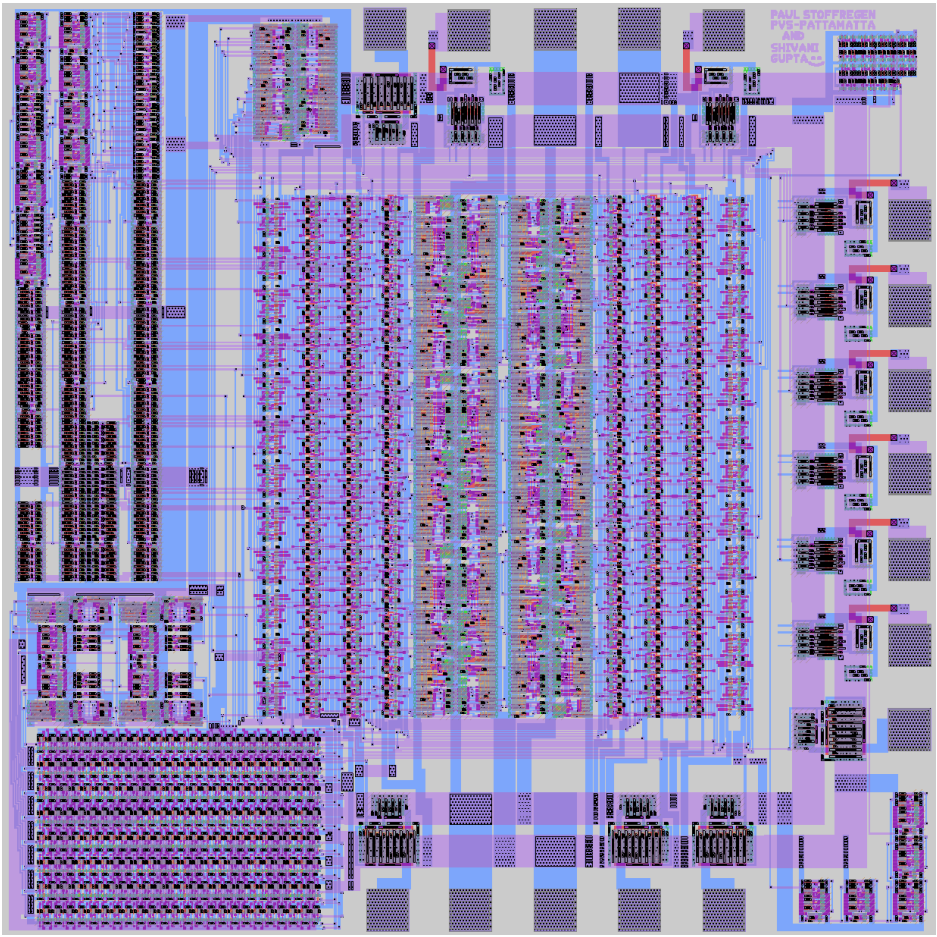


TFT (4)


Polarizer
Color filter
Color filter glass
Liquid Crystal
Voltage
TFT glass
Polarizer
BackLight

Monolithic Integrated Circuits





Integrated Circuits Advantages

- Low cost
- Small dimensions
- Reliability
- Identity of temperature characteristics

Monolithic Integrated Circuits

- Standard
- Application Specific (ASIC)

Standard Circuits Advantages

- Low cost
- “off shelf” accessibility
- Verified reliability
- Many suppliers and manufacturers (usually)

Standard Circuits Disadvantages

- Not optimized for specific problems
- Large area occupation

ASIC Advantages

- Easy parameter optimization for specific system
- Effective area usage
- Higher reliability and decreased number of devices on board

ASIC Disadvantages

- High cost for low series
- High project costs
- Single Supplier
- Long designing time

Specialized Circuits

- Programmable (FPLD)
- Semi-custom
- Custom

Field Programmable Logic Devices

- Writable
- Writable / erasable
- Volatile

"Field Engineer"

Semi-custom circuits

- Gate array
- Linear array

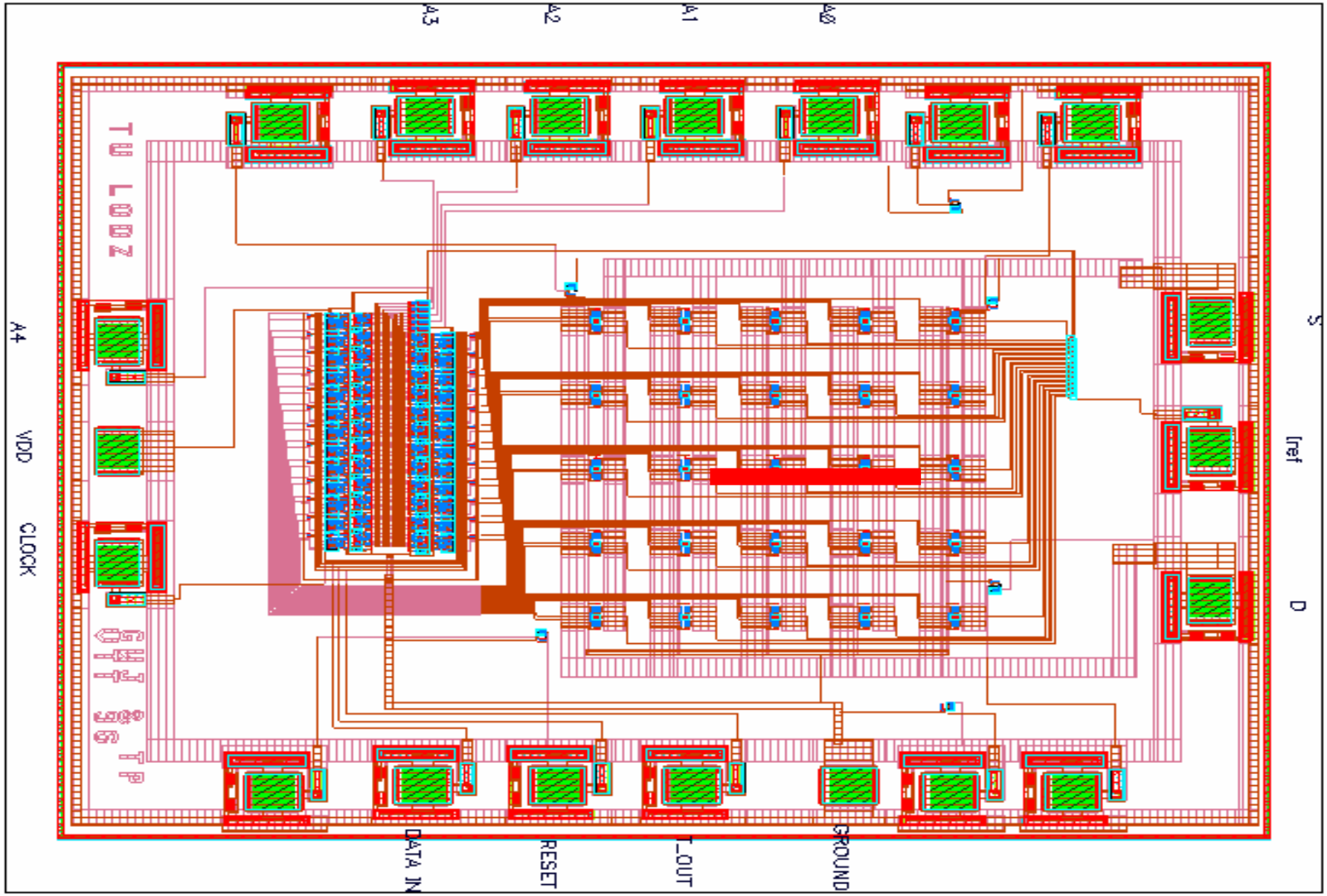
Custom Circuits

- Standard Cell
- Full Custom

Designer Tasks

- Draw the circuit
- Draw the state diagram
- Describe behavior using high level language i.e. VHDL or Verilog
- Draw masks of integrated circuit

Designer Task



Design Tools

- Xilinx
- Synopsis/Viewlogic
- Compass
- Cadence
- Mentor Graphics

Design tools functions

- Edition of text, circuit scheme, topography
- Synthesis
- Topography and scheme comparison
- Design rules checking
- Component positioning and interconnecting
- Simulation

MOS TRANSISTOR (Metal-Oxide-Semiconductor)

BASICS

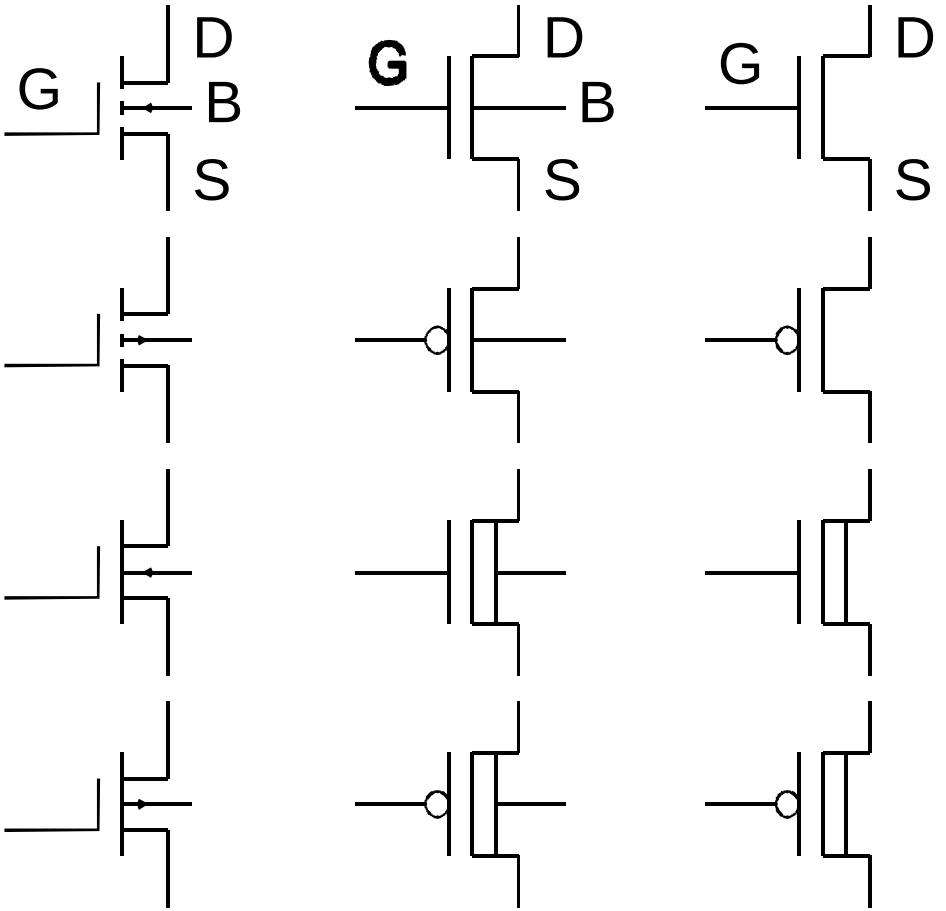
MOS Transistor Symbols

Enhanced Mode n-type Transistor

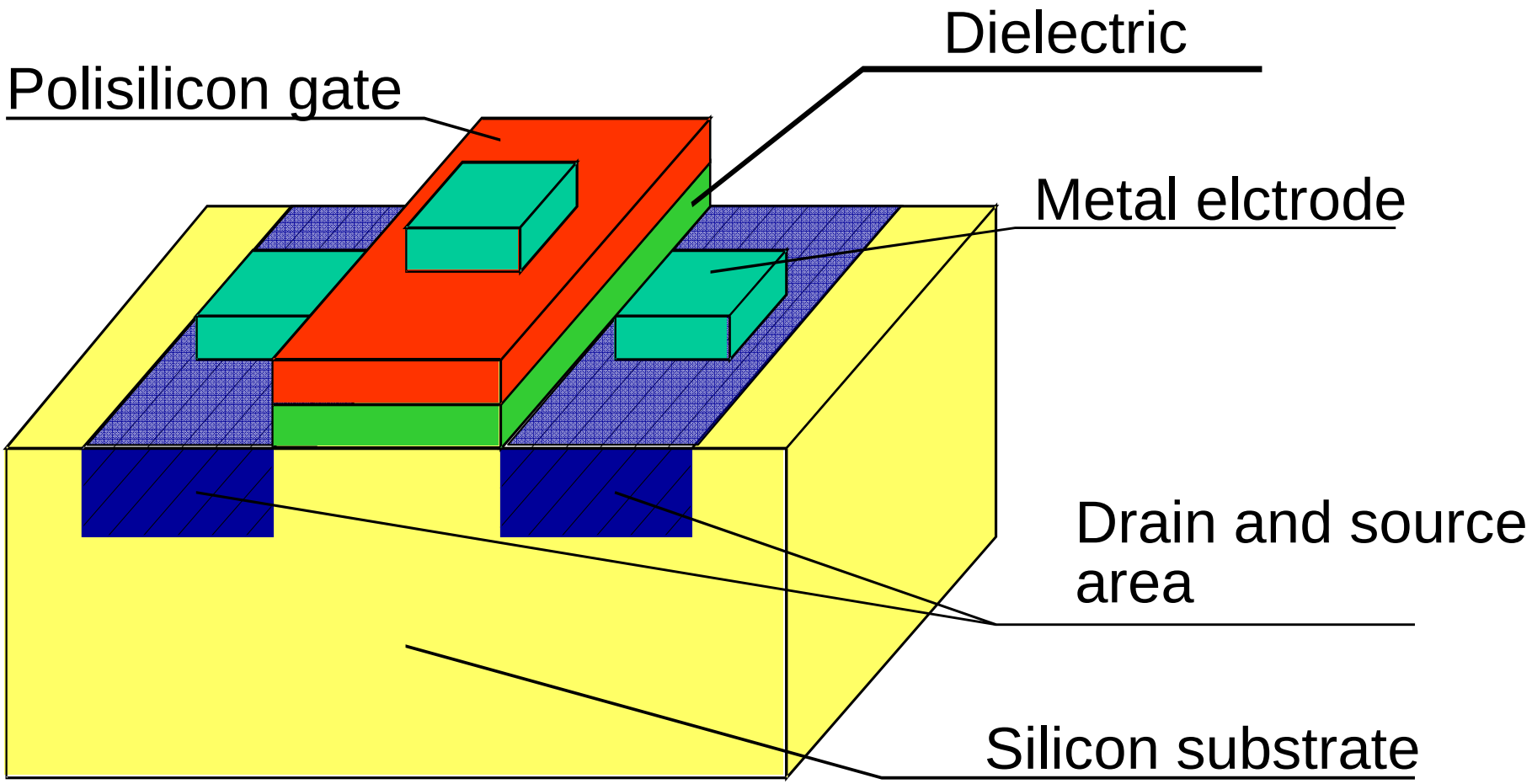
Enhanced Mode p-type Transistor

Depleted Mode n-type Transistor

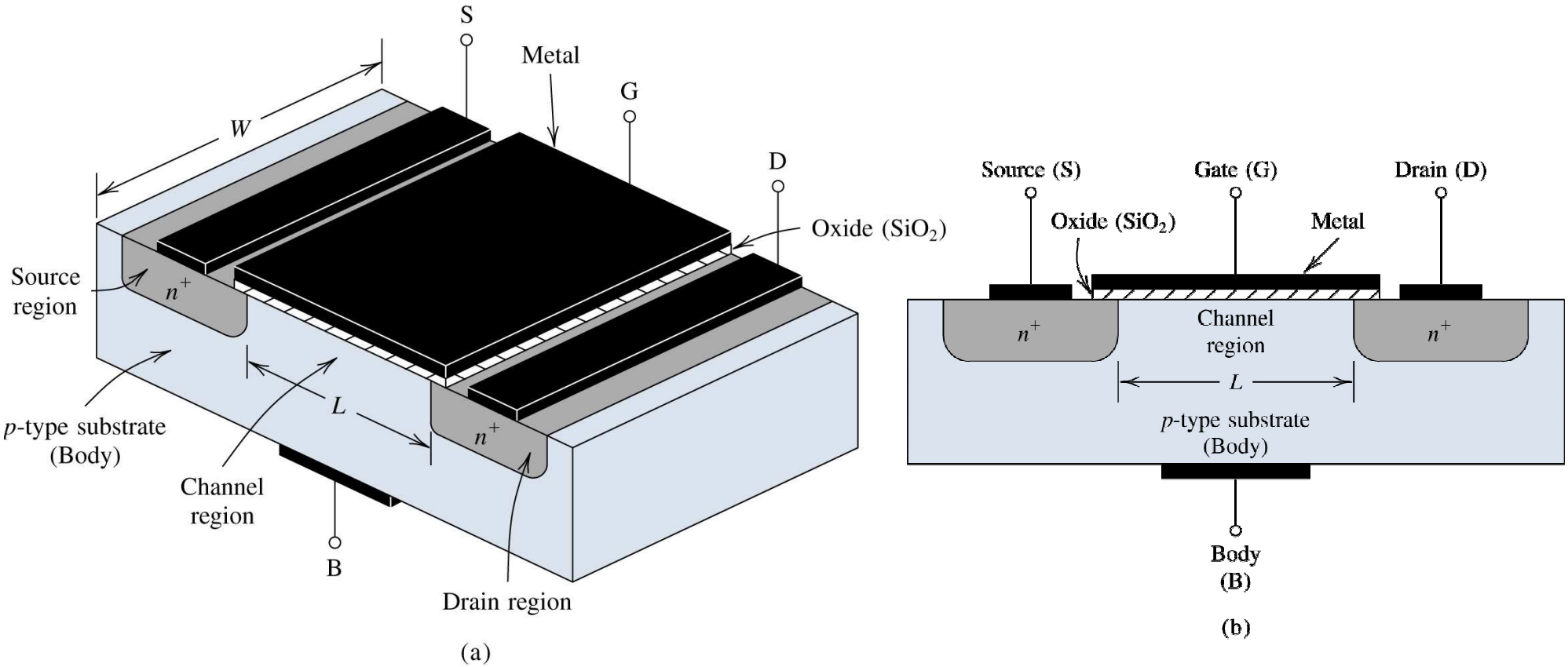
Depleted Mode p-type Transistor



MOS Transistor



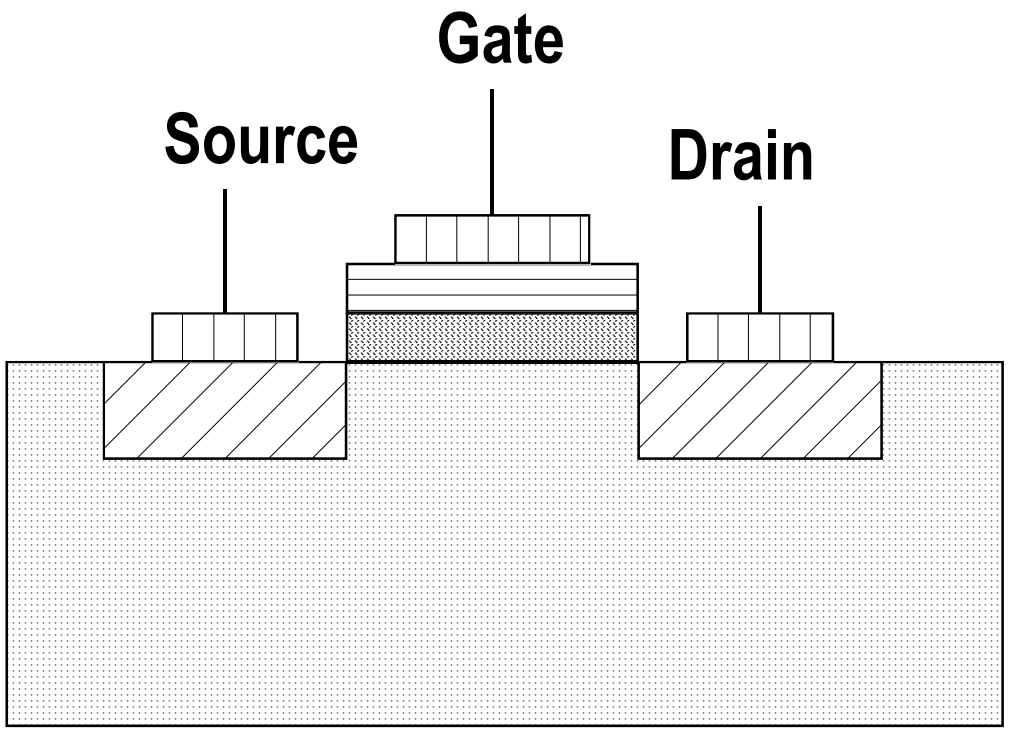
nMOS Transistor – physical structure

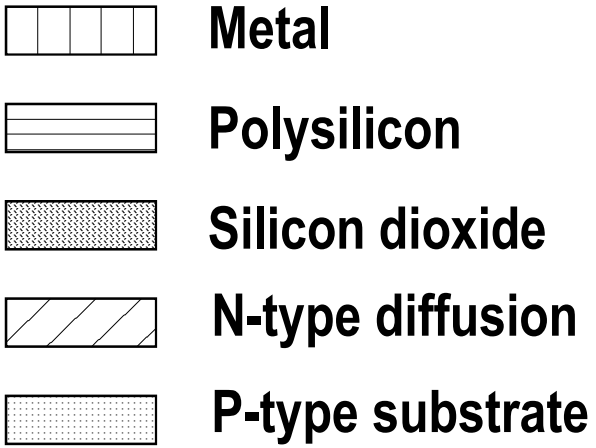


Enhancement-type NMOS transistor: (a) perspective view (b) cross section

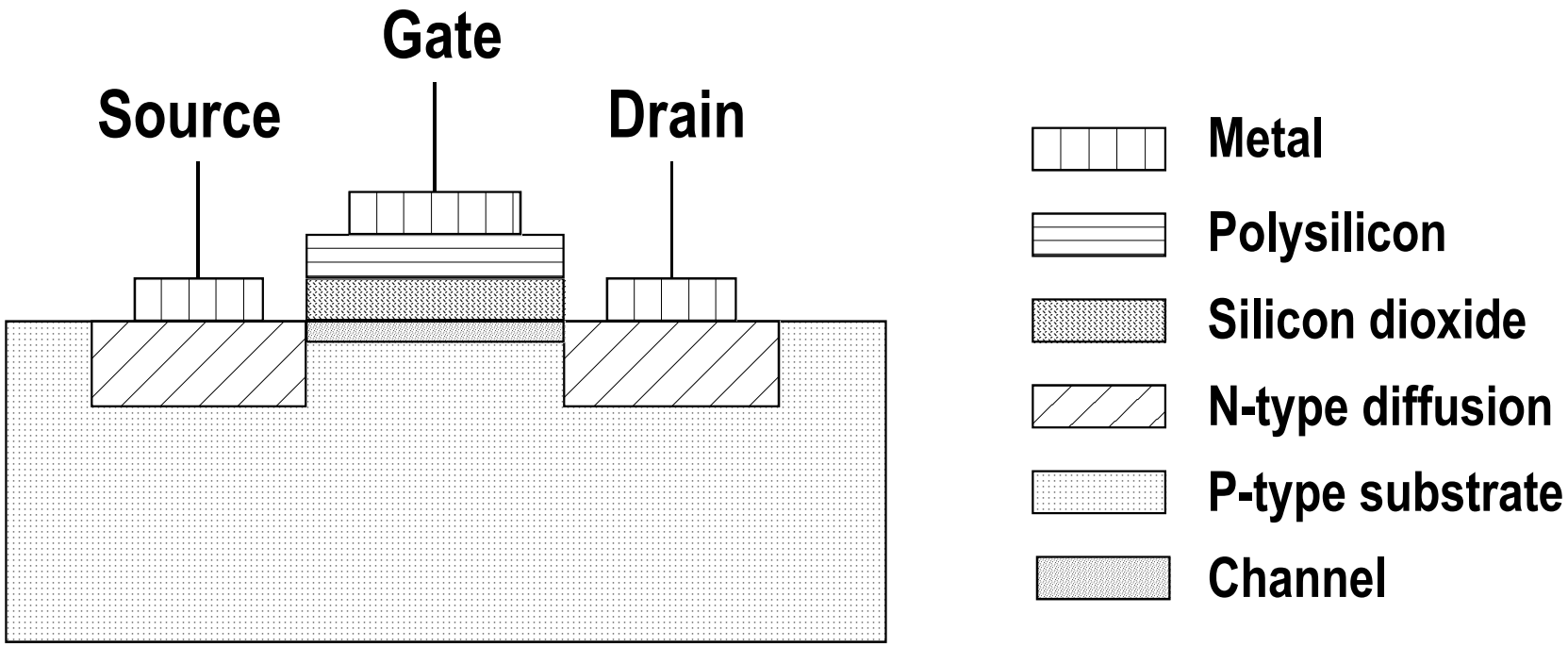
Typically L = 1 to 10 μm, W = 2 to 500 μm,
and the thickness of the oxide layer is in the range of 0.02 to 0.1 μm.

nMOS Transistor cross-section

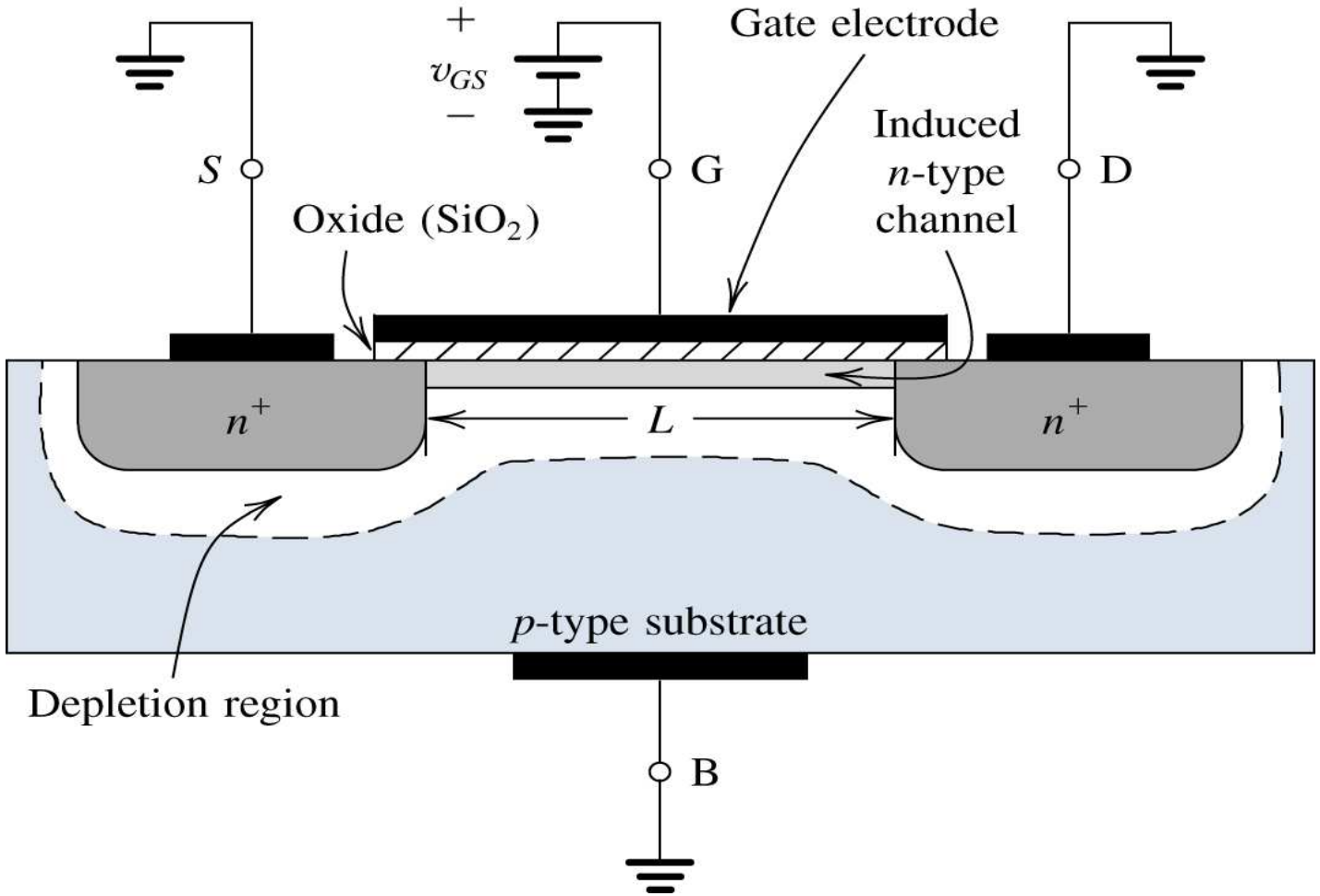




nMOS Transistor with polarised gate cross-section

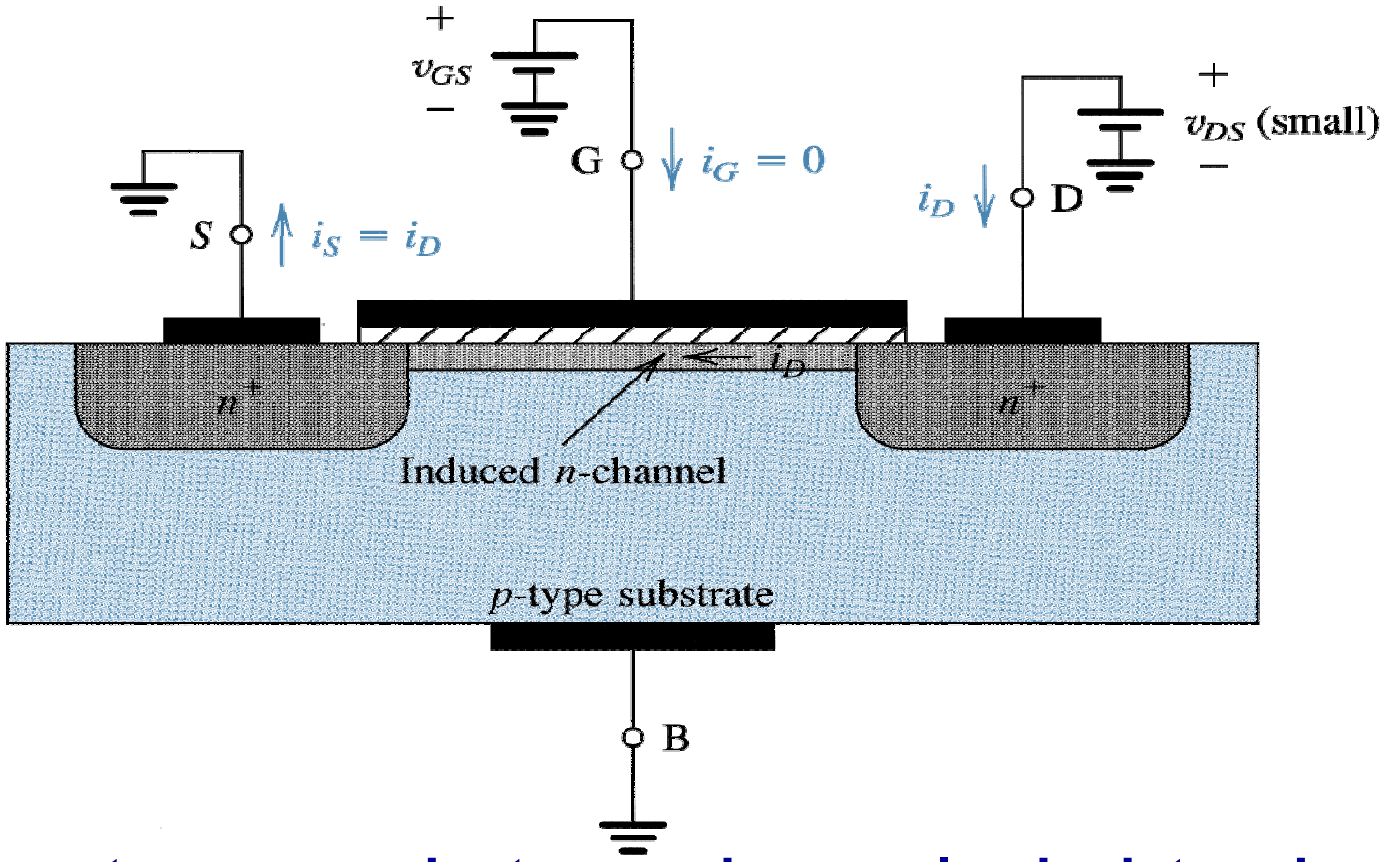


nMOS operation - positive voltage applied to the gate



An n channel is induced at the top of the substrate beneath the gate.

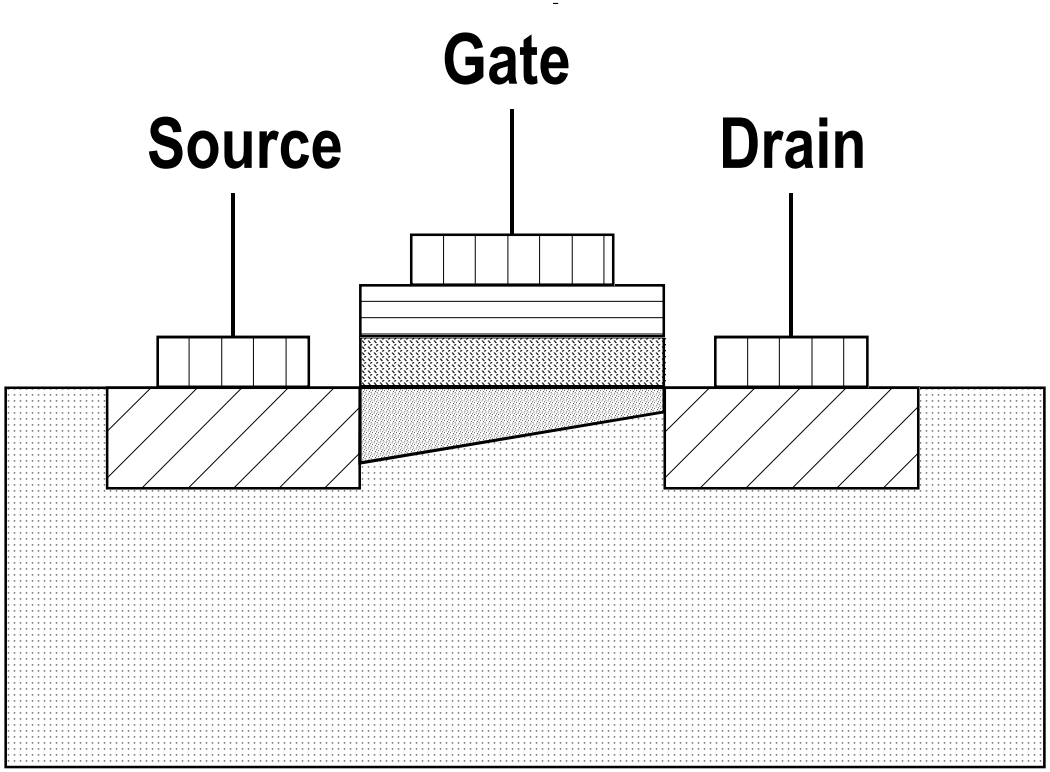
nMOS operation - $V_{GS} > V_t$ and with a small V_{DS} applied

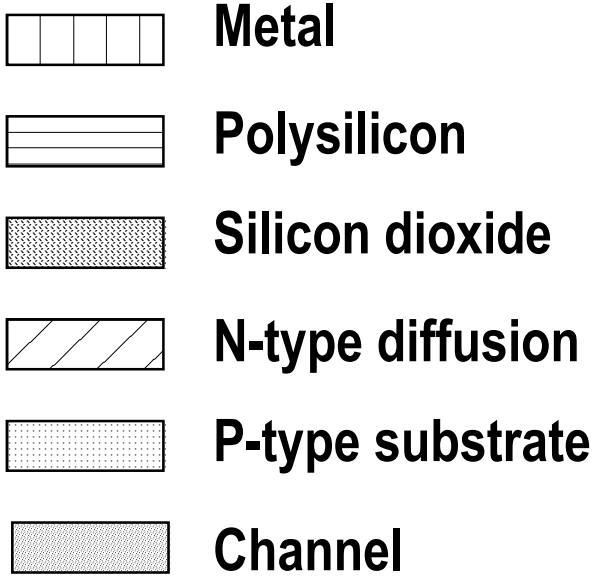


The device acts as a conductance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and this i_D is proportional to $(v_{GS} - Vt)\ v_{DS}$.

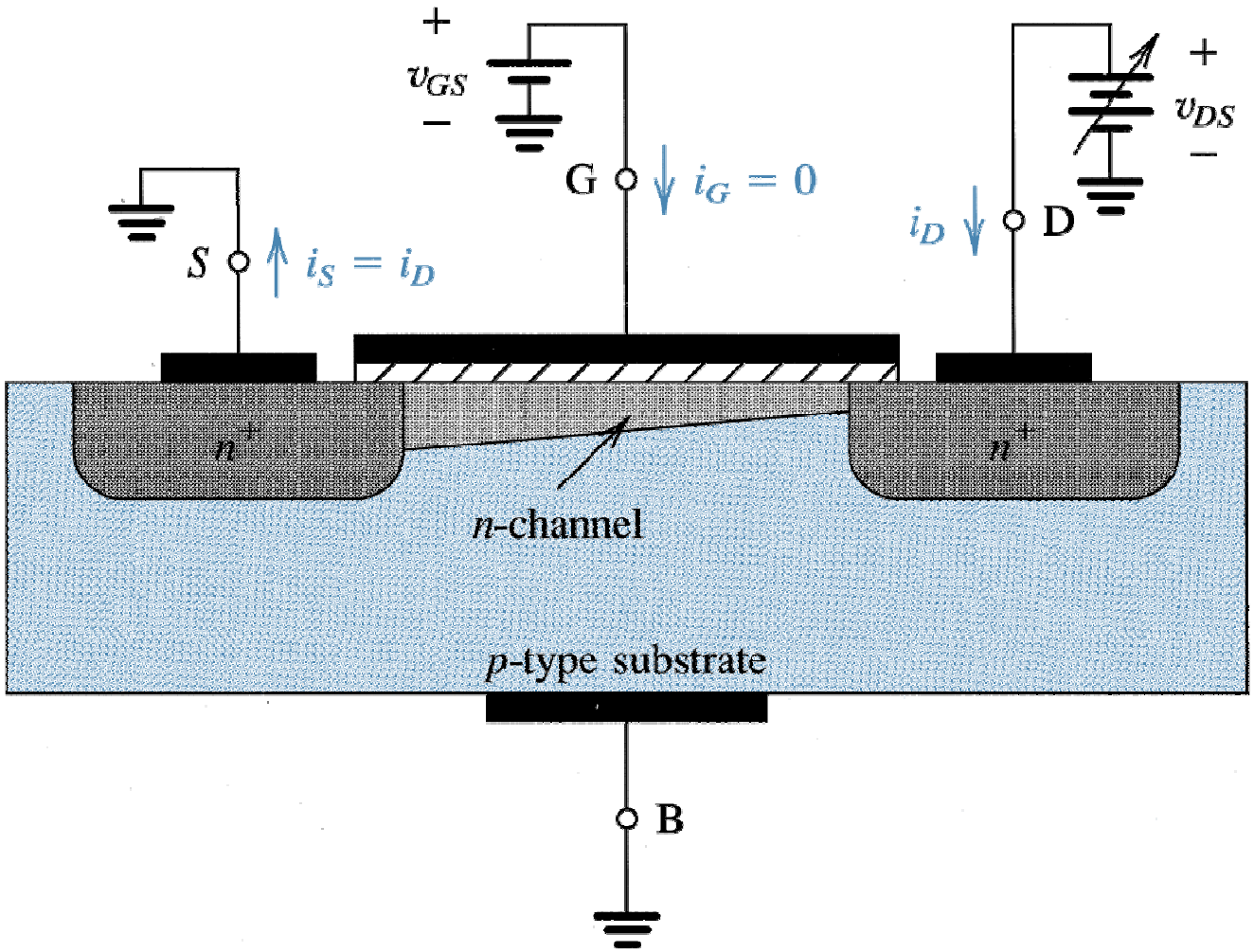
Note that the depletion region is not shown (for simplicity).

nMOS Transistor In Linear Range





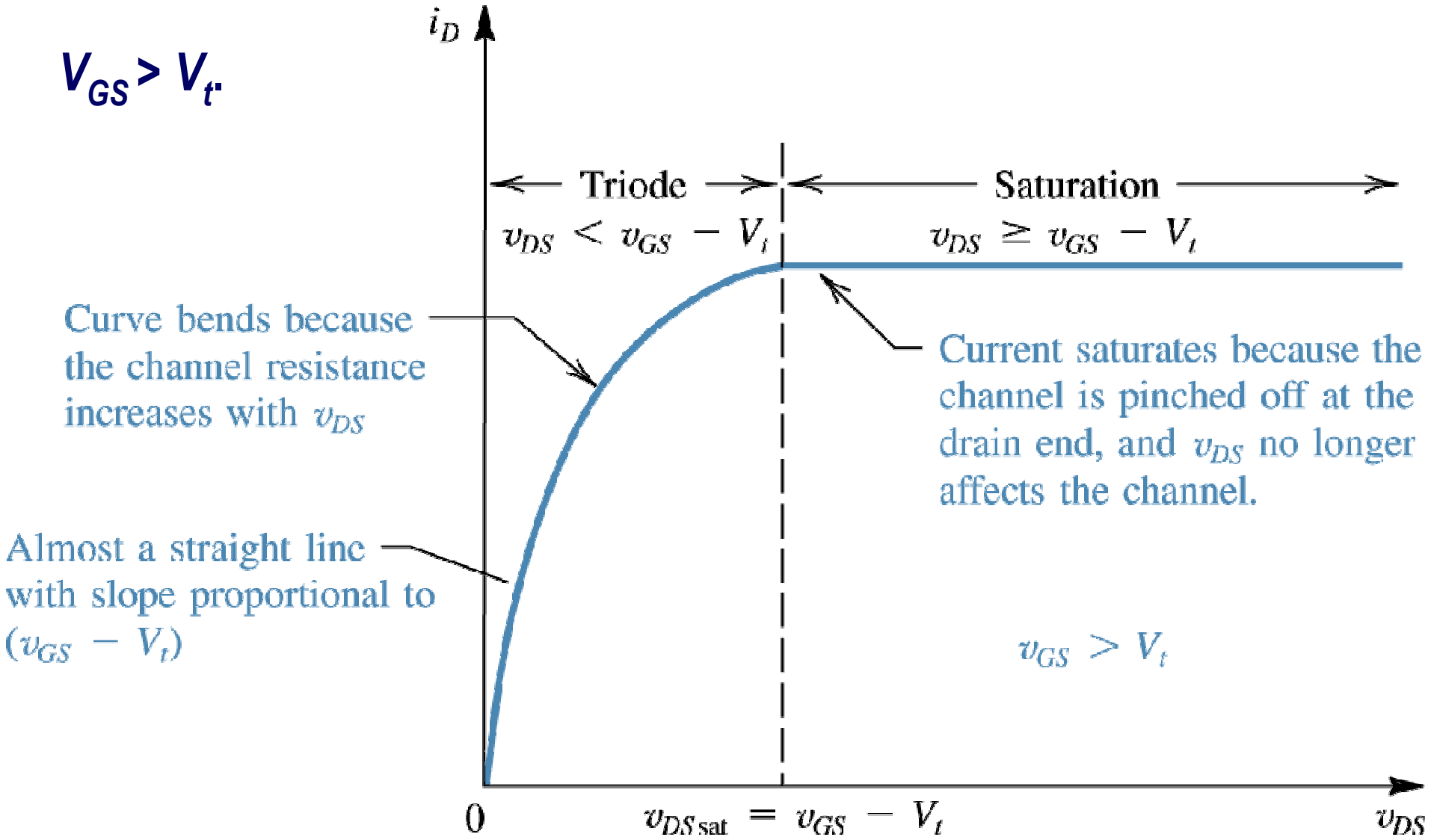
nMOS operation - V_{DS} is increased



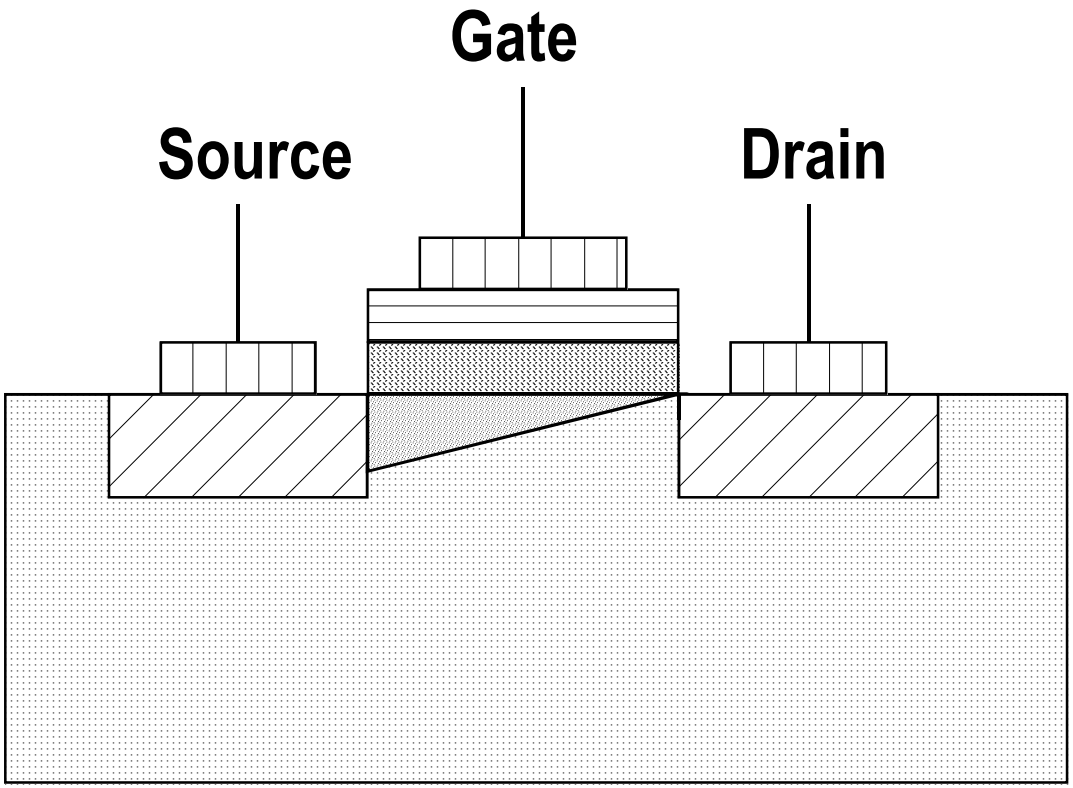
The induced channel acquires a tapered shape and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

The drain current versus the drain-to-source voltage V_{DS}

$V_{GS} > V_t$.



nMOS Transistor Near The Saturation



Metal

Polysilicon

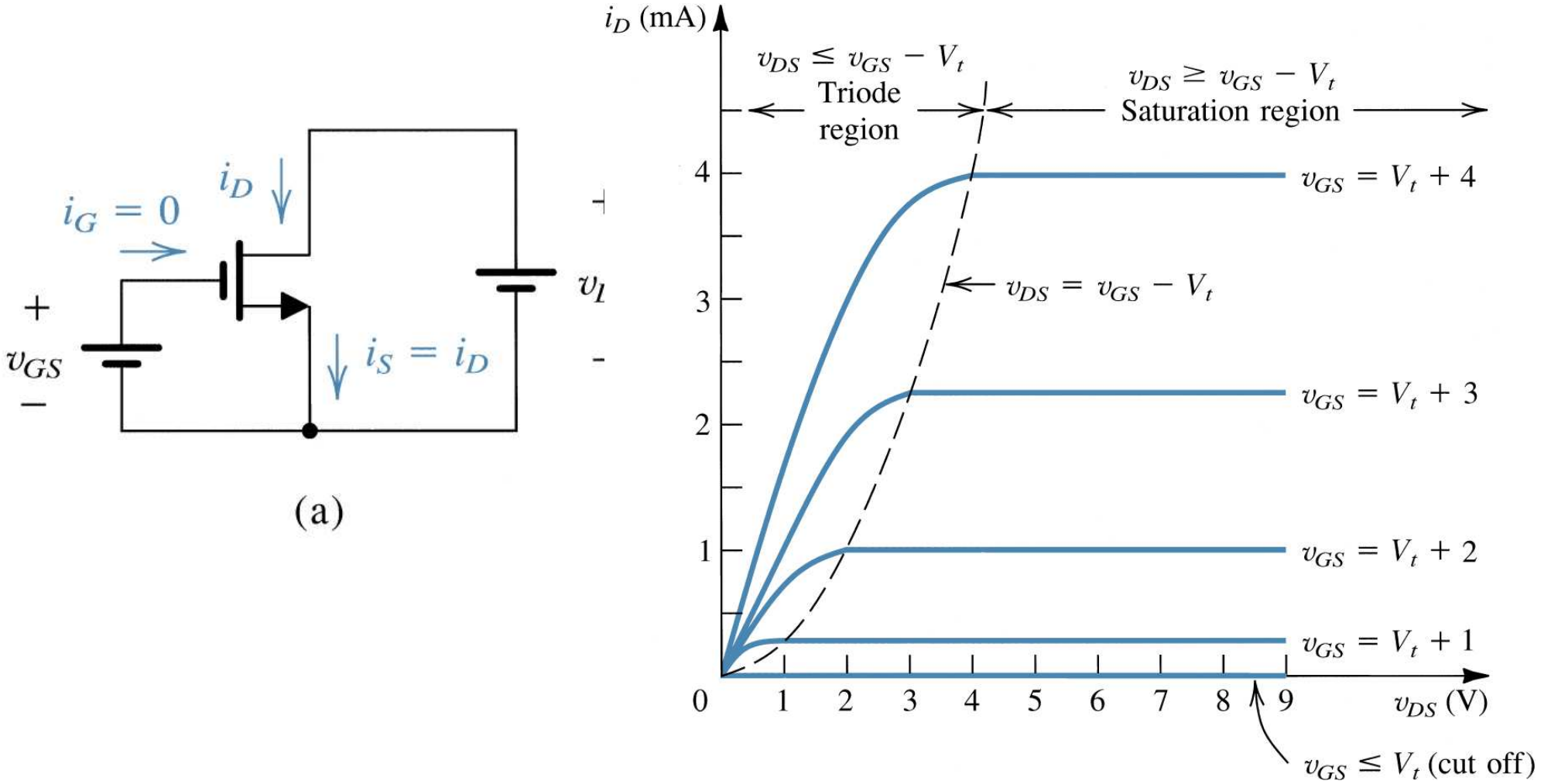
Silicon dioxide

N-type diffusion

P-type substrate

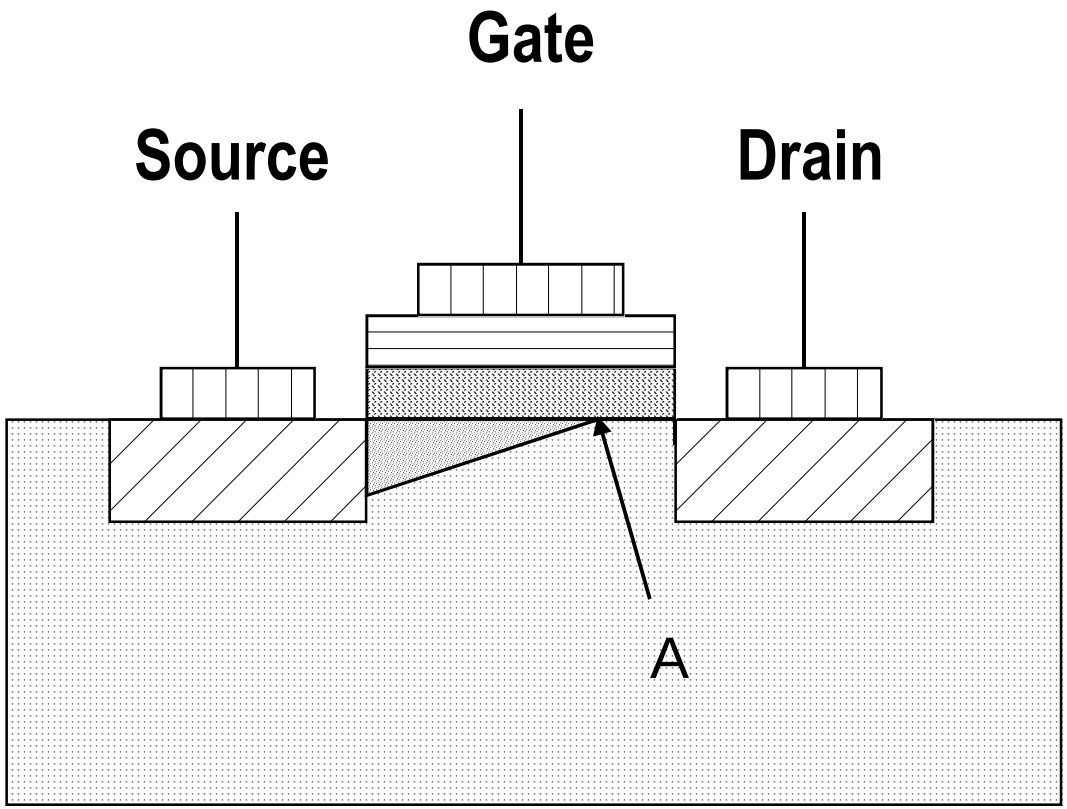
Channel

nMOS transistor operation – output characteristic



The output (i_D – v_{DS})characteristics for a device with V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2.

Saturated nMOS Transistor



Metal

Polysilicon

Silicon dioxide

N-type diffusion

P-type substrate

Channel

Saturated nMOS Transistor

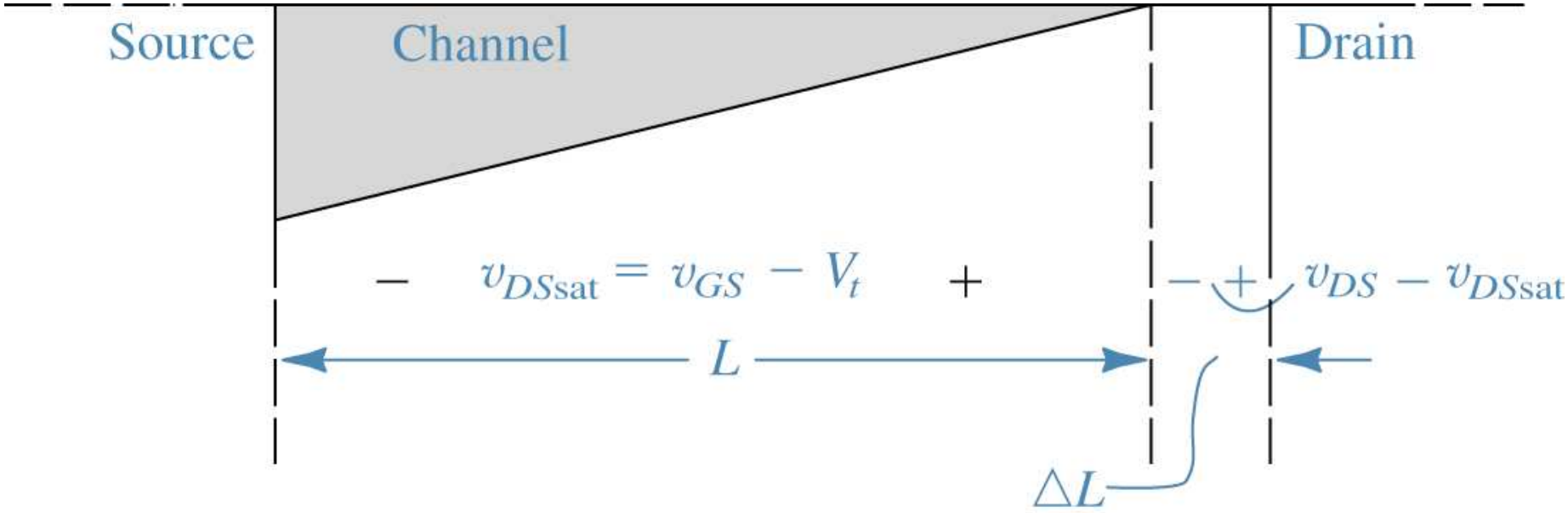


Fig. 5.15 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

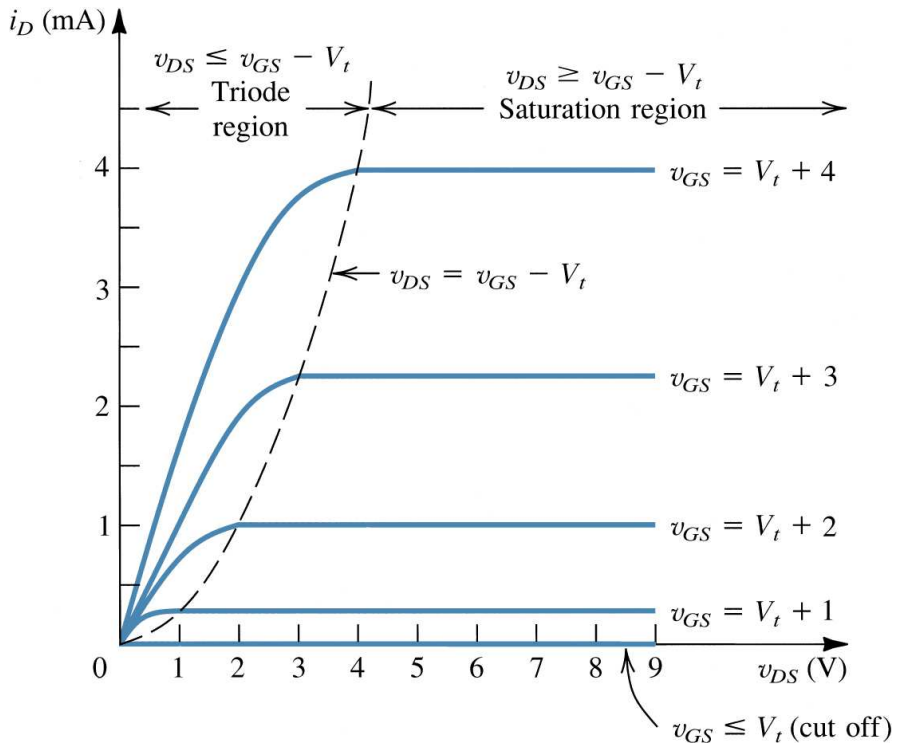


Fig. 5.11 (a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D - v_{DS} characteristics for a device with V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2.

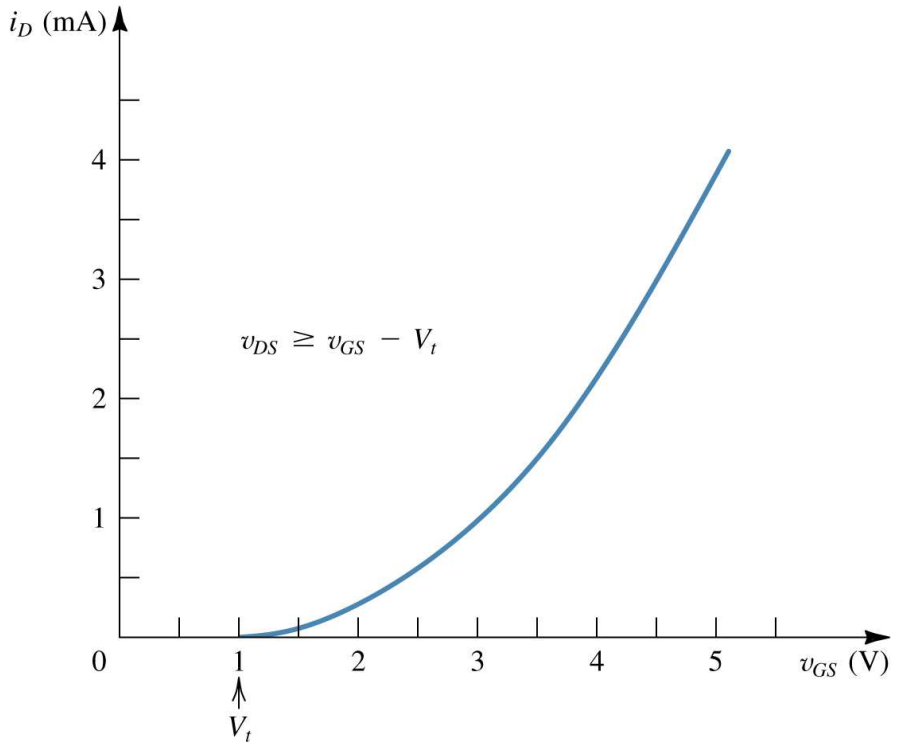


Fig. 5.12 The i_D - v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2).

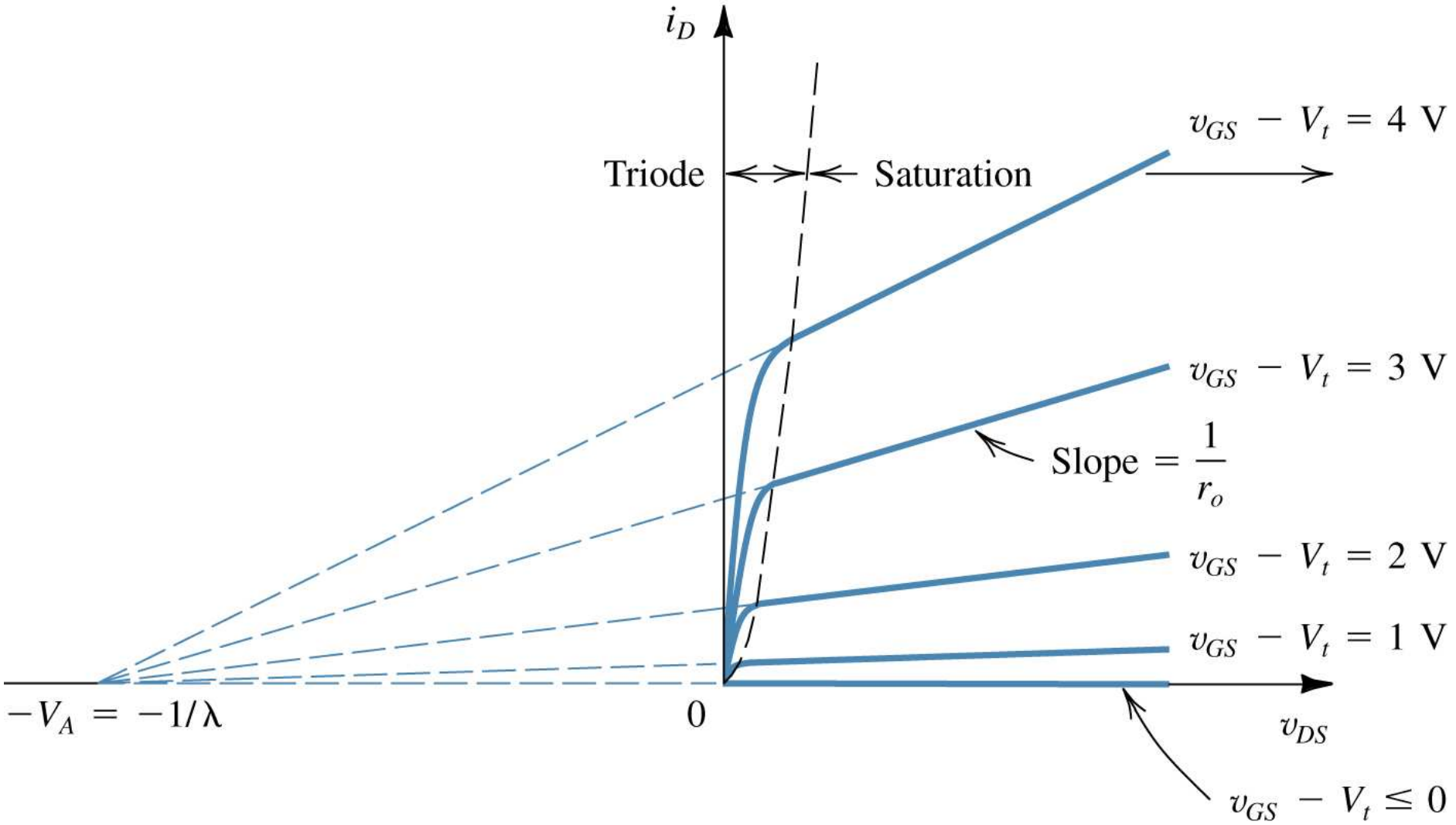


Fig. 5.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A is typically in the range of 30 to 200 V.

Depletion-type n-channel MOSFET

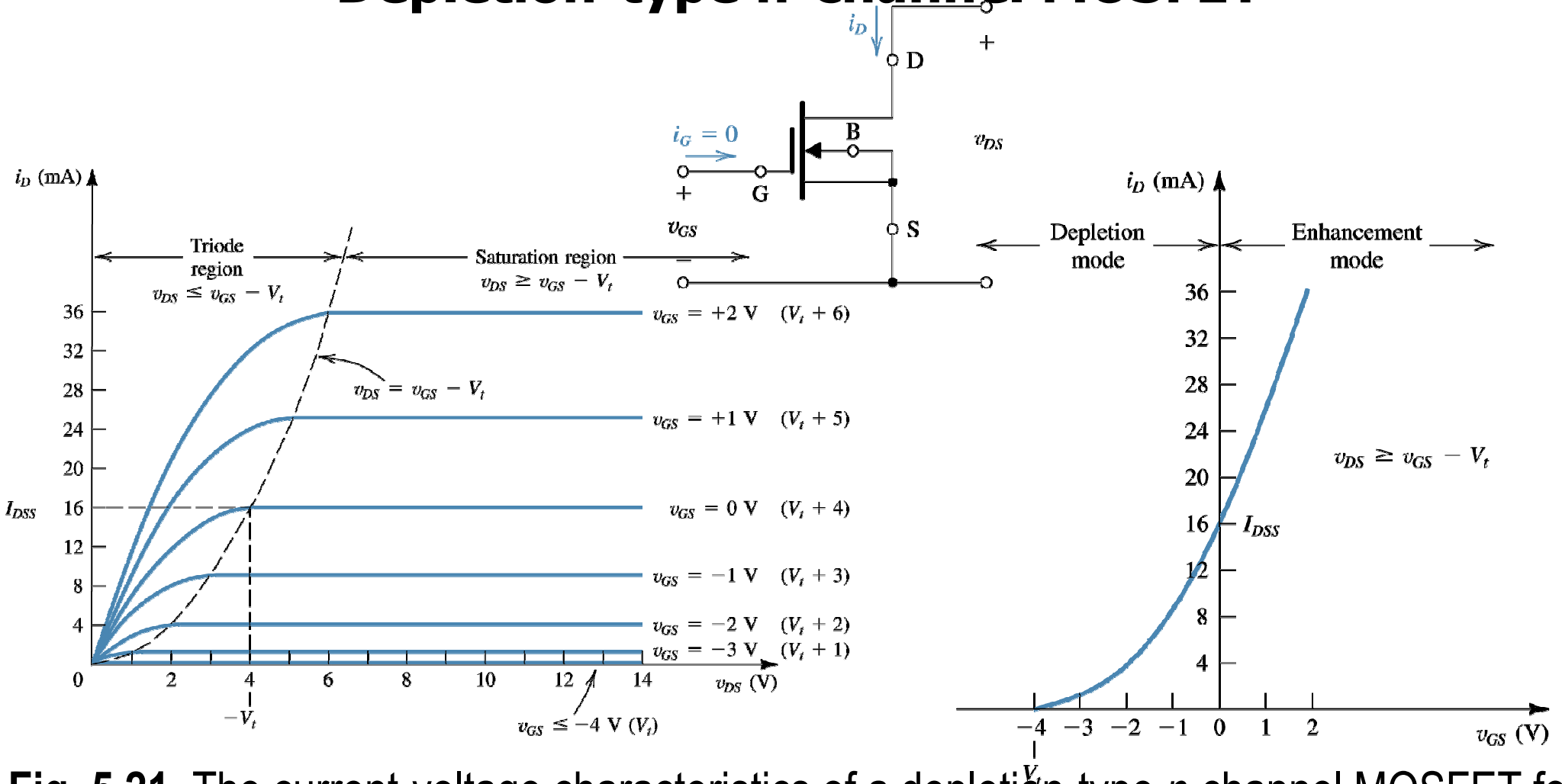


Fig. 5.21 The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which V_t = -4 V and $k'_n(W/L)$ = 2 mA/V^2: **(a)** transistor with current and voltage polarities indicated; **(b)** the i_D - v_{DS} characteristics; **(c)** the i_D - v_{GS} characteristic in saturation.

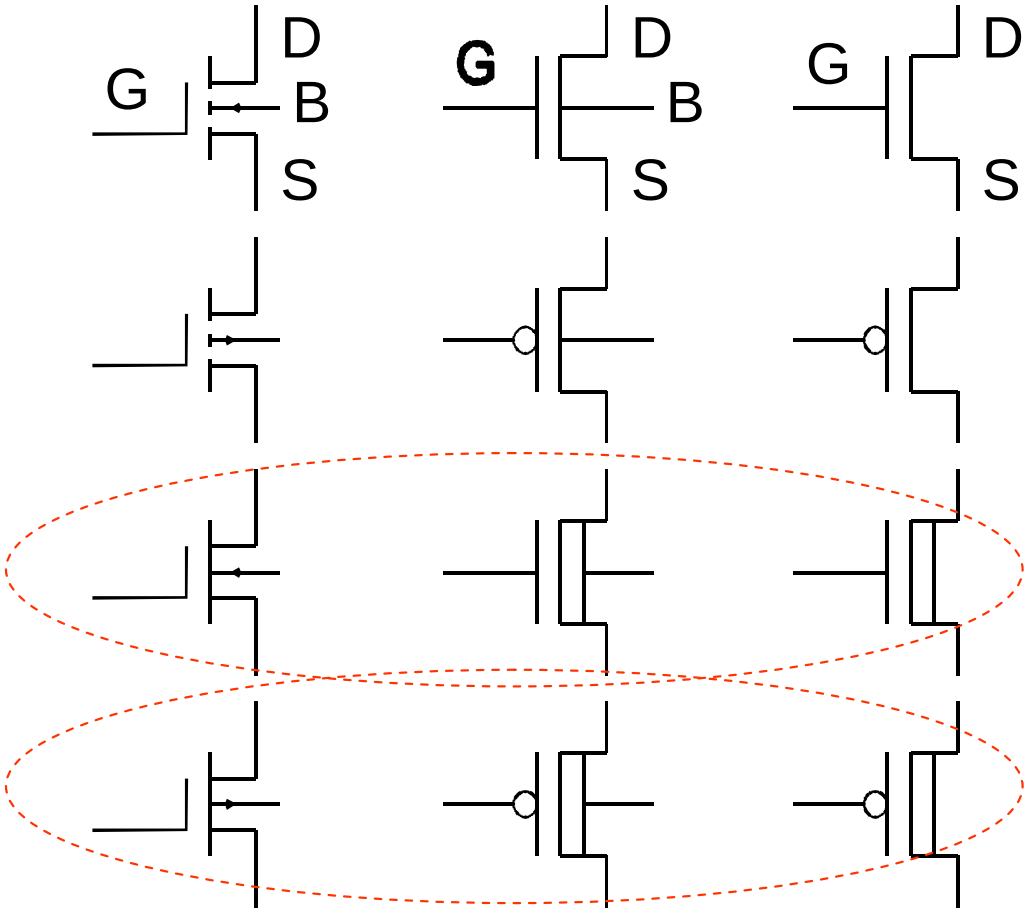
MOS Transistor Symbols

Enhanced Mode n-type Transistor

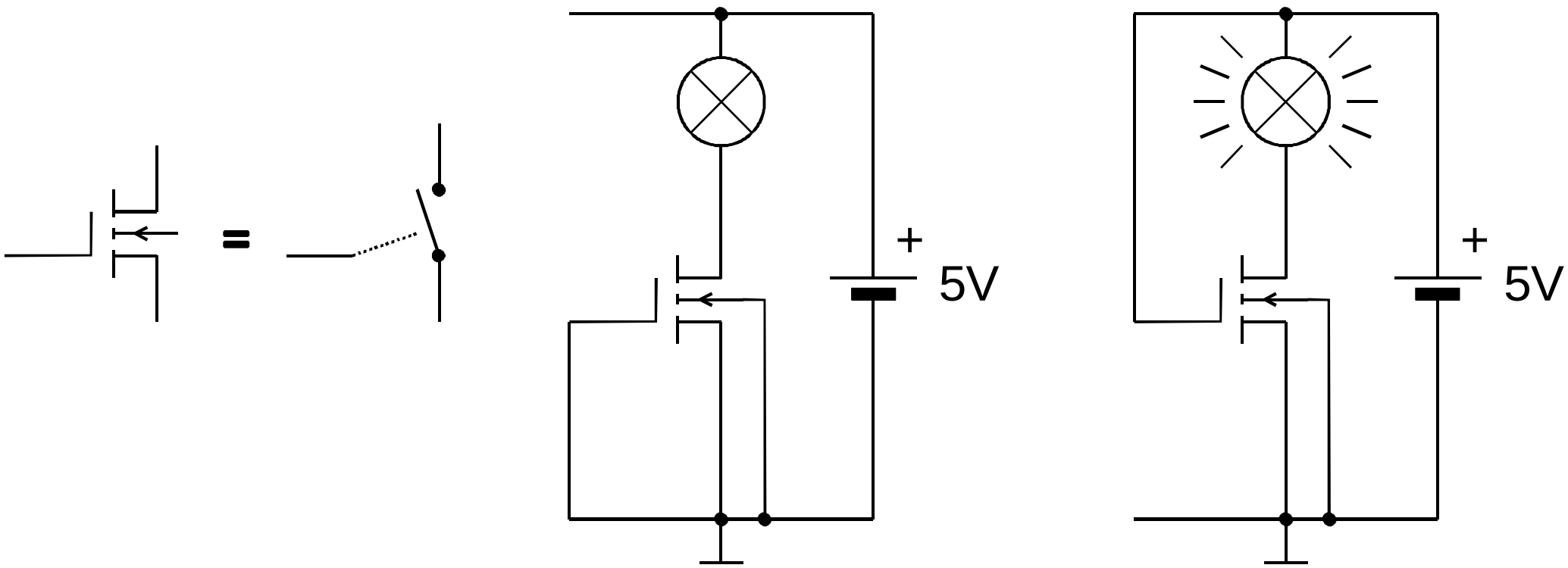
Enhanced Mode p-type Transistor

Depleted Mode n-type Transistor

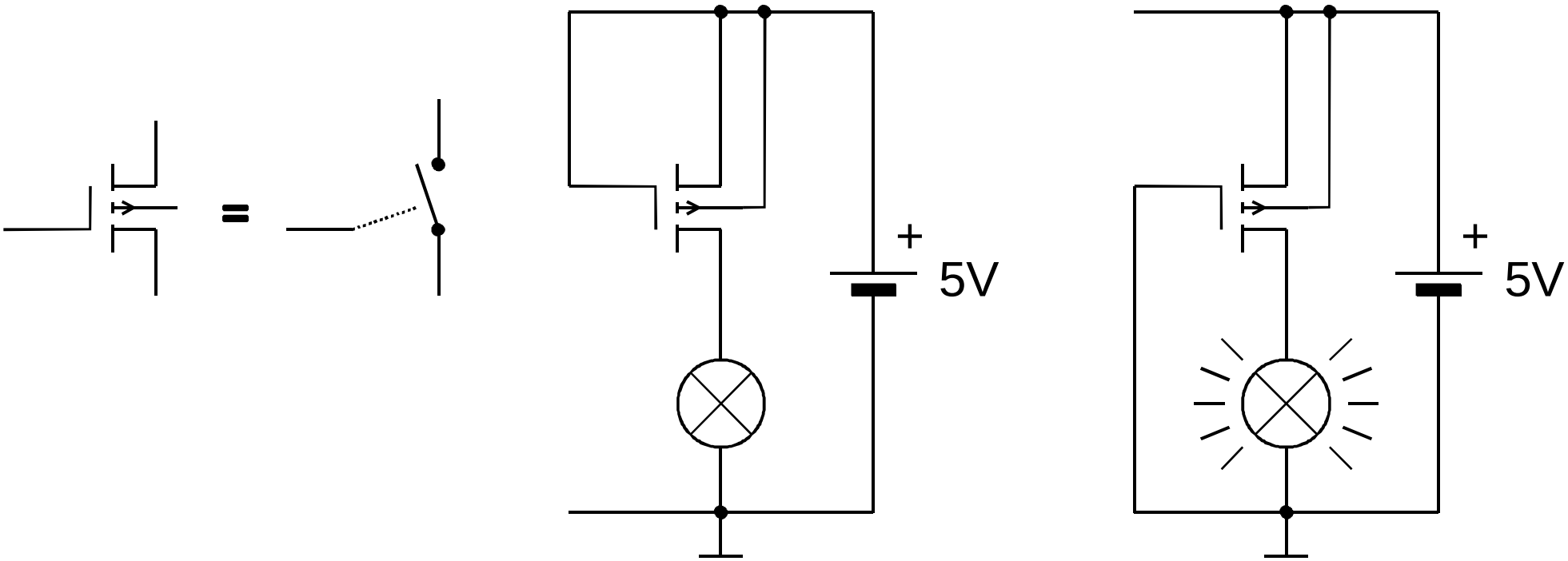
Depleted Mode p-type Transistor



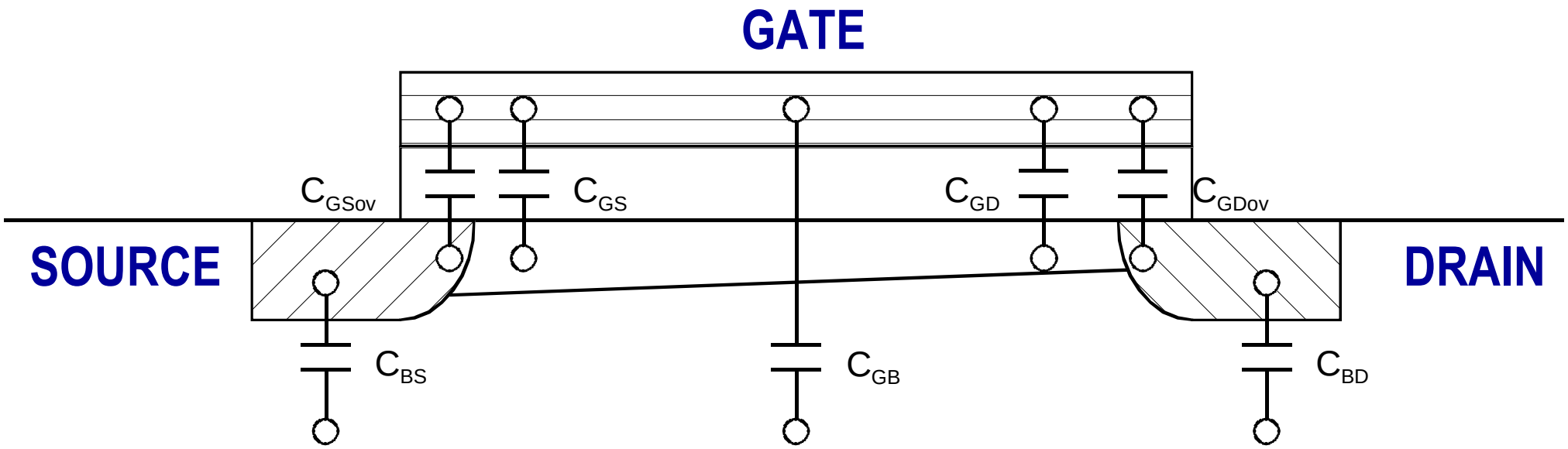
nMOS Transistor As a Switch



pMOS Transistor As a Switch

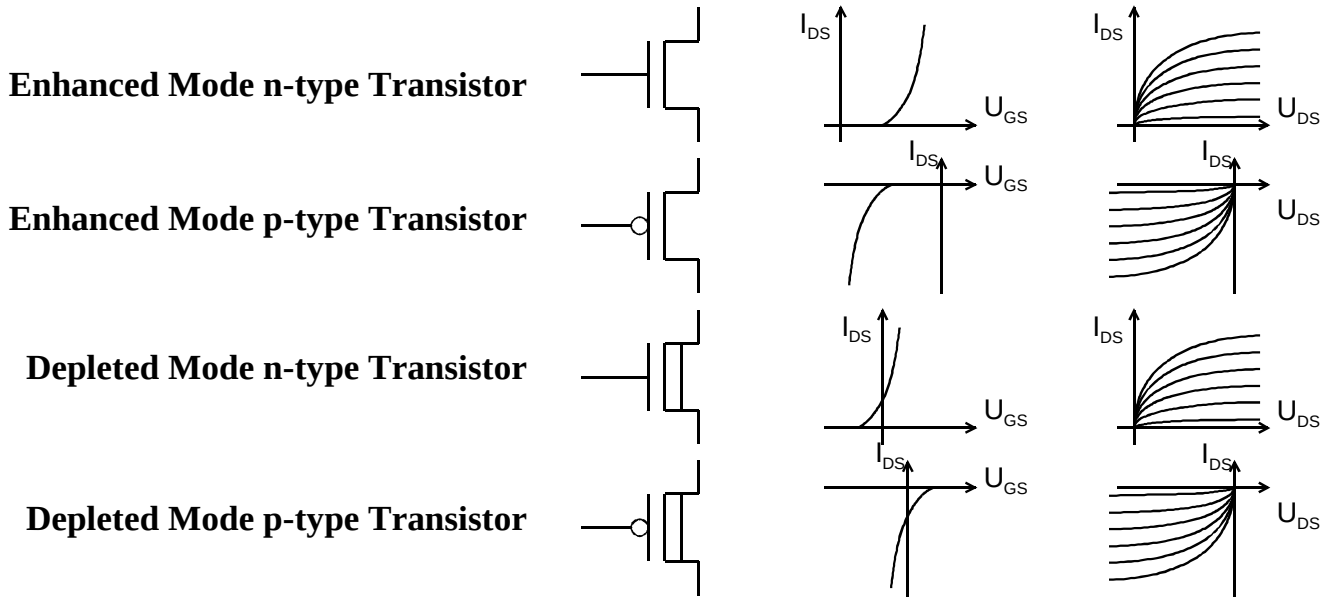


MOS Transistor Capacitances



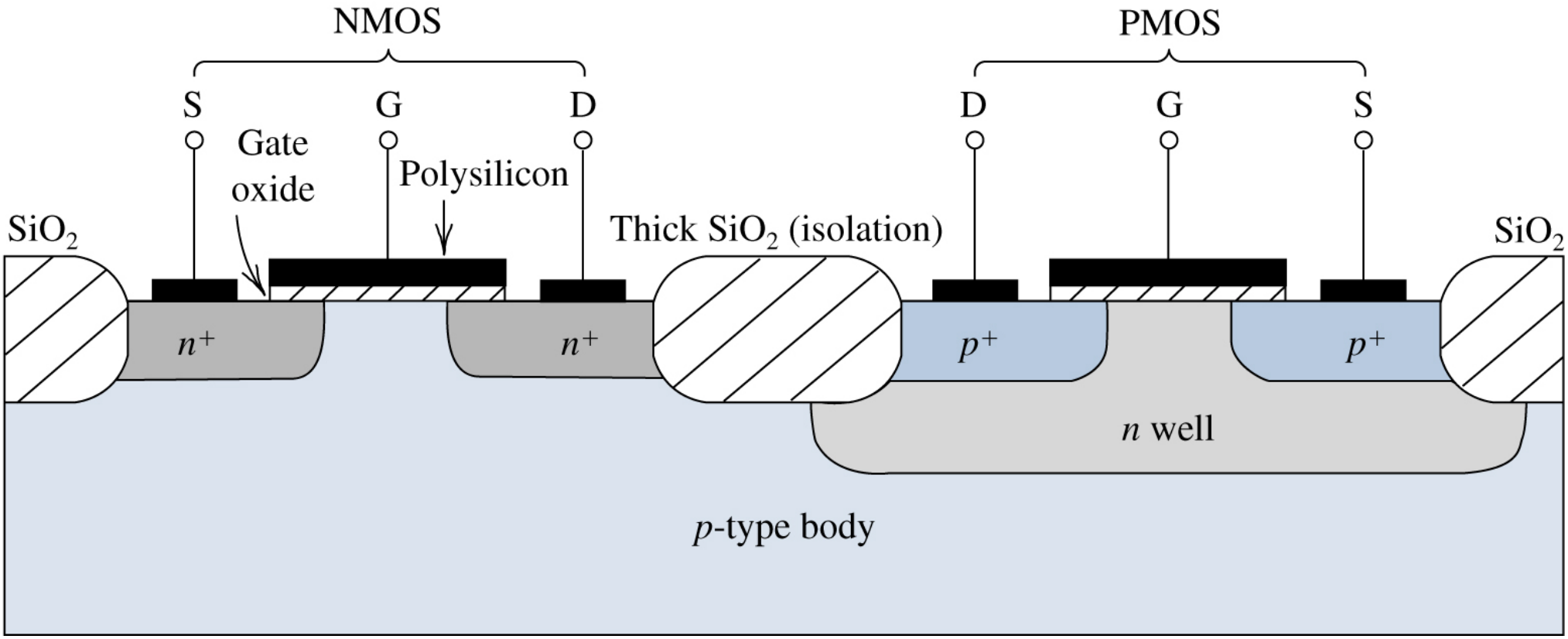
MOS Transistor - summary

Zakres pracy	Napięcia na końcówkach
Zakres odcięcia, nieprzewodzenia	$U_{GS}<U_{FB}$
Zakres liniowy, nienasycenia, triodowy	$U_{GS}\geq V_T$ i $U_{DS}<U_{Dsat}$
Zakres nasycenia, pentodowy	$U_{GS}\geq V_T$ i $U_{DS}\geq U_{Dsat}$
Zakres podprogowy, słabej inwersji	$U_{FB}\leq U_{GS}<V_T$



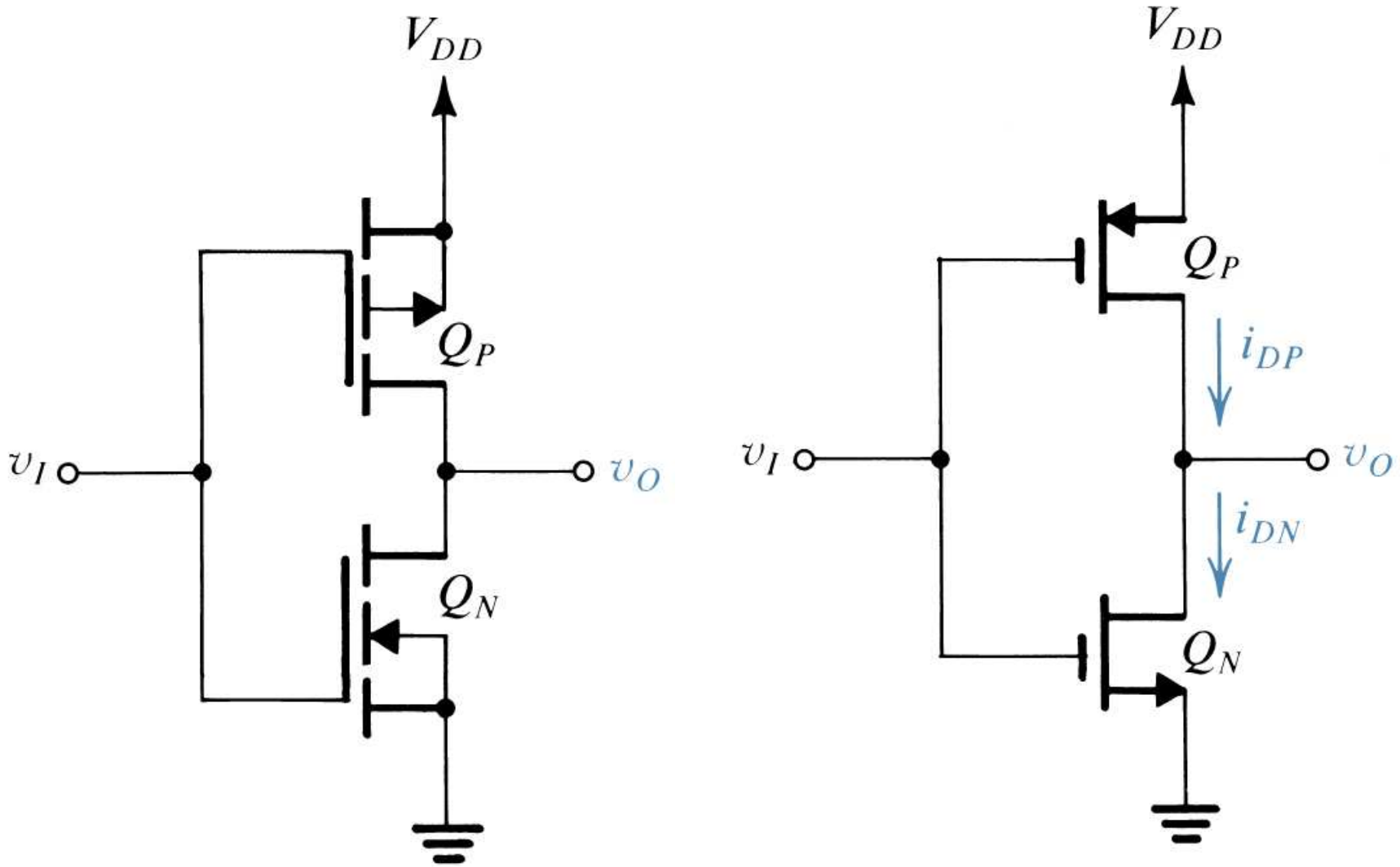
CMOS Inverter

CMOS inverter cross-section

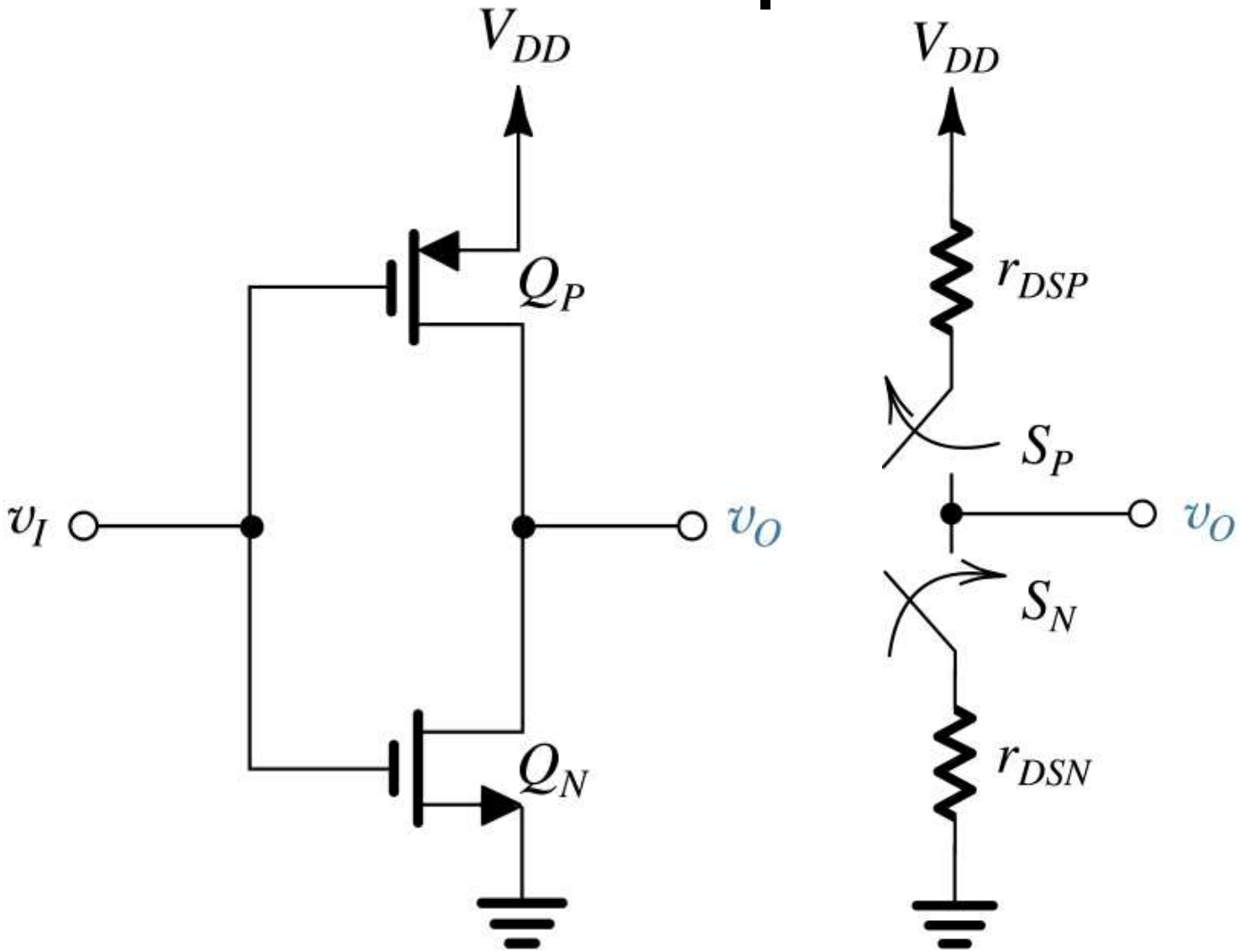


Note that the PMOS transistor is formed in a separate *n*-type region, known as an ***n* well**. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a ***p* well**.

CMOS inverter scheme



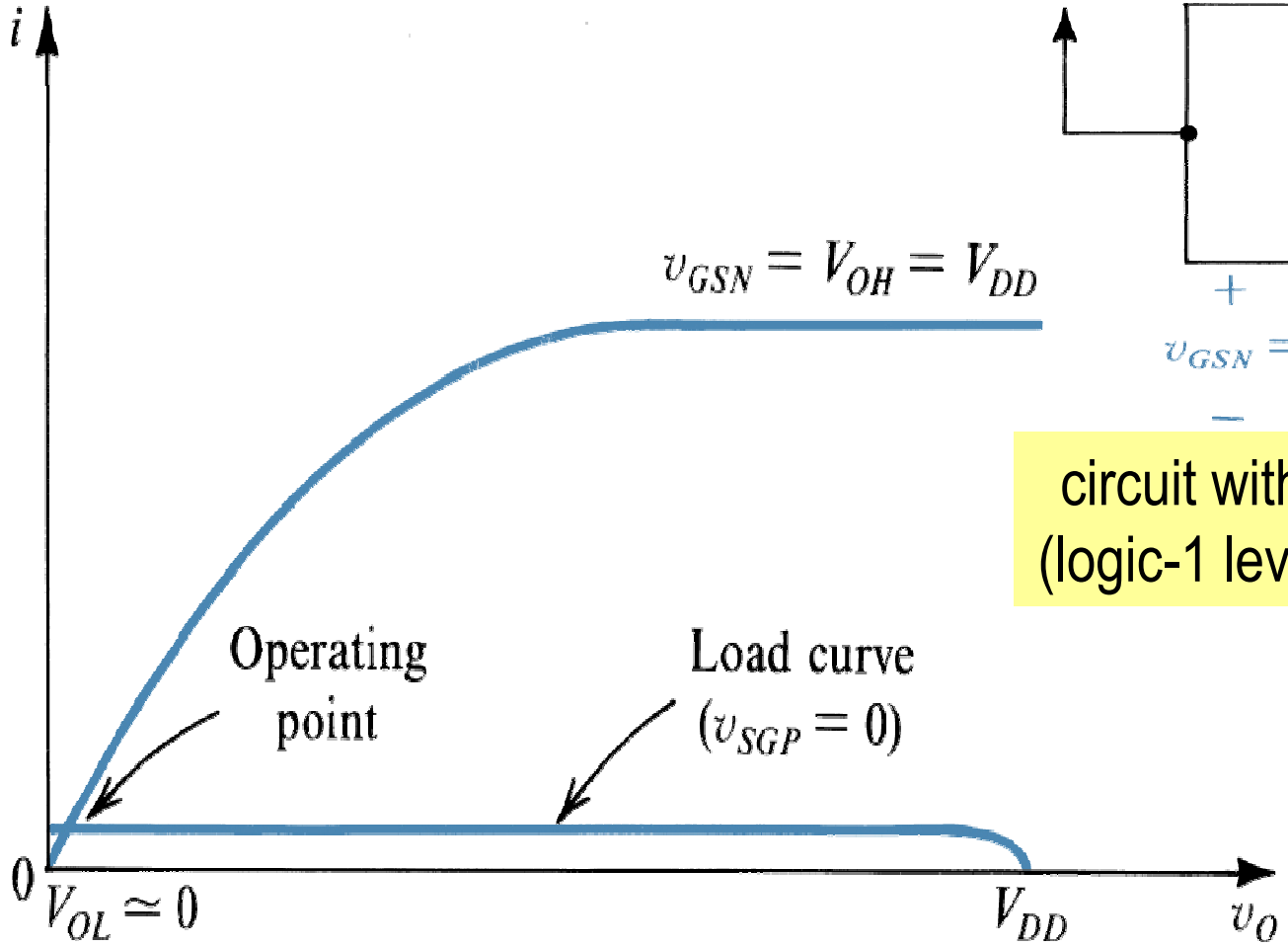
CMOS inverter and pair of switches

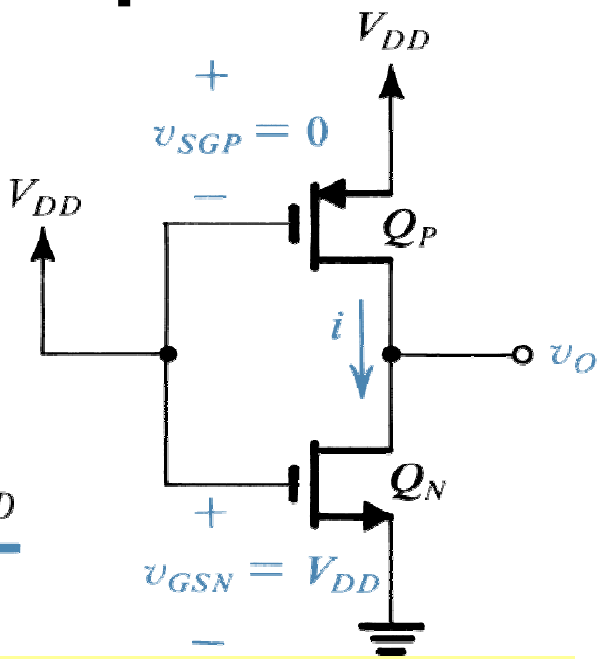


Note: switches must operate in a complementary fashion.

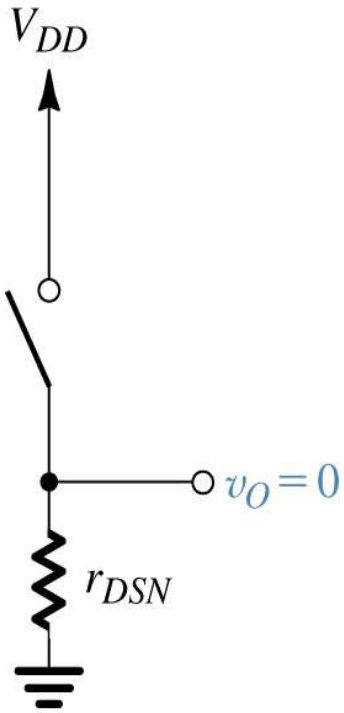
CMOS inverter operation

v_1 is high





circuit with v1 = VDD (logic-1 level, or VOH);

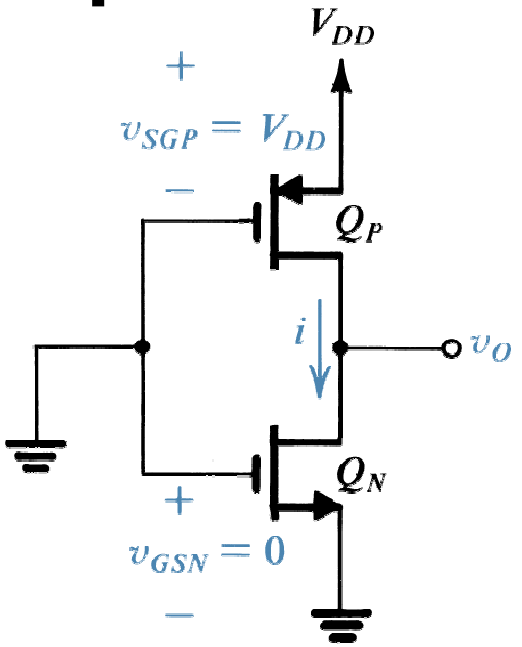


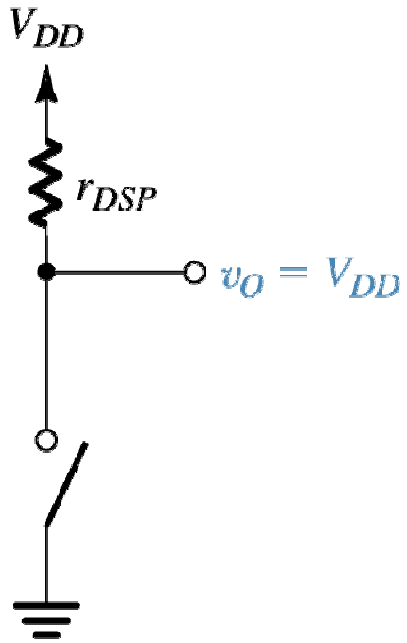
equivalent circuit.

graphical construction to determine the operating point

CMOS inverter operation

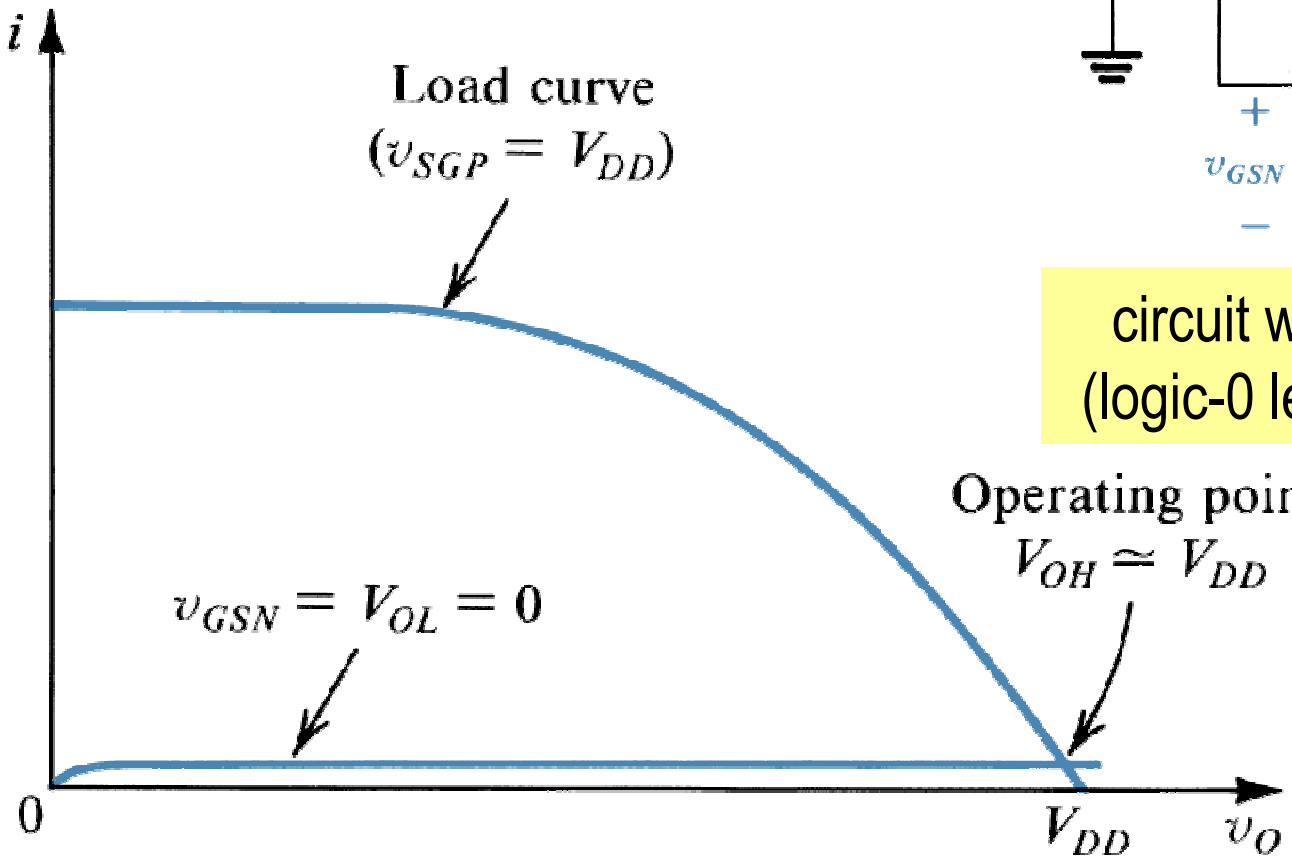
v_1 is low





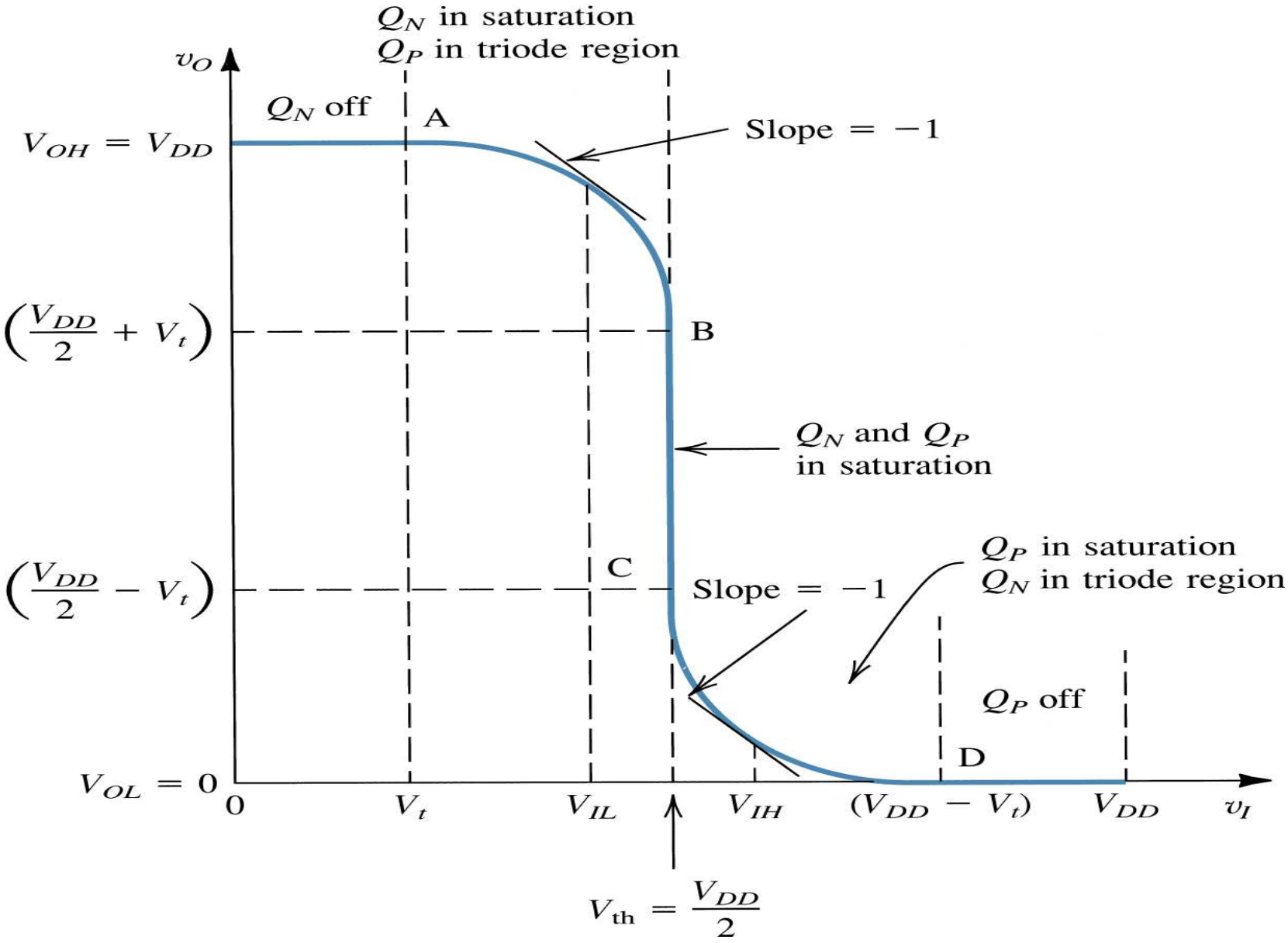
circuit with v1 = 0V (logic-0 level, or V_{OL});

equivalent circuit.

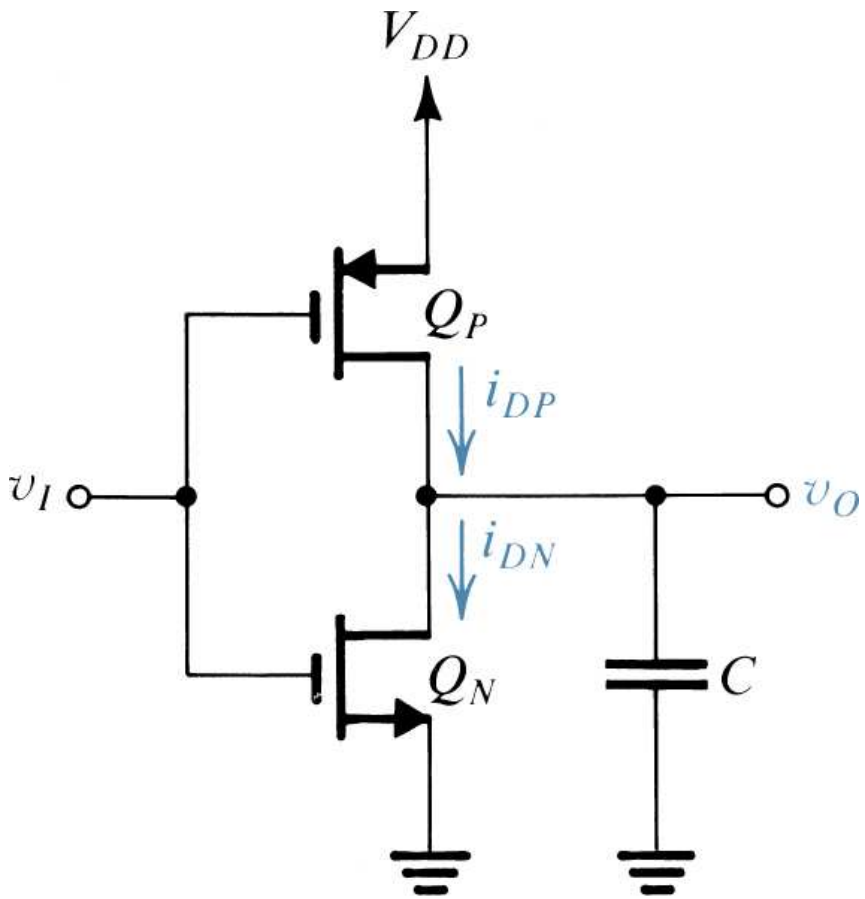


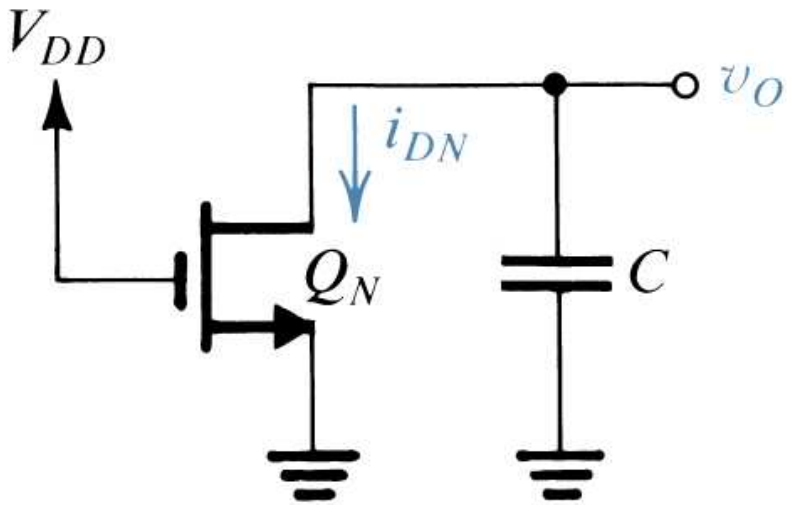
graphical construction to determine the operating point

Voltage transfer characteristic of the CMOS inverter



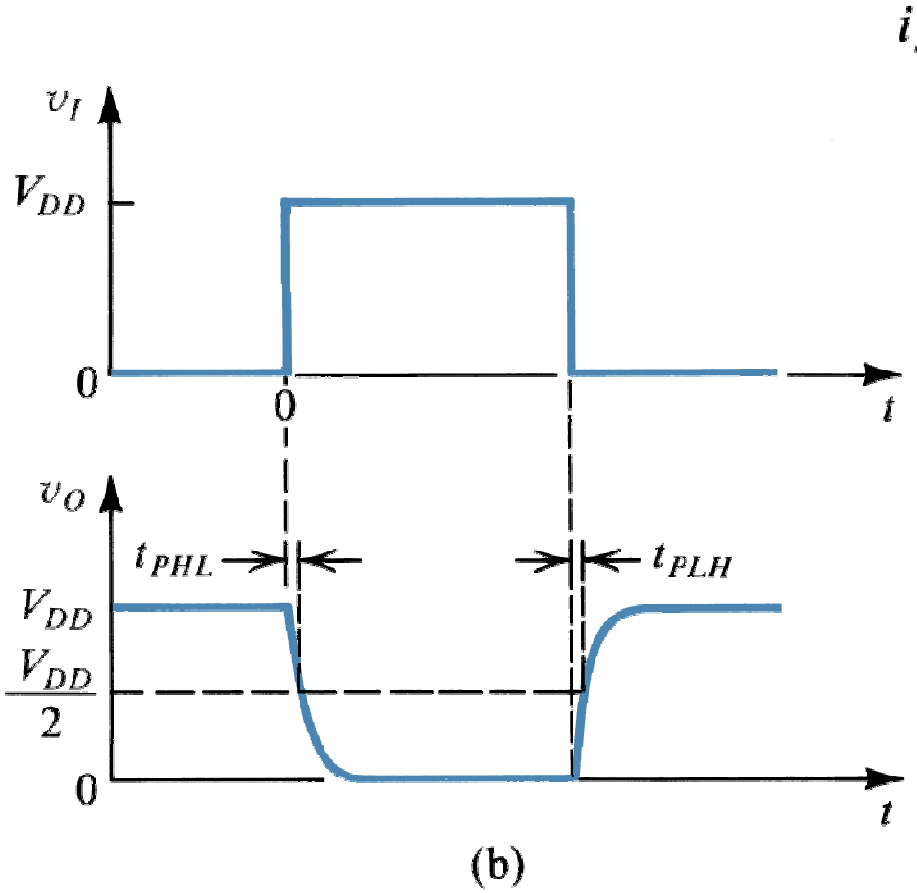
Dynamic operation of a capacitive loaded CMOS inverter



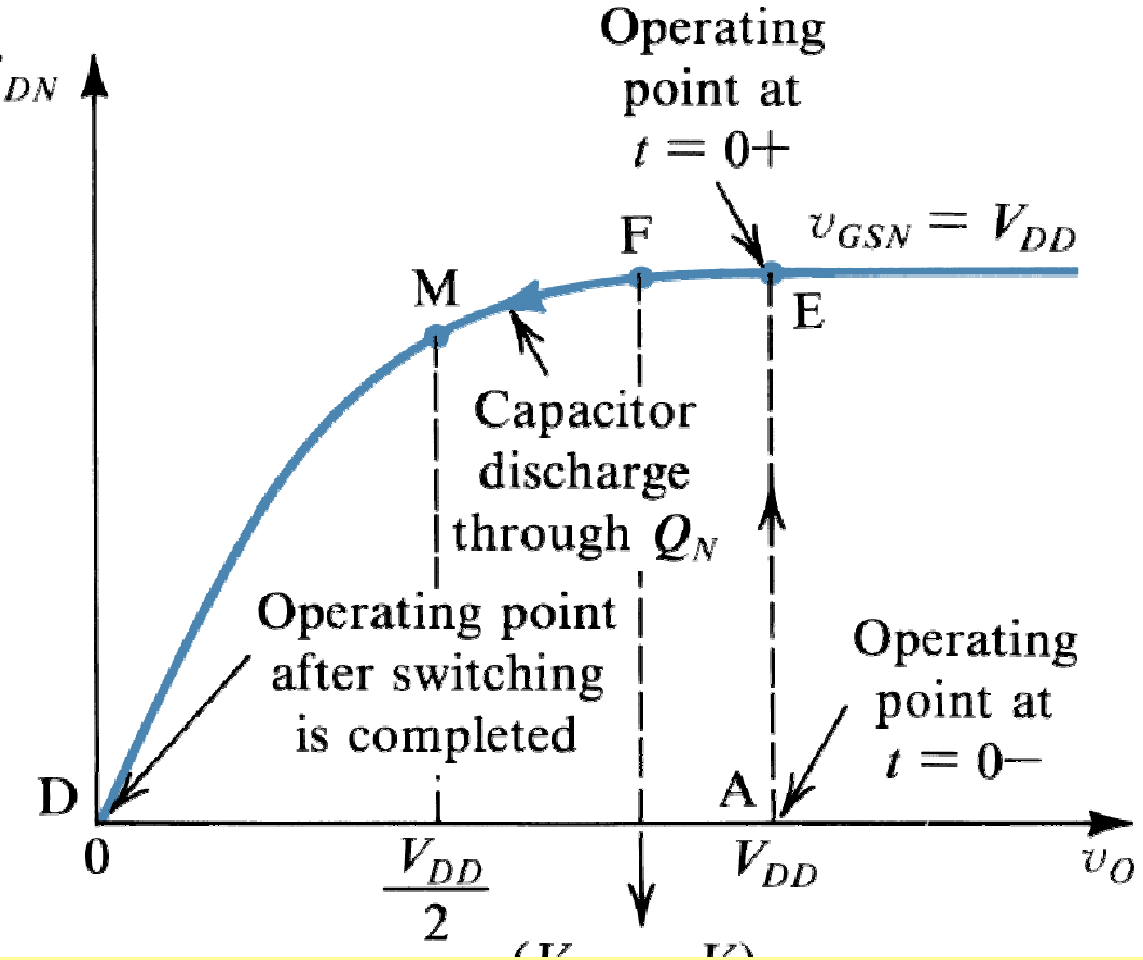


equivalent circuit during the capacitor discharge.

Dynamic operation of a capacitive loaded CMOS inverter



input and output waveforms



trajectory of the operating point as the input goes high and C discharges through the Q_N